# FAIRCHILD

SEMICONDUCTOR

# FQP9N50C/FQPF9N50C 500V N-Channel MOSFET

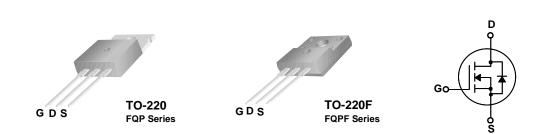
# **General Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

#### Features

- 9 A, 500V,  $R_{DS(on)} = 0.8 \Omega @V_{GS} = 10 V$
- Low gate charge (typical 28 nC)
- Low Crss (typical 24 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQP9N50C	FQPF9N50C	Units	
V <sub>DSS</sub>	Drain-Source Voltage		5	500	
I <sub>D</sub>	Drain Current - Continuous ( $T_C = 25^{\circ}C$ )		9	9 *	А
	- Continuous (T <sub>C</sub> = 100°C)		5.4	5.4 *	А
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	36	36 *	А
V <sub>GSS</sub>	Gate-Source Voltage		±	30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		360		mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	9		А
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		13.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4	.5	V/ns
P <sub>D</sub>	Power Dissipation ( $T_c = 25^{\circ}C$ )		135	44	W
	- Derate above 25°C		1.07	0.35	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to	o +150	°C
TL	Maximum lead temperature for soldering purposes,		200		°C
'L	1/8" from case for 5 seconds	300			
Drain current lim	ited by maximum junction temperature		÷		

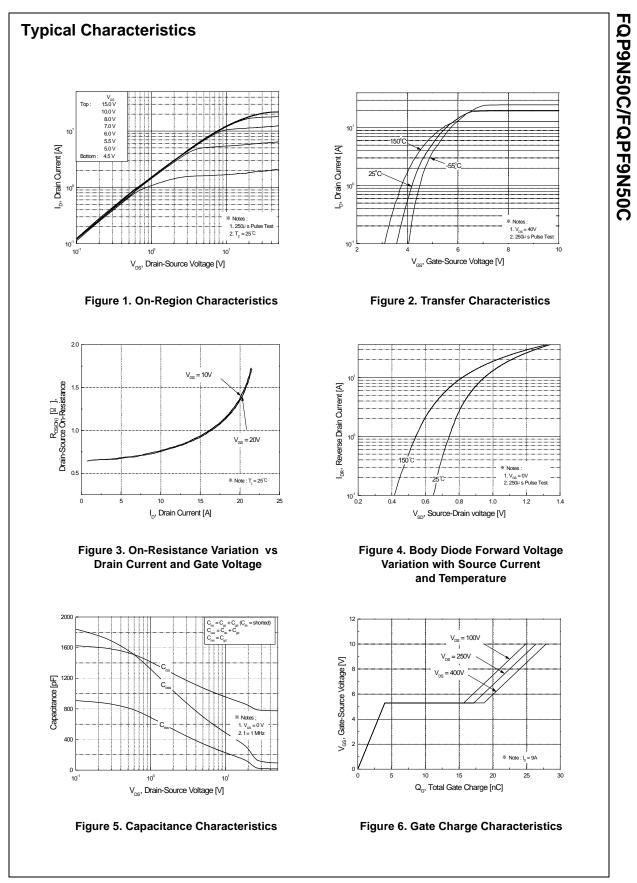
## **Thermal Characteristics**

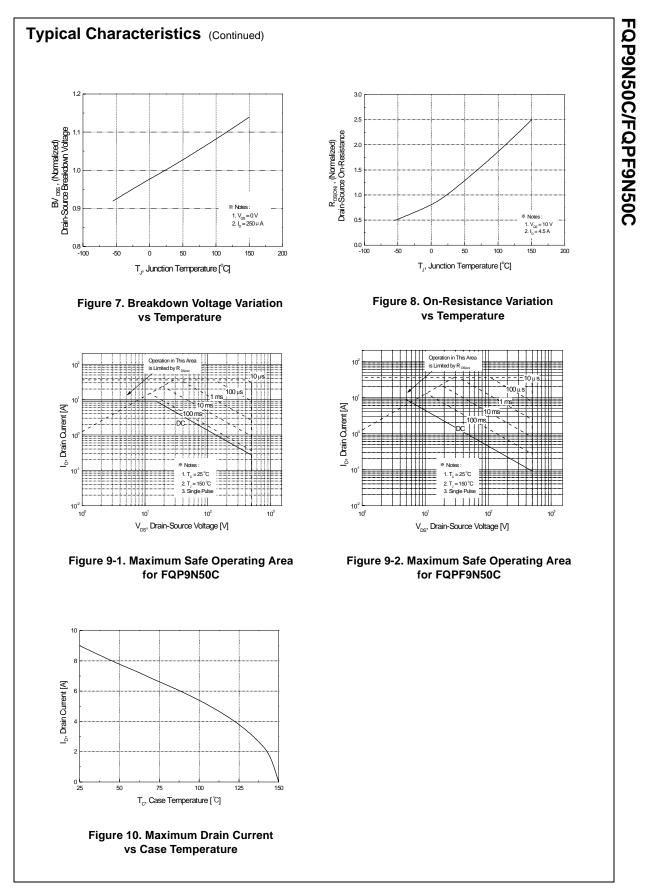
Symbol	Parameter	FQP9N50C	FQPF9N50C	Units	
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction-to-Case	0.93	2.86	°C/W	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5		°C/W	
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W	

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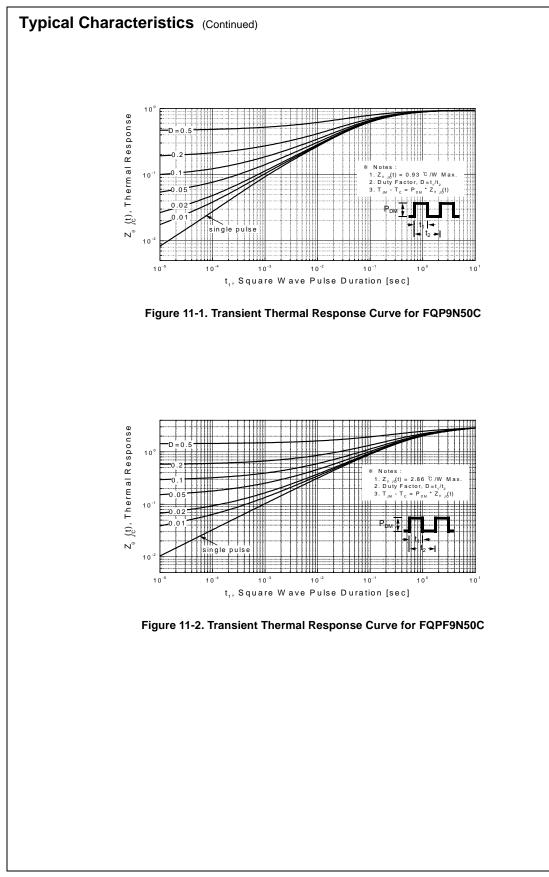
**FET**<sup>™</sup>

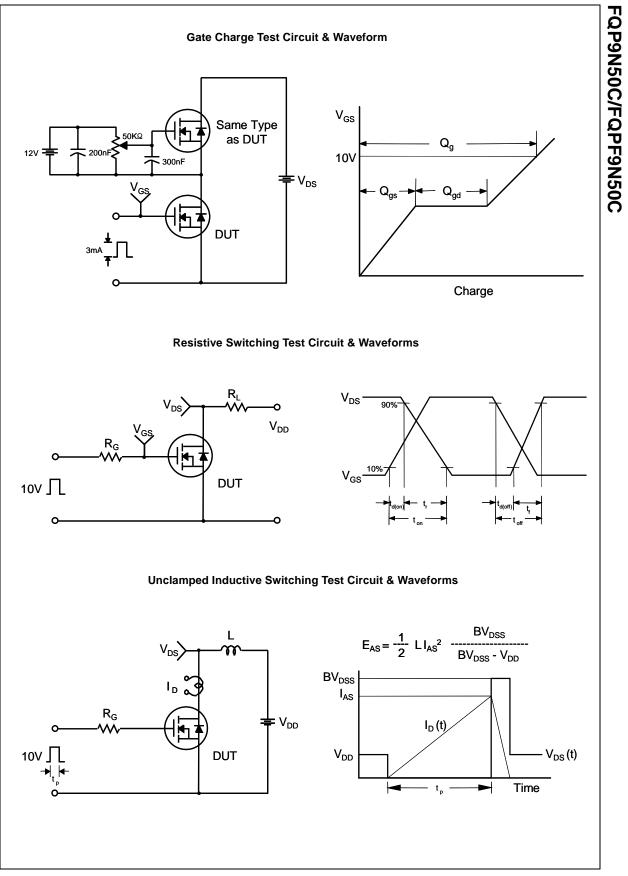
Symbol	Parameter	Test Conditions	Min	Тур	Мах	Units
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, Referenced to 25°C		0.57		V/°C
DSS		V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			1	μA
	Zero Gate Voltage Drain Current	$V_{DS} = 400 \text{ V}, \text{ T}_{C} = 125^{\circ}\text{C}$			10	μA
GSSF	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			100	nA
GSSR	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
/ <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 4.5 \text{ A}$		0.65	0.8	Ω
FS	Forward Transconductance	$V_{DS} = 40 \text{ V}, \text{ I}_{D} = 4.5 \text{ A}$ (Note 4)		6.5		S
	ic Characteristics					
Siss	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		790	1030	pF
Coss	Output Capacitance	f = 1.0 MHz		130	170	pF
Srss	Reverse Transfer Capacitance			24	30	pF
Switchi	ing Characteristics					
d(on)	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 9 A,		18	45	ns
r	Turn-On Rise Time	$R_{G} = 25 \Omega$		65	140	ns
d(off)	Turn-Off Delay Time			93	195	ns
f	Turn-Off Fall Time	(Note 4, 5)		64	125	ns
ζ <sup>g</sup>	Total Gate Charge	$V_{DS} = 400 \text{ V}, \text{ I}_{D} = 9 \text{ A},$		28	35	nC
Հ <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		4		nC
ጋ <sub>gd</sub>	Gate-Drain Charge	(Note 4, 5)		15		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
s	Maximum Continuous Drain-Source Did	•			9	А
SM	Maximum Pulsed Drain-Source Diode F	Forward Current			36	А
/ <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_{S} = 9 A$			1.4	V
rr	Reverse Recovery Time	$V_{GS} = 0 V, I_S = 9 A,$		335		ns
ל <sup>וג</sup>	Reverse Recovery Charge	$dI_{F} / dt = 100 \text{ A}/\mu \text{s} \qquad (\text{Note 4})$		2.95		μC
L = 8 mH, I <sub>SD</sub> ≤ 9A, di	tating : Pulse width limited by maximum junction tempe $I_{AS} = 9A, V_{DD} = 50V, R_G = 25 \Omega$ , Starting $T_J = 25^{\circ}C$ /dt $\leq 200A/\mus, V_{DD} \leq BV_{DSS}$ , Starting $T_J = 25^{\circ}C$ Pulse width $\leq 300\mu s$ , Duty cycle $\leq 2\%$ ndependent of operating temperature	rature				

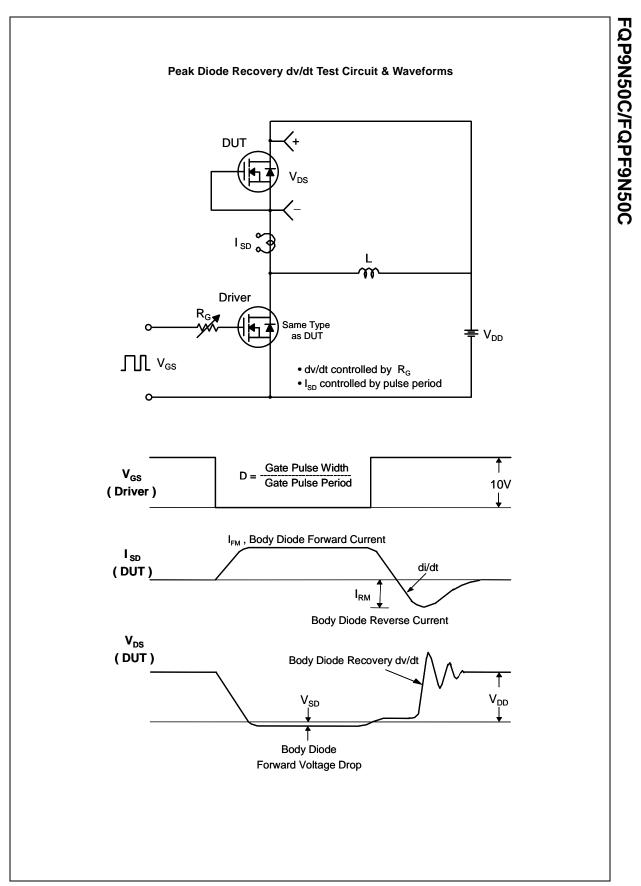


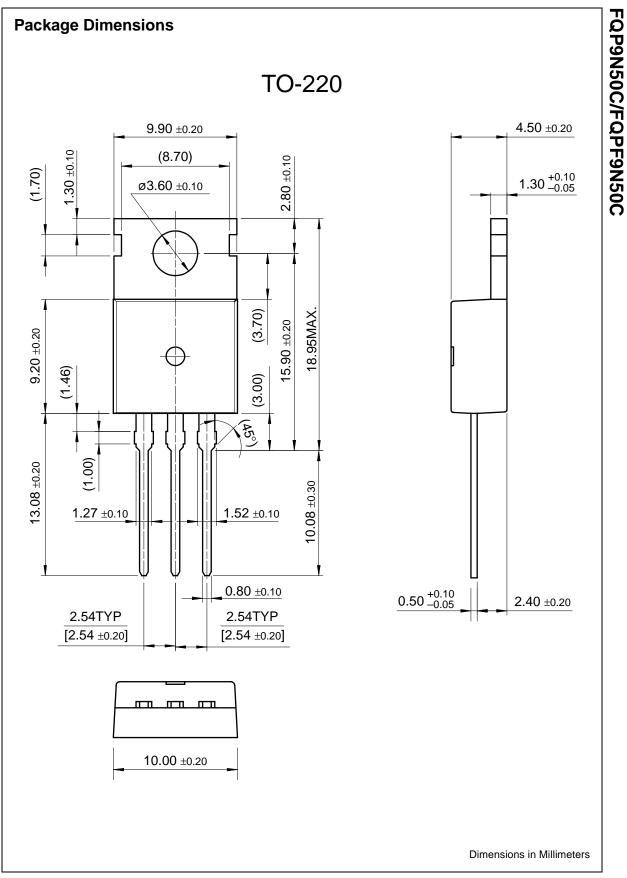


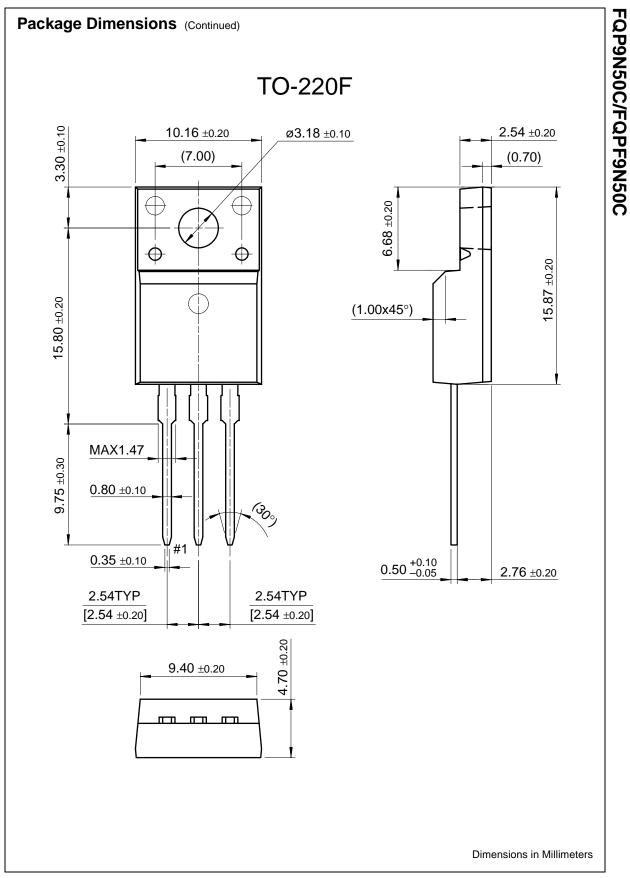
Rev. A, June 2003











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## **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.



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## FQPF9N50C

**General description** 

500V N-Channel Advance Q-FET C-Series

#### Contents

 General description Features •Product status/pricing/packaging •Order Samples

 Models Qualification Support

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datasheet

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### back to top

### **Features**

• 9A, 500V

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- Low gate charge (typical 28 nC)
- Low Crss (typical 24 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

### back to top

Product status/pricing/packaging



This page Print version

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Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FQPF9N50C	Full Production	Full Production	\$1.10	<u>TO-220F</u>	3		Line 1: <b>\$Y</b> (Fairchild logo) & <b>Z</b> (Asm. Plant Code) & <b>4</b> (4-Digit Date Code) Line 2: FQPF Line 3: 9N50C
FQPF9N50CT	Full Production	Full Production	\$1.14	<u>TO-220F</u>	3		Line 1: <b>\$Y</b> (Fairchild logo) & <b>Z</b> (Asm. Plant Code) & <b>4</b> (4-Digit Date Code)
FQPF9N50CYDTU	Preliminary	Ø	\$1.20	TO-220F	3		Line 1: <b>\$Y</b> (Fairchild logo) & <b>Z</b> (Asm. Plant Code) &E& <b>3</b> (3-Digit Date Code) Line 2: FQPF Line 3: 9N50C

\* Fairchild 1,000 piece Budgetary Pricing \*\* A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a <u>Fairchild distributor</u> to obtain samples

Ø Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FQPF9N50C is available. Click here for more information.

## back to top

## Models

Package & leads	Condition	Temperature range	ange Vcc range Software version Revision		Revision date
		PSPICE			
TO-220F-3	O-220F-3 <u>Electrical/Thermal</u> -55°C to 150°C		0V to 50V	OrCAD 10.3	Jul 27, 2007

## back to top

## **Qualification Support**

Click on a product for detailed qualification data

Product
FQPF9N50C
FQPF9N50CT
FQPF9N50CYDTU

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