

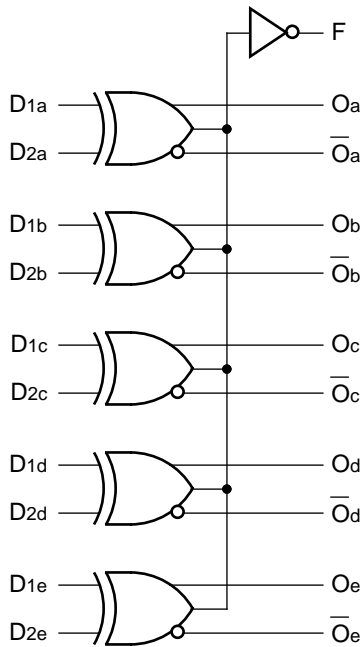
FEATURES

- Max. propagation delay of 1000ps
- IEE min. of -58mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S307 is an ultra-fast quint exclusive-OR/NOR gate designed for use in high-performance ECL systems. A function output that is the wire-OR result of the exclusive-OR outputs is also available. The inputs on the device have 75KΩ pull-down resistors.

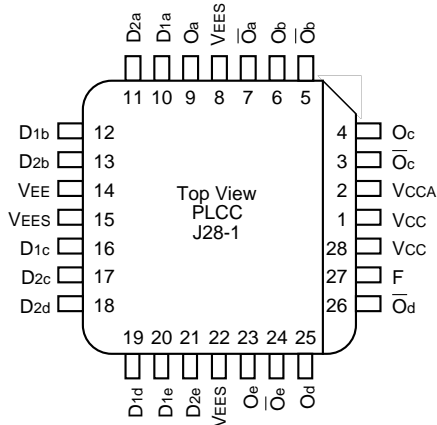
BLOCK DIAGRAM



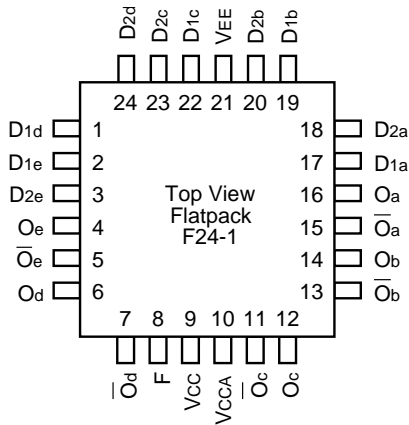
PIN NAMES

Pin	Function
D _{na} – D _{ne}	Data Inputs (n-1...5)
E	Enable Input
O _a – O _e	Data Outputs
\overline{O}_a – \overline{O}_e	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S307FC	F24-1	Commercial	SY100S307FC	Sn-Pb
SY100S307FCTR ⁽¹⁾	F24-1	Commercial	SY100S307FC	Sn-Pb
SY100S307JC	J28-1	Commercial	SY100S307JC	Sn-Pb
SY100S307JCTR ⁽¹⁾	J28-1	Commercial	SY100S307JC	Sn-Pb
SY100S307JZ ⁽²⁾	J28-1	Commercial	SY100S307JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S307JZTR ^(1, 2)	J28-1	Commercial	SY100S307JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

$$F = (D1a \oplus D2a) + (D1b \oplus D2b) + (D1c \oplus D2c) + (D1d \oplus D2d) + (D1e \oplus D2e).$$

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current D2a — D2e D2a — D2e	—	—	200 250	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-58	-40	-27	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS**CERPACK**

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

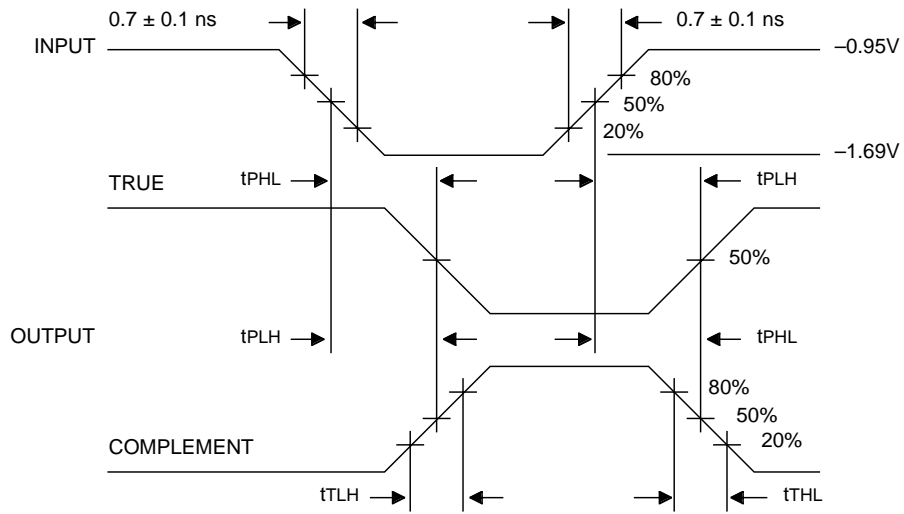
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PH2}	Propagation Delay D2a — D2e to O, \bar{O}	200	1100	200	1150	200	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay D1a — D1e to O, \bar{O}	200	1000	200	950	200	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay Data to F	300	1525	300	1525	300	1525	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PH2}	Propagation Delay D2a — D2e to O, \bar{O}	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay D1a — D1e to O, \bar{O}	300	900	300	900	300	930	ps	
t _{PLH} t _{PHL}	Propagation Delay Data to F	300	1425	300	1425	300	1425	ps	
t _{TLH} t _{THL}	Transition Time 3 20% to 80%, 80% to 20%	00	900	300	900	300	900	ps	

TIMING DIAGRAM

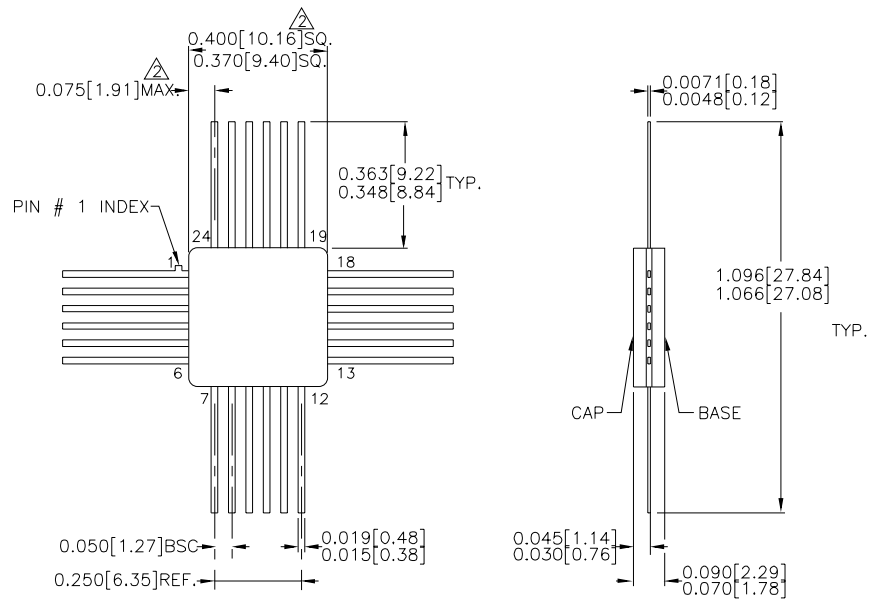


Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

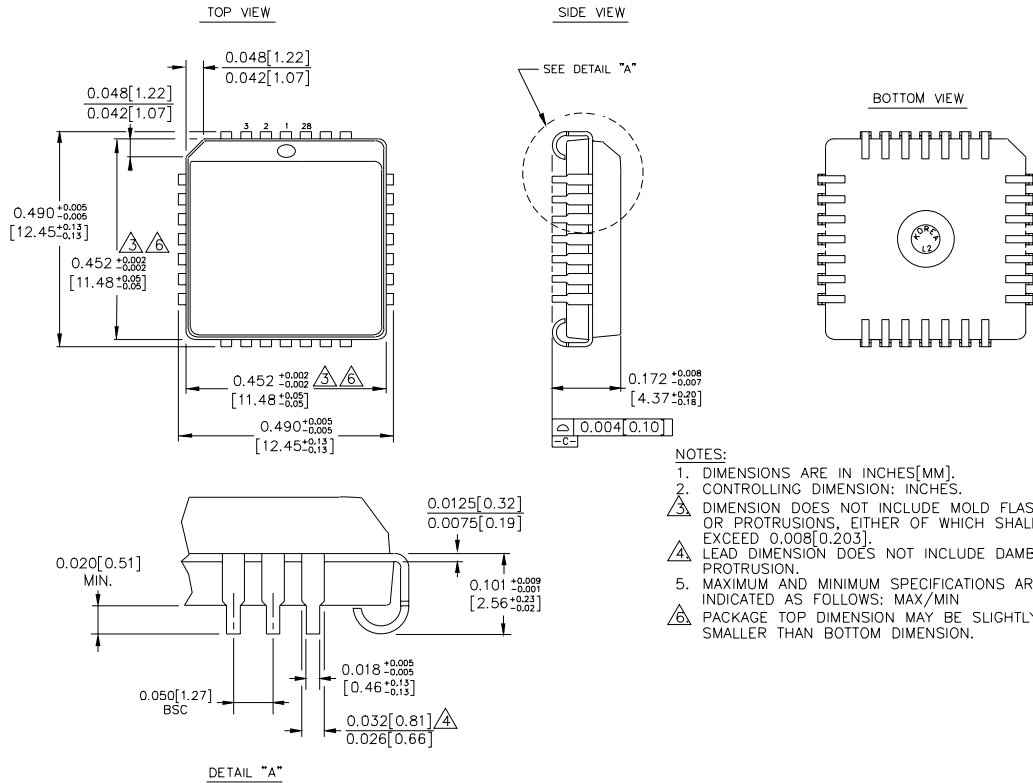
24-PIN CERPACK (F24-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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