

# MM54HC164/MM74HC164 8-Bit Serial-in/Parallel-out Shift Register

## General Description

The MM54HC164/MM74HC164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

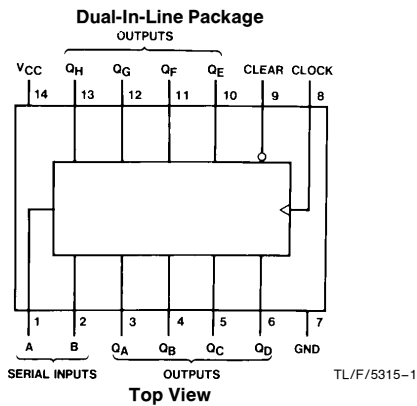
This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1  $\mu$ A maximum
- Low quiescent supply current: 80  $\mu$ A maximum (74HC Series)
- Fanout of 10 LS-TTL loads

## Connection and Logic Diagrams

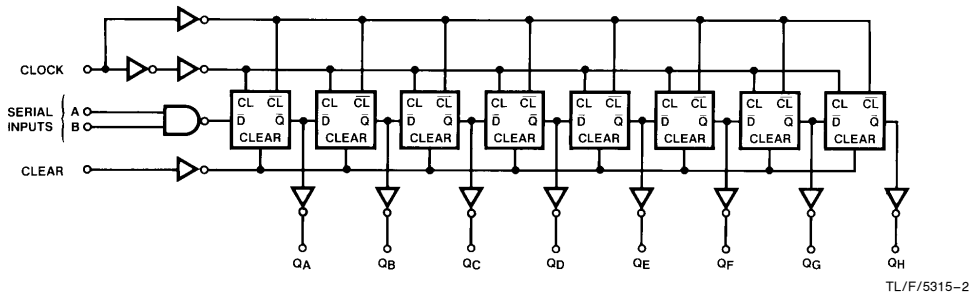


## Truth Table

Inputs		Outputs				
Clear	Clock	A	B	Q <sub>A</sub>	Q <sub>B</sub>	... Q <sub>H</sub>
L	X	X	X	L	L	L
H	L	X	X	Q <sub>AO</sub>	Q <sub>BO</sub>	Q <sub>HO</sub>
H	↑	H	H	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	↑	X	L	L	Q <sub>An</sub>	Q <sub>Gn</sub>

H = High Level (steady state), L = Low Level (steady state)  
 X = Irrelevant (any input, including transitions)  
 ↑ = Transition from low to high level.  
 Q<sub>AO</sub>, Q<sub>BO</sub>, Q<sub>HO</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady state input conditions were established.  
 Q<sub>An</sub>, Q<sub>Gn</sub> = The level of Q<sub>A</sub> or Q<sub>G</sub> before the most recent ↑ transition of the clock; indicated a one-bit shift.

## Order Number MM54HC164 or MM74HC164



MM54HC164/MM74HC164 8-Bit Serial-in/Parallel-out Shift Register

## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				74HC $T_A = -40$ to $85^\circ C$		54HC $T_A = -55$ to $125^\circ C$		
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

### AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

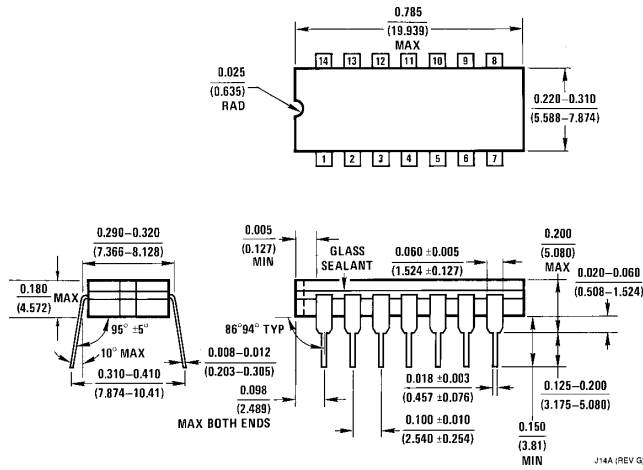
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency			30	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Output		19	30	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clear to Output		23	35	ns
$t_{REM}$	Minimum Removal Time, Clear to Clock		-2	0	ns
$t_S$	Minimum Setup Time Data to Clock		12	20	ns
$t_H$	Minimum Hold Time Clock to Data		1	5	ns
$t_W$	Minimum Pulse Width Clear or Clock		10	16	ns

### AC Electrical Characteristics $C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

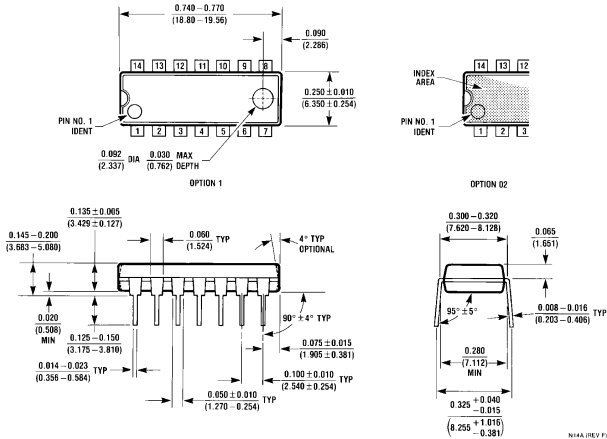
Symbol	Parameter	Conditions	$V_{CC}$	$T_A=25^{\circ}C$			74HC $T_A=-40\text{ to }85^{\circ}C$		54HC $T_A=-55\text{ to }125^{\circ}C$		Units
				Typ	Guaranteed Limits		Guaranteed Limits		Guaranteed Limits		
$f_{MAX}$	Maximum Operating Frequency		2.0V		5	4	3	MHz			
			4.5V		27	21	18	MHz			
			6.0V		31	24	20	MHz			
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Output		2.0V	115	175	218	254	ns			
			4.5V	13	35	44	51	ns			
			6.0V	20	30	38	44	ns			
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clear to Output		2.0V	140	205	256	297	ns			
			4.5V	28	41	51	59	ns			
			6.0V	24	35	44	51	ns			
$t_{REM}$	Minimum Removal Time Clear to Clock		2.0V	-7	0	0	0	ns			
			4.5V	-3	0	0	0	ns			
			6.0V	-2	0	0	0	ns			
$t_S$	Minimum Setup Time Data to Clock		2.0V	25	100	125	150	ns			
			4.5V	14	20	25	30	ns			
			6.0V	12	17	21	25	ns			
$t_H$	Minimum Hold Time Clock to Data		2.0V	-2	5	5	5	ns			
			4.5V	0	5	5	5	ns			
			6.0V	1	5	5	5	ns			
$t_W$	Minimum Pulse Width Clear or Clock		2.0V	22	80	100	120	ns			
			4.5V	11	16	20	24	ns			
			6.0V	10	14	18	20	ns			
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time		2.0V		75	95	110	ns			
			4.5V		15	19	22	ns			
			6.0V		13	16	19	ns			
$t_r, t_f$	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns			
			4.5V		500	500	500	ns			
			6.0V		400	400	400	ns			
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per package)	5.0V	150				pF			
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF			

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## Physical Dimensions inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54HC164J or MM74HC164J**  
**NS Package Number J14A**



**Molded Dual-In-Line Package (N)**  
**Order Number MM74HC164N**  
**NS Package Number N14A**

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