National Semiconductor

September 2002

CLC5526
Digital Variable Gain Amplifier (DVGA)

General Description

The CLC5526 is a high performance, digitally controlled, variable-gain amplifier (DVGA). It has been designed for use in a broad range of mixed signal and digital communication applications such as mobile radio, cellular base stations and back-channel modems where automatic-gain-control (AGC) is required to increase system dynamic range.

The CLC5526 has differential input and output, allowing large signal swings on a single 5V rail. The input impedance is 200Ω. The differential output impedance is 600Ω and is designed to drive a 1 kΩ differential load. The output amplifier has excellent intermodulation performance. The CLC5526 is designed to accept signals from RF elements and maintain a terminated impedance environment.

The CLC5526 maintains a 350 MHz bandwidth over its entire gain and attenuation range from +30 dB to −12 dB. Internal clamping ensures very fast overdrive recovery. Two tone intermodulation distortion is excellent: at 150 MHz, 1 V_{pp} it is −64 dBc.

Input signals to the CLC5526 are scaled by an accurate, differential R-2R resistive ladder with an input impedance of 200Ω. A scaled version of the input is selected under digital control and passed to the internal amplifier. The input common mode level is set at 2.4V via a bandgap referenced bias generator which can be overridden by an external input.

Following the resistive ladder is a fixed, 30 dB gain amplifier. The output stage common mode voltage of the CLC5526 is set to 3V, by internal, positive supply connected resistors.

Digital control of the CLC5526 is accomplished by a 3-bit parallel gain control input and a data valid pin to latch the data. If the data is not latched, the DVGA is transparent to gain control updates. All digital inputs are TTL/CMOS compatible.

A shutdown input reduces the CLC5526 supply currrent to a few mA. During shutdown, the input termination is maintained and current attenuation settings are held.

The CLC5526 operates over the industrial temperature range of −40˚C to +85˚C. The part is available in a 20-pin SSOP package.

Features

- 350 MHz bandwidth
- Differential input and output
- Gain control: parallel w/data latching
- Supply voltage: +5V
- Supply current: 48 mA

Key Specifications

- Low two tone intermod:
  distortion: −64 dBc @ 1 V_{PP}, 150 MHz
  24.5 dBm IP3, 150 MHz
- Low noise: 2.5 nV/√Hz (max gain),
  9.3 dB noise figure (max gain)
- Wide gain range: +30 dB to −12 dB
- Gain step size: 6 dB

Applications

- Cellular/PCS base stations
- IF sampling receivers
- Infrared/CCD imaging
- Back-channel modems
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

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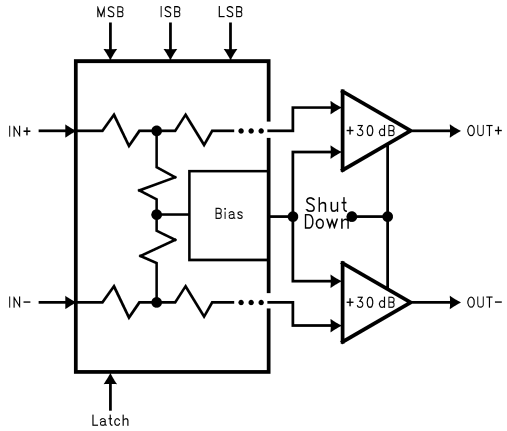
Block Diagram



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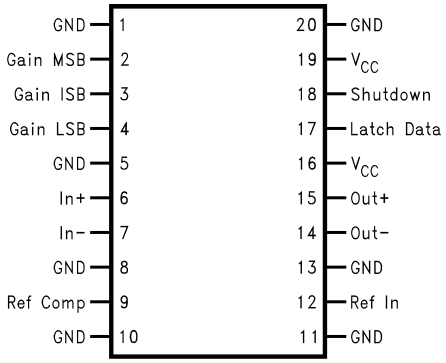
Pin Configuration



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Ordering Information

CLC5526MSA	20-Pin SSOP
CLC5526PCASM	Evaluation Board

Pin Descriptions

Pin Name	Pin No.	Description
GND	1, 5, 8, 10, 11, 13, 20	Circuit ground.
Gain MSB	2	Gain Selection Most Significant Bit
Gain ISB	3	Gain Selection Data Bit
Gain LSB	4	Gain Selection Least Significant Bit
In+	6	Positive Differential Input
In–	7	Negative Differential Input
Ref Comp	9	Reference Compensation
V_{CC}	16, 19	Positive Supply Voltage
Shutdown	18	Low Power Standby Control (Active High)
Latch Data	17	Data Latch Control (Active High)
Out+	15	Positive Differential Output
Out–	14	Negative Differential Output
Ref In	12	External Reference Input

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage (V_{CC})	−0.5V to +6V
Differential Voltage between any Two Grounds	<200 mV
Analog Input Voltage Range	−0.5V to +V_{CC}
Digital Input Voltage Range	−0.5V to +V_{CC}
Output Short Circuit Duration (one-pin to ground)	Infinite
Junction Temperature	150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec

Recommended Operating Conditions

Positive Supply Voltage (V_{CC})	+5V ±5%
Differential Voltage between any Two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	±0.5V
Operating Temperature Range	−40˚C to +85˚C

Package Thermal Resistance

Package	(θ_{JA})	(θ_{JC})
20-Pin SSOP	90˚C/W	38˚C/W

Reliability Information

Transistor Count	300

Electrical Characteristics

The following specifications apply for V_{CC} = +5V, R_L = 1 kΩ maximum gain setting. **Boldface limits apply for T_A = T_{min} = −40˚C to T_{max} = +85˚C,** all other limits T_A = 25˚C (Notes 2, 3, 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
BW	Small-Signal Bandwidth			350		MHz
NOISE AND DISTORTION						
	2nd Harmonic Distortion	f_{IN} = 150 MHz, 1 V_{PP}	53	67		dBc
		f_{IN} = 250 MHz, 1 V_{PP}		64		dBc
		f_{IN} = 150 MHz, 2 V_{PP}	43	62		dBc
		f_{IN} = 250 MHz, 2 V_{PP}		58		dBc
	3rd Harmonic Distortion	f_{IN} = 150 MHz, 1 V_{PP}	53	71		dBc
		f_{IN} = 250 MHz, 1 V_{PP}		70		dBc
		f_{IN} = 150 MHz, 2 V_{PP}	43	57		dBc
		f_{IN} = 250 MHz, 2 V_{PP}		56		dBc
IMD	Two Tone Intermodulation Distortion	f_1 = 149.9 MHz, f_2 = 150.1 MHz, 1 V_{PP} Composite		64		dBc
		f_1 = 149.9 MHz, f_2 = 150.1 MHz, 2 V_{PP} Composite		61		dBc
		f_1 = 249.9 MHz, f_2 = 250.1 MHz, 1 V_{PP} Composite		63		dBc
		f_1 = 249.9 MHz, f_2 = 250.1 MHz, 2 V_{PP} Composite		54		dBc
	Two Tone, 3rd Order Intermodulation	150 MHz		24.5		dBm
	Thermal Noise	Minimum Gain Setting		2.2		nV/√Hz
		Maximum Gain Setting		2.5		nV/√Hz
	Noise Figure	Maximum Gain Setting		9.3		dB
ANALOG I/O						
	Differential Input Impedance			200		Ω
	Differential Output Impedance			600		Ω
	Input Signal Level (AC Coupled)	Maximum Gain		126		mV
	Maximum Input Signal Level	Recommended		6		V_{PP}
	Maximum Output Signal Level	Recommended		4		V_{PP}
	Output Clipping			8		V_{PP}
GAIN PARAMETERS						

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5V, R_L = 1 kΩ maximum gain setting. **Boldface limits apply for $T_A = T_{min}$ = –40˚C to T_{max} = +85˚C,** all other limits T_A = 25˚C (Notes 2, 3, 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Maximum Gain			30		dB
	Minimum Gain			–12		dB
	Gain Step Size			6.02		dB
	Gain Step Accuracy	(1 sigma)		0.03		dB
	Cumulative Gain Step Error	(1 sigma)		0.085		dB
DIGITAL INPUTS/TIMING						
	Logic Compatibility			TTL/CMOS		V
V_{IL}	Logic Input Low Voltage				**0.8**	V
V_{IH}	Logic Input High Voltage		**2.0**			V
T_{SU}	Setup Time			3		ns
T_{HOLD}	Hold Time			3		ns
T_{PW}	Minimum Pulse Width			3		ns
POWER REQUIREMENTS						
I_{CC}	+5V Supply Current			48	60	mA
	Shutdown			9		mA

Note 1: "Absolute Maximum Ratings" are limited values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

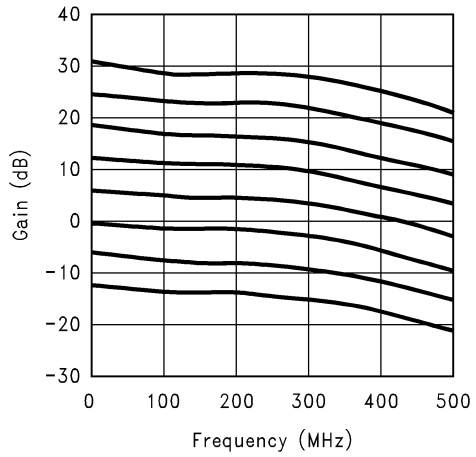
Note 2: Limits are 100% tested at 25˚C.

Note 3: Typical specifications are the mean values of the distributions of deliverable amplifiers tested to date.

Note 4: Outgoing quality levels are determined from tested parameters.

Typical Performance Characteristics (V_{CC} = +5V, R_L = 1 kΩ, max gain; unless specified)

Gain vs. Frequency



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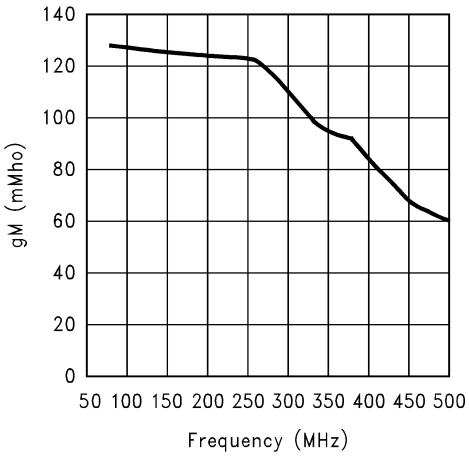
Transconductance vs. Frequency



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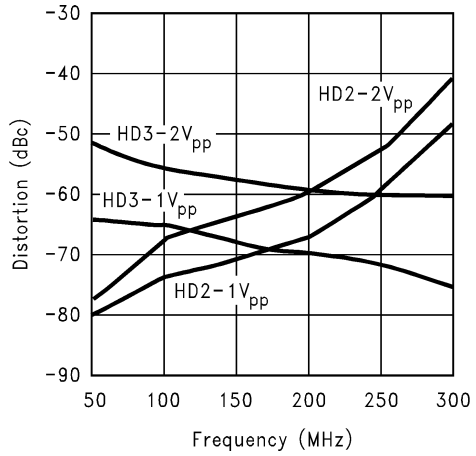
2nd and 3rd Harmonic Distortion vs. Frequency



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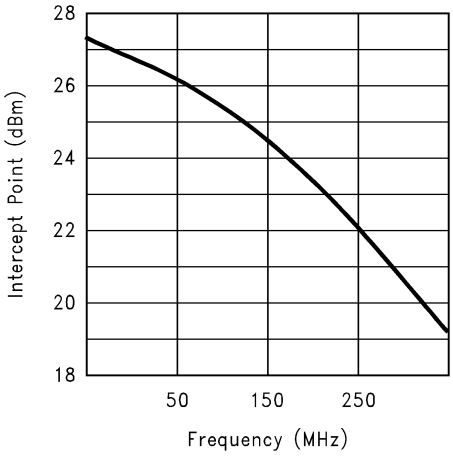
2-Tone, 3rd Order Intermodulation Output Intercept vs Frequency



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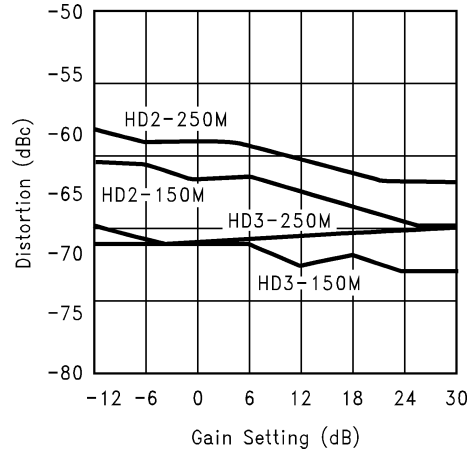
Distortion vs. Gain Setting



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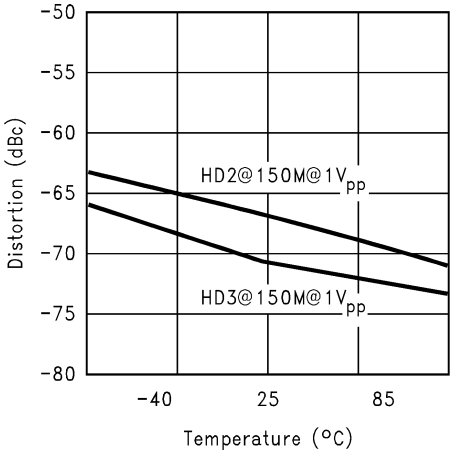
Distortion vs. Temperature



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Typical Performance Characteristics (V_{CC} = +5V, R_L = 1 kΩ, max gain; unless specified)
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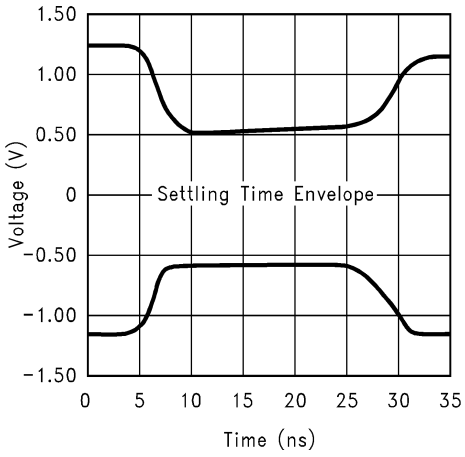
6dB Gain Step, Time Domain Response



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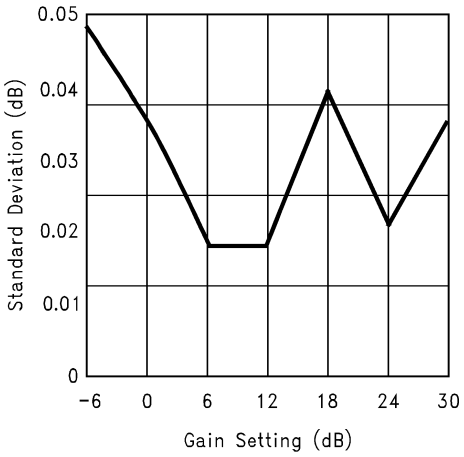
Gain Step Error Deviation vs. Gain Setting



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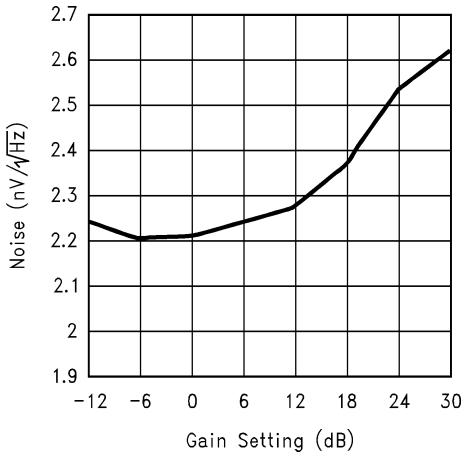
Input Referred Thermal Noise vs. Gain Setting (Gain Block)



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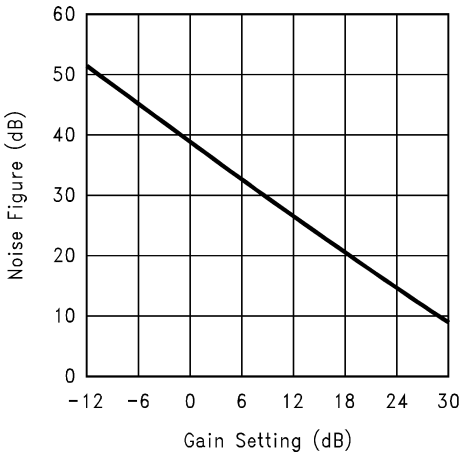
Noise Figure vs. Gain Setting



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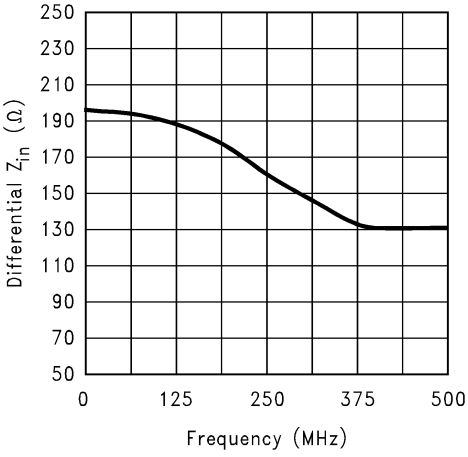
Differential Z_{IN} vs. Frequency



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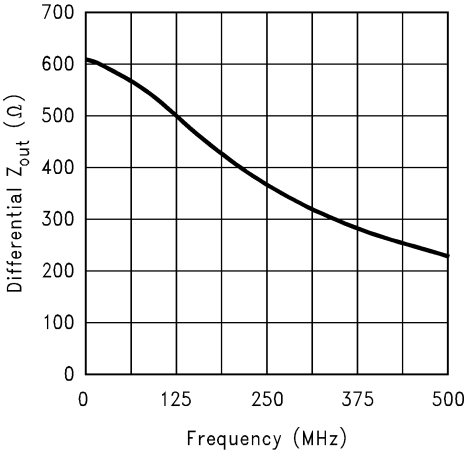
Differential Z_{OUT} vs. Frequency



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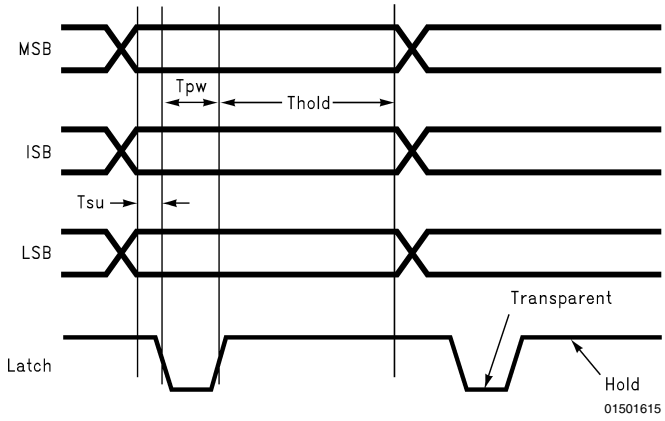
Timing Diagram



Truth Table

Gain Word	MSB	ISB	LSB	Gain (dB)
0	0	0	0	–12
1	0	0	1	–6
2	0	1	0	0
3	0	1	1	+6
4	1	0	0	+12
5	1	0	1	+18
6	1	1	0	+24
7	1	1	1	+30

Applications

DESCRIPTION

The CLC5526 is a digitally programmable, variable gain amplifier with the following features:

- 8 gain settings ranging from –12 to +30 dB in 6dB steps
- Differential inputs and outputs (externally AC coupled)
- Self biased input common-mode voltage
- 3-bit parallel digital control
- Single +5V supply
- Low-Power standby mode

Please refer to *Figure 1* for a representative block diagram.

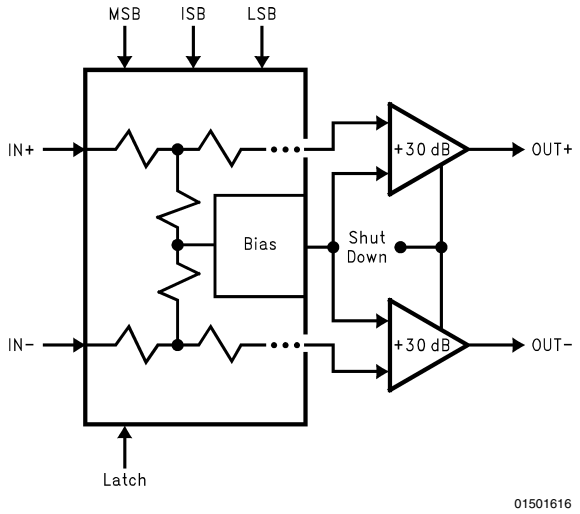


FIGURE 1. CLC5526 Block Diagram

GAIN SELECTION

Gain levels can be decreased from the maximum value in –6dB steps via the 3-bit digital inputs. *Table 1* shows the gain selection truth table for a 1000Ω differential load.

TABLE 1. Gain Selection Truth Table

Gain Word	MSB	ISB	LSB	Gain (dB)
0	0	0	0	–12
1	0	0	1	–6
2	0	1	0	0
3	0	1	1	+6
4	1	0	0	+12
5	1	0	1	+18
6	1	1	0	+24
7	1	1	1	+30

Gain settings can be calculated as follows:

GAIN = –12 dB + (Gain Word) * 6.02 dB

Gain selection has two modes: Transparent or latched, depending on the LATCH input. If the LATCH input is held LOW, then the device is in the transparent mode. Changes on data inputs will result in direct changes to the gain setting. Input data will be latched upon the LOW to HIGH transition of LATCH. While LATCH is HIGH, digital data will be ignored until LATCH is strobed low again.

Note: Upon power-up the analog inputs are disconnected from the internal amplifier. LATCH will need to be strobed LOW before an analog output will be present!

DIFFERENTIAL I/O CONSIDERATIONS

Analog inputs and outputs need to be AC coupled to prevent DC loading of the common-mode voltages. If driving the CLC5526 from a single-ended 50Ω source is required, a 1:2 transformer should be used to generate the differential inputs. As the differential input impedance of the CLC5526 is 200Ω, the 1:4 impedance ratio will allow for optimum matching to the 50Ω source. The secondary outputs of the transformer should be AC coupled to the CLC5526 analog inputs, while the secondary center tap of the transformer should be directly connected to the system ground.

The CLC5526 is designed to drive differential circuits, such as the CLC5957 Analog to Digital convertor. *Figure 2* below shows a typical application of the CLC5526.

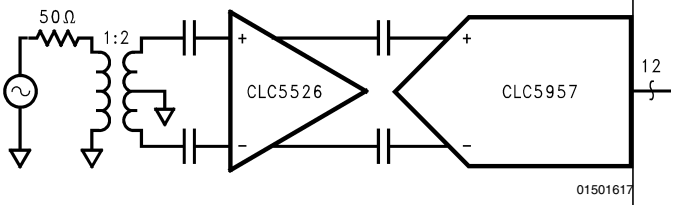


FIGURE 2. Differential I/O Connections

DRIVING LOADS

Actual gain of the CLC5526 will vary with the output load. The device is designed to provide +30 dB maximum gain with a 1000Ω differential load.

Each output of the CLC5526 contains an internal 300Ω resistor to the V_{CC} rail. Actual gain calculations need to take this in account with a given external load resistor. The effective load resistance can be used with the following equation to calculate max gain values.

$A_V = 20 \log (0.0843 * R_{leff})$

Where: $R_{leff} = R_{int} \parallel R_{ext(diff)}$

$R_{int} = 600\Omega$ differential

Chart 1 shows maximum gain values over output load. Resistor values are for differential loads.

Applications (Continued)

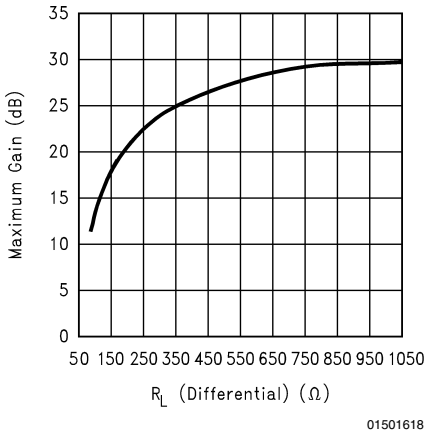


Chart 1: Maximum Gain vs R_{LOAD}

Stray capacitance at the output, along with the output load value will form a pole, which can degrade the CLC5526 bandwidth. For a narrow-band application this problem can be alleviated by using a tuned load, which will incorporate any stray parasitic impedance into a resonant circuit. By tuning the resonant load, full gain can be achieved with a given resistive load.

A typical tuned load is shown below in *Figure 3*, where the resonant frequency is tuned about 150 MHz.

The 1000Ω load in this circuit can represent the input impedance of the CLC5957 Analog to Digital converter. Actual values for the reactive components may vary slightly to account for board and device parasitic elements.

The Diversity Receiver Chipset may also use the ADC12L066 A/D converter in place of the CLC5957. Please refer to the Low Power Diversity Receiver Chipset (LDRCS) User's Guide for input matching between the CLC5526 and ADC12L066.

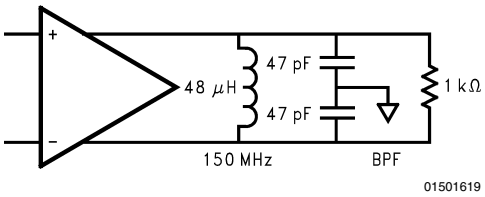


FIGURE 3. CLC5526 Driving a Tuned Load

Typical Application

Although the CLC5526 can be used as a general purpose digital variable gain amplifier, it was specifically designed to provide the variable gain function in National's Diversity Receiver Chipset. In this application, the CLC5526 drives a tuned BPF and the CLC5957 Analog to Digital converter. Digitized IF data is downsampled and tuned with the CLC5903 dual digital tuner which also provides the AGC control function. AGC data is fed back to the CLC5526. The CLC5957 differential input impedance is 1000Ω, so with the tuned load, full gain of the CLC5526 is achieved. *Figure 4* shows the block diagram of the Diversity Receiver Chipset application. *Figure 5* shows the SINAD vs Input Power of the diversity receiver chipset. For input power levels ranging from 0 dB to −110 dB, the chip set provides a signal to noise ratio in excess of the 9 dB required for a typical GSM system.

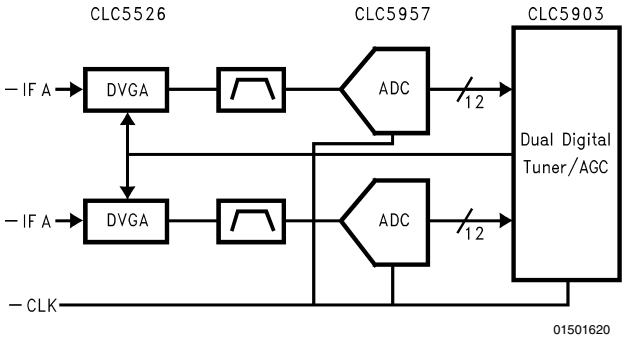


FIGURE 4. Diversity Receiver Chipset Block Diagram

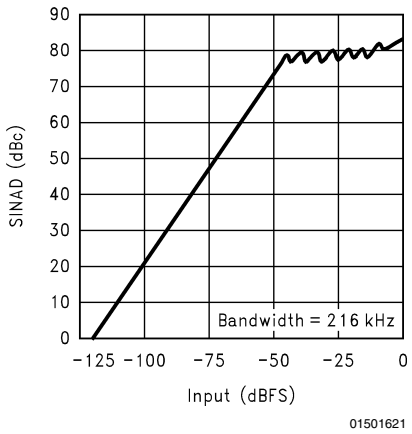


FIGURE 5. Diversity Receiver Chipset SINAD vs Input Power

Layout Considerations

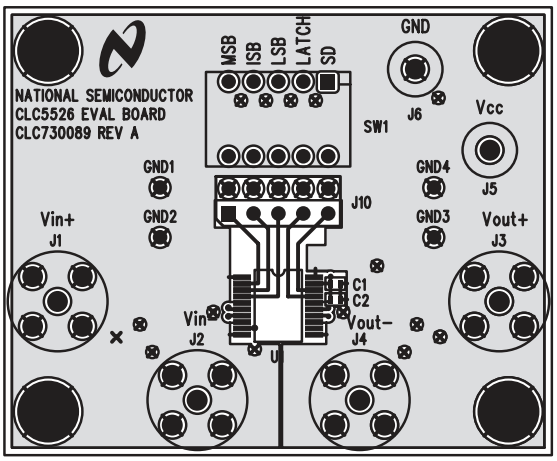
A proper printed circuit layout is essential for achieving high frequency performance. National Semiconductor provides evaluation boards for the CLC5526, which include input and output transformers for impedance matching and single to differential signal conversion.

Supply bypassing is required for best performance. Provide a 6.8 µF Tantalum and 0.1 µF ceramic capacitor as close as possible to the supply pin.

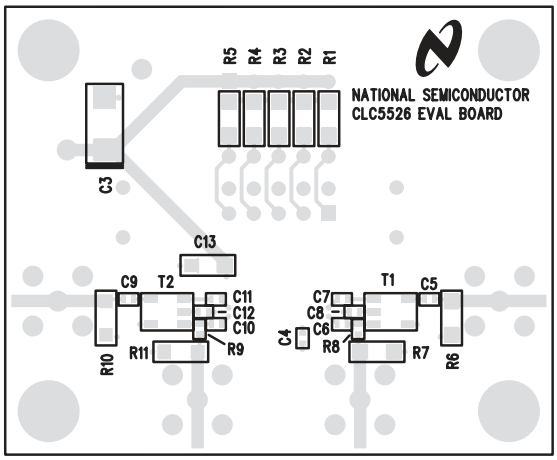
In addition, a 100 pF ceramic capacitor should be placed between the COMP pin (pin 9) and the system ground. This will filter high frequency noise from the common-mode level.

Ceramic coupling capacitors should be used to AC couple both the input and output. Actual values will depend upon the signal frequency.

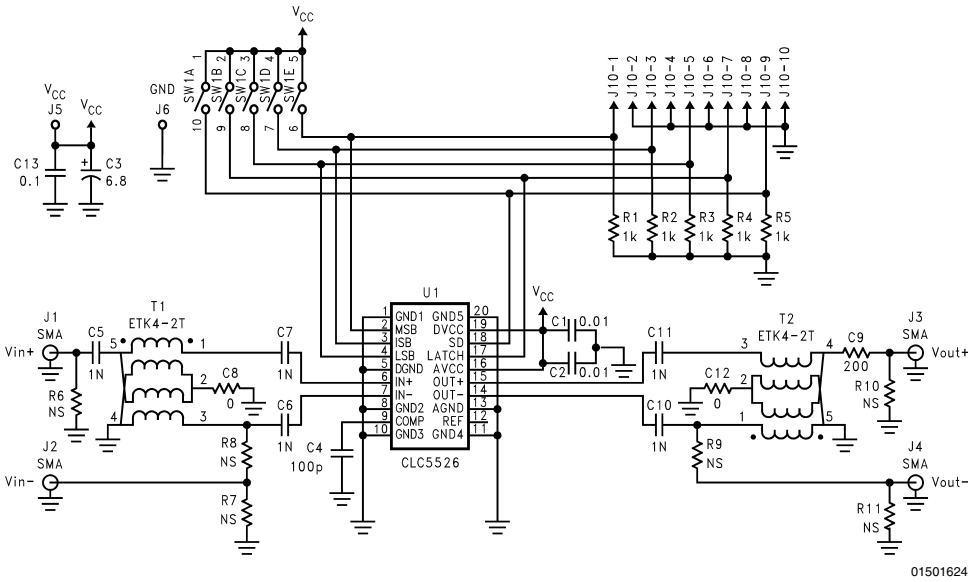
Evaluation Board Layout and Schematic Diagram



CLC5526 Layer 1



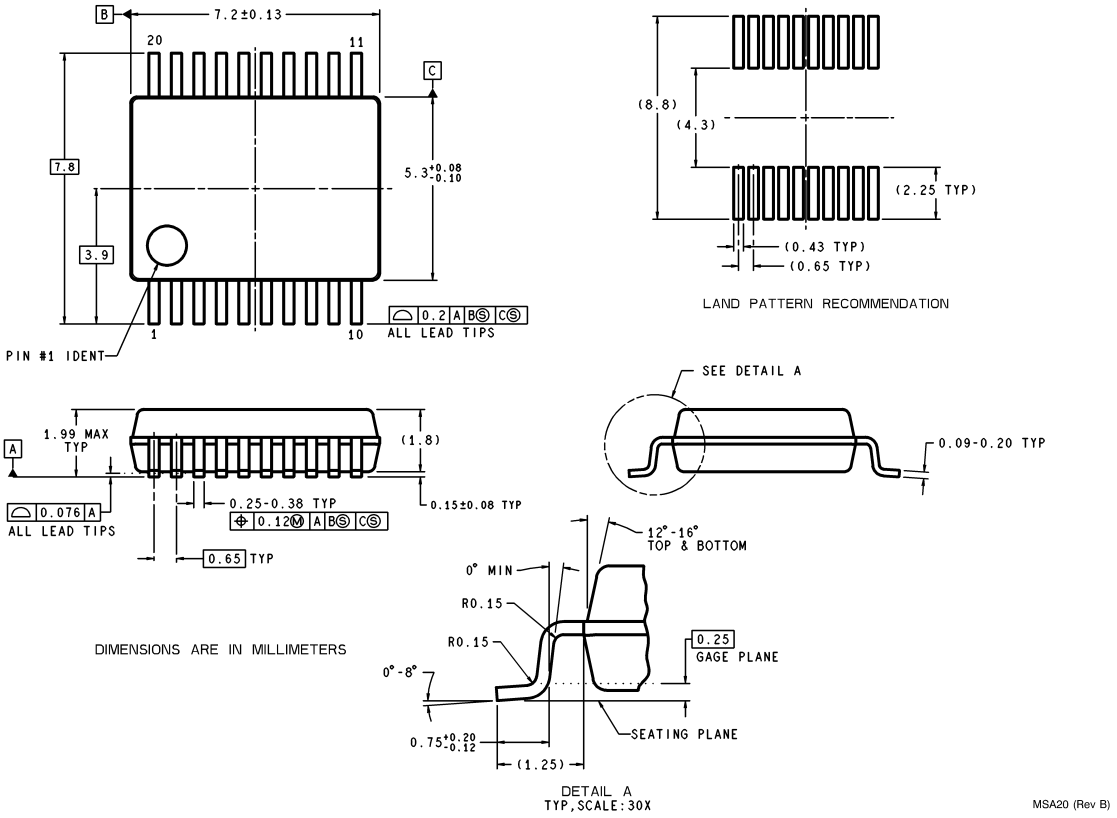
CLC5526 Layer 2



Evaluation Board Schematic

Physical Dimensions inches (millimeters)

unless otherwise noted



Millimeters only

20-Lead SSOP
NSC Package Number MSA20

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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