MC10134

Dual Multiplexer With Latch

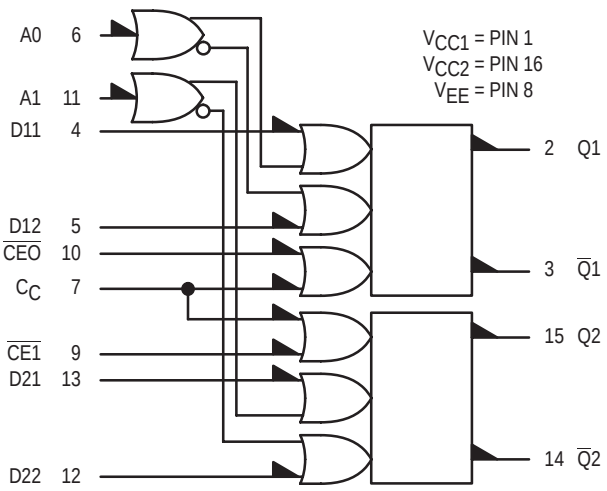
The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

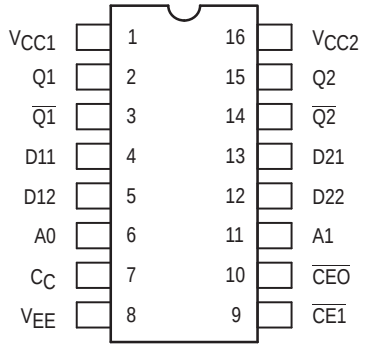
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

- P_D = 225 mW typ/pkg (No Load)
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT

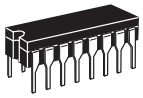


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

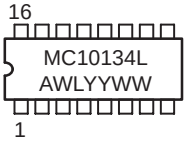
ON Semiconductor

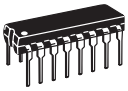
http://onsemi.com

MARKING DIAGRAMS

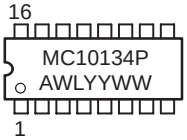


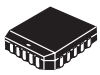
CDIP–16
L SUFFIX
CASE 620



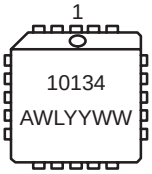


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Q_n

$C = \overline{C}_E + C_C$

ORDERING INFORMATION

Device	Package	Shipping
MC10134L	CDIP–16	25 Units / Rail
MC10134P	PDIP–16	25 Units / Rail
MC10134FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		60			55		60	mAdc
Input Current	I_{inH}	4 5 6 7 10		460 460 425 460 425			290 290 265 290 265		290 290 265 290 265	µAdc
	I_{inL}	4*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 2	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 2	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 2		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data	t_{4+2+}	2	1.0	3.5	1.0		3.3	1.0	3.6	
Clock	t_{10-2+}	2	1.0	6.0	1.0		5.7	1.0	6.3	
Select	t_{6+2+}	2	1.0	4.8	1.0		4.6	1.0	5.0	
Setup Time Data	t_{setup}	2	2.5		2.5			2.5		
Select	t_{setup}	2	3.5		3.5			3.5		
Hold Time Data	t_{hold}	2	1.5		1.5			1.5		
Select	t_{hold}	2	1.0		1.0			1.0		
Rise Time (20 to 80%)	t_{2+}	2	1.5	3.7	1.5		3.5	1.5	3.8	
Fall Time (20 to 80%)	t_{2-}	2	1.5	3.7	1.5		3.5	1.5	3.8	

* All other inputs tested in the same manner.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4 5 6 7 10	4 5 6 7 10				8 8 8	1, 16 1, 16 1, 16
		I_{inL}	4*		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 2	4 5,6	6,7,10 7,10			8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 2	 6	4,6,7,10 5,7,10			8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 2	 6	6,7,10 7,10	4 5		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 2	 6	6,7,10 7,10		4 5	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			**+1.11 V**	**+0.31 V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Data	t_{4+2+}	2		6,7,10	4	2	8	1, 16
	Clock	t_{10-2+}	2	4	7	10	2	8	1, 16
	Select	t_{6+2+}	2	5	7,10	6	2	8	1, 16
Setup Time	Data	t_{setup}	2		6,7	4,10	2	8	1, 16
	Select	t_{setup}	2	5	7,11	6,10	2	8	1, 16
Hold Time	Data	t_{hold}	2		6,7	4,10	2	8	1, 16
	Select	t_{hold}	2	5	7,11	6,10	2	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2		6,7,10	4	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2		6,7,10	4	2	8	1, 16

* All other inputs tested in the same manner.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.