TelCom Semiconductor, Inc.

TC33025

High Speed Double-Ended PWM Controller

FEATURES

- **50nsec Propagation Delay to Outputs**
- **Dual High Current Totem Pole Outputs**
- **Wide Bandwidth Error Amplifier**
- **Fully–Latched Logic with Double Pulse Suppression**
- **Latching PWM for Cycle-By-Cycle Current Limiting**
- **Soft–Start Control with Latched Overcurrent Reset**
- **Input Undervoltage Lockout with Hysteresis**
- **Low Start–Up Current (500μA Typ)**
- **Internally Trimmed Reference with Undervoltage Lockout**
- **90% Maximum Duty Cycle (Externally Adjustable)**
- **Precision Trimmed Oscillator**
- **Voltage or Current Mode Operation to 1.0MHz**
- **Functionally Similar to the UC3825**

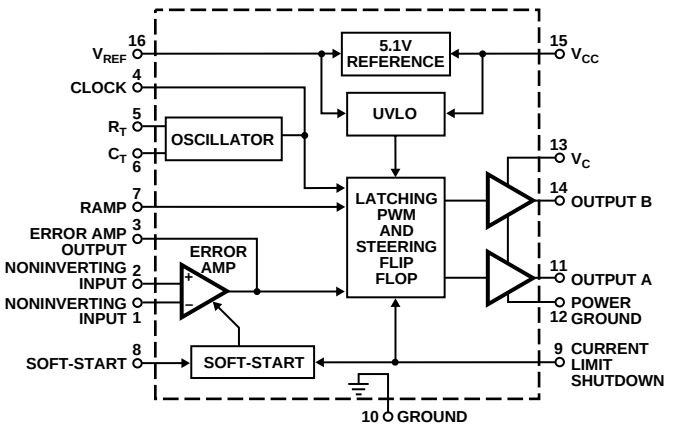
GENERAL DESCRIPTION

The TC33025 is a high speed, fixed frequency, double–ended pulse width modulator controller optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. This integrated circuit features an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering.

The flexibility of this device allows it to be easily configured for either current mode or voltage mode control.

FUNCTIONAL BLOCK DIAGRAM



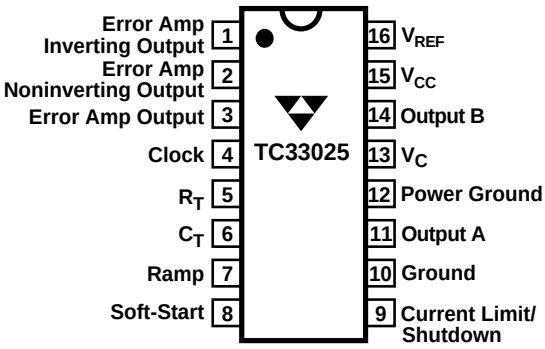
This device contains 227 active transistors.

ORDERING INFORMATION

Part Number	Package	Temperature Range
TC33025VPE	16-Pin PDIP	–40˚C to +80°C
TC33025VOE	16-Pin SOIC	–40˚C to +80°C

PIN CONFIGURATIONS

16-Pin SOIC/PDIP



TC33025

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage ..... V_{CC} = 30V
Output Driver Supply Voltage ..... V_C = 20V
Output Current, Source or Sink (Note 1)
DC ..... I_{OUT} = 0.5A
Pulsed (0.5µsec) ..... I_{OUT} = 2.0A
Current Sense, Soft–Start Ramp and
Error Amp Inputs ..... V_{IN} = –0.3 to 7.0V
Error Amp Output and Soft–Start Sink Current I_{OUT} = 10mA
Storage Temperature Range ..... –65°C to +150°C
Clock and R_T Output Current ..... I_{COUT}= 5.0mA
Power Dissipation and Thermal Characteristics
16-Pin SOIC
Maximum Power Dissipation
@ T_A = +25°C ..... P_D = 862mW
Thermal Resistance, Junction–to–Air ... θ_{JA} = 145˚C/W
16-Pin PDIP
Maximum Power Dissipation
@ T_A = +25°C ..... P_D = 1.25W
Thermal Resistance, Junction–to–Air ... θ_{JA} = 100˚C/W
Operating Junction Temperature ..... T_J = +150°C
Operating Ambient Temperature (Note 2)
TC33025 ..... T_A = –40 to +105°C
Storage Temperature Range ..... T_{STG} = –55 to +150 °C

*Static sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above thise listed under Absolute Maximum Power Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operation section of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{CC} = 15V, R_T = 3.65kΩ, C_T = 1.0nF, for typical values T_A = +25°C, for min/max values. T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Reference Section						
V_{REF}	Reference Output Voltage	I_{OUT} = 1.0mA, T_J = +25°C	5.05	5.1	5.15	V
REG_{LINE}	Line Regulation	V_{CC} = 10V to 30V	–	2.0	15	mV
REG_{LOAD}	Load Regulation	I_{OUT} = 1.0mA to 10mA	–	2.0	15	mV
T_S	Temperature Stability		–	0.2	–	mV/°C
V_{REF}	Total Output Variation Over Line, Load, and Temperature		4.95	–	5.25	V
V_N	Output Noise Voltage	f = 10Hz to 10kHz, T_J = +25°C	–	50	–	µV
S	Long Term Stability	T_A = +125°C for 1000 Hours	–	5.0	–	mV
ISC	Output Short Circuit Current		–30	–65	–100	mA
Oscillator Section						
f_{OSC}	Frequency	T_J = +25°C	380	400	420	kHz
	Line (V_{CC} = 10V to 30V) and Temperature ($T_A = T_{LOW}$ to T_{HIGH})		370	400	430	kHz
$\Delta f_{OSC}/\Delta V$	Frequency Change with Voltage	V_{CC} = 10V to 30V	–	0.2	1.0	%
$\Delta f_{OSC}/\Delta T$	Frequency Change with Temperature	$T_A = T_{LOW}$ to T_{HIGH}	–	2.0	–	%
V_P	Sawtooth Peak Voltage		2.6	2.8	3.0	V
V_V	Sawtooth Valley Voltage		0.7	1.0	1.25	V
V_{OH}	Clock Output Voltage High State		3.9	4.5	–	V
V_{OL}	Low State		–	2.3	2.9	V

Notes: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{LOW} = – 40°C for TC33025 T_{HIGH} = +105°C for TC33025

ELECTRICAL CHARACTERISTICS: V_{CC} = 15V, R_T = 3.65kΩ, C_T = 1.0nF, for typical values T_A = +25°C, for min/max values. T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Error Amplifier Section						
V_{IO}	Input Offset Voltage		–	–	15	mV
I_{IB}	Input Bias Current		–	0.6	3.0	µA
I_{IO}	Input Offset Current		–	0.1	1.0	µA
A_{VOL}	Open–Loop Voltage Gain	V_O = 1.0V to 4.0V	60	95	–	dB
GBW	Gain Bandwidth Product	T_J = +25°C	4.0	8.3	–	MHz
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 5.5V	75	95	–	dB
PSRR	Power Supply Rejection Ratio	V_{CC} = 10V to 30V	85	110	–	dB
I_{SOURCE} I_{SINK}	Output Current, Source Output Current, Sink	V_O = 4.0V V_O = 1.0V	0.5 1.0	3.0 3.6	– –	mA
V_{OH}	Output Voltage Swing, High State	I_O = – 0.5mA	4.5	4.75	5.0	V
V_{OL}	Output Voltage Swing, Low State	I_O = 1.0mA	0	0.4	1.0	
SR	Slew Rate		6.0	12	–	V/µsec
PWM Comparator Section						
I_{IB}	Ramp Input Bias Current		–	–0.5	–5.0	µA
DC_{MAX}	Duty Cycle, Maximum		80	90	–	%
DC_{MIN}	Duty Cycle, Minimum		–	–	0	
V_{TH}	Zero Duty Cycle Threshold	Voltage Pin 3(4) (Pin 7(9) = 0V)	1.1	1.25	1.4	V
$t_{PLH\ (in/out)}$	Propagation Delay	Ramp Input to Output, T_J = +25°C	–	60	100	nsec
Soft-Start Section						
I_{CHG}	Charge Current	V Soft–Start = 0.5V	3.0	9.0	20	µA
I_{DISCHG}	Discharge Current	V Soft–Start = 1.5V	1.0	4.0	–	mA
Current Sense Section						
I_{IB}	Input Bias Current	Pin 9 (12) = 0V to 4.0V	–	–	15	µA
V_{TH}	Current Limit Comparator Threshold		0.9	1.0	1.10	V
V_{TH}	Shutdown Comparator Threshold		1.25	1.40	1.55	
$t_{PLH\ (in/out)}$	Propagation Delay	Current Limit/Shutdown to Output, T_J = +25°C	–	50	80	nsec
Output Section						
V_{OL}	Output Voltage Low State	I_{SINK} = 20mA I_{SINK} = 200mA	– –	0.25 1.2	0.4 2.2	V
V_{OH}	Output Voltage High State	I_{SOURCE} = 20mA I_{SOURCE} = 200mA	13 12	13.5 13	– –	
$V_{OL\ (UVLO)}$	Output Voltage with UVLO Activated	V_{CC} = 6.0V, I_{SINK} = 0.5mA	–	0.25	1.0	V
I_L	Output Leakage Current	V_C = 20V	–	100	500	µA
t_R	Output Voltage Rise Time	C_L = 1.0nF, T_J = +25°C	–	30	60	nsec
t_F	Output Voltage Fall Time	C_L = 1.0nF, T_J = +25°C	–	30	60	nsec
Undervoltage Lockout Section						
$V_{TH\ (ON)}$	Start–Up Threshold	V_{CC} Increasing	8.8	9.2	9.6	V
V_H	UVLO Hysteresis Voltage	V_{CC} Decreasing After Turn–On	0.4	0.8	1.2	V
Total Device						
I_{CC}	Power Supply Current Start–Up Operating	 V_{CC} = 8.0V	 – –	 0.5 25	 1.2 35	mA

Notes: 1. Maximum package power dissipation limits must be observed.

2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{LOW} = – 40°C for TC33025 T_{HIGH} = +105°C for TC33025

TC33025

Pin No. DIP/SOIC	Symbol	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{REF}, however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency. Because this part is a push–pull output, each output runs at one–half the frequency set at this pin.
7	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft–Start	A capacitor at this pin sets the Soft–Start time.
9	Current Limit/Shutdown	This pin has two functions. First, it provides cycle–by–cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft–Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Output A	This is a high current totem pole output.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noiseon the control circuitry.
14	Output B	This is a high current totem pole output.
15	V_{CC}	This pin is the positive supply of the control IC.
16	V_{REF}	This is a 5.1V reference. It is usually connected to the noninverting input of the error amplifier.

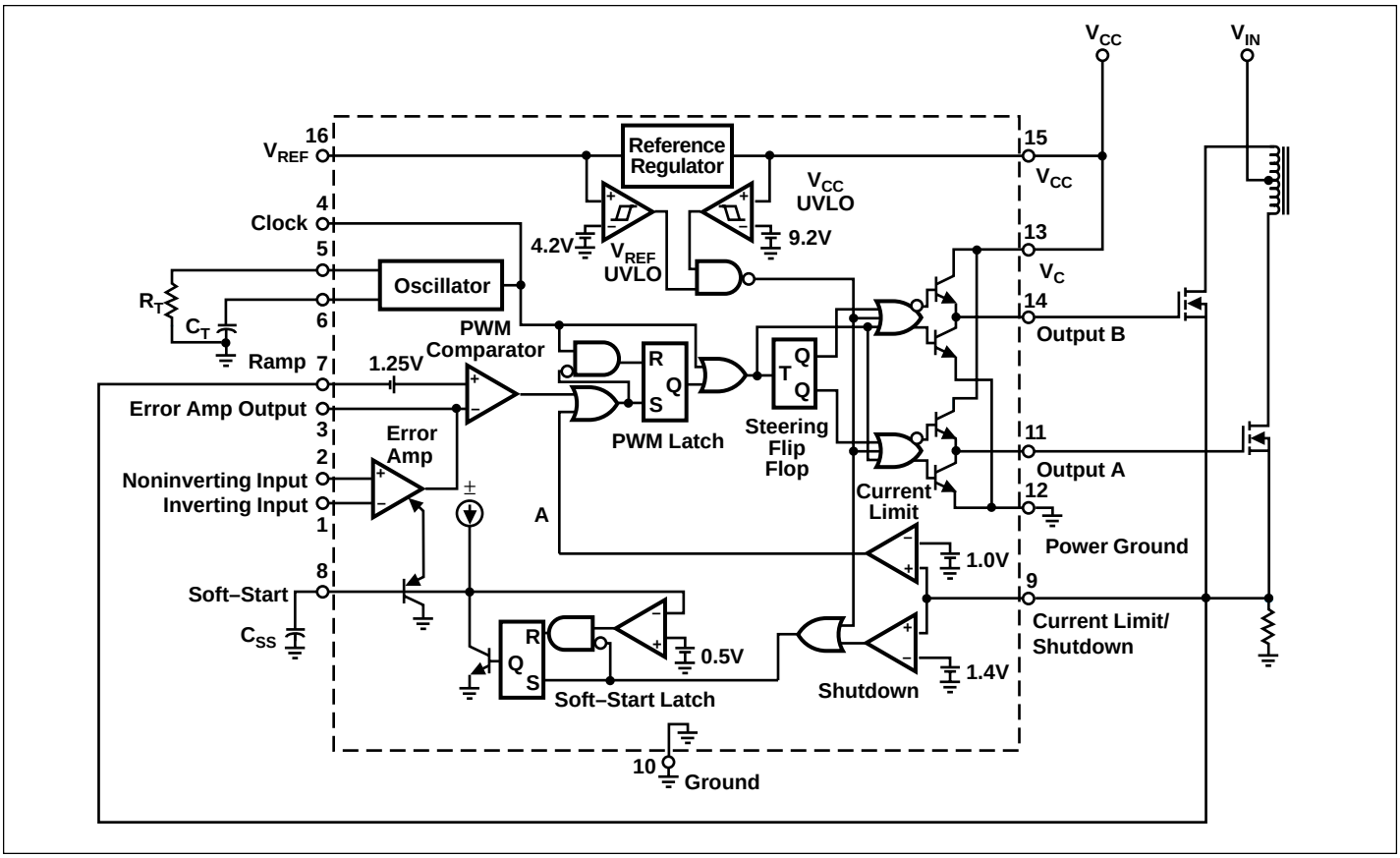


Figure 1. Representative Block Diagram

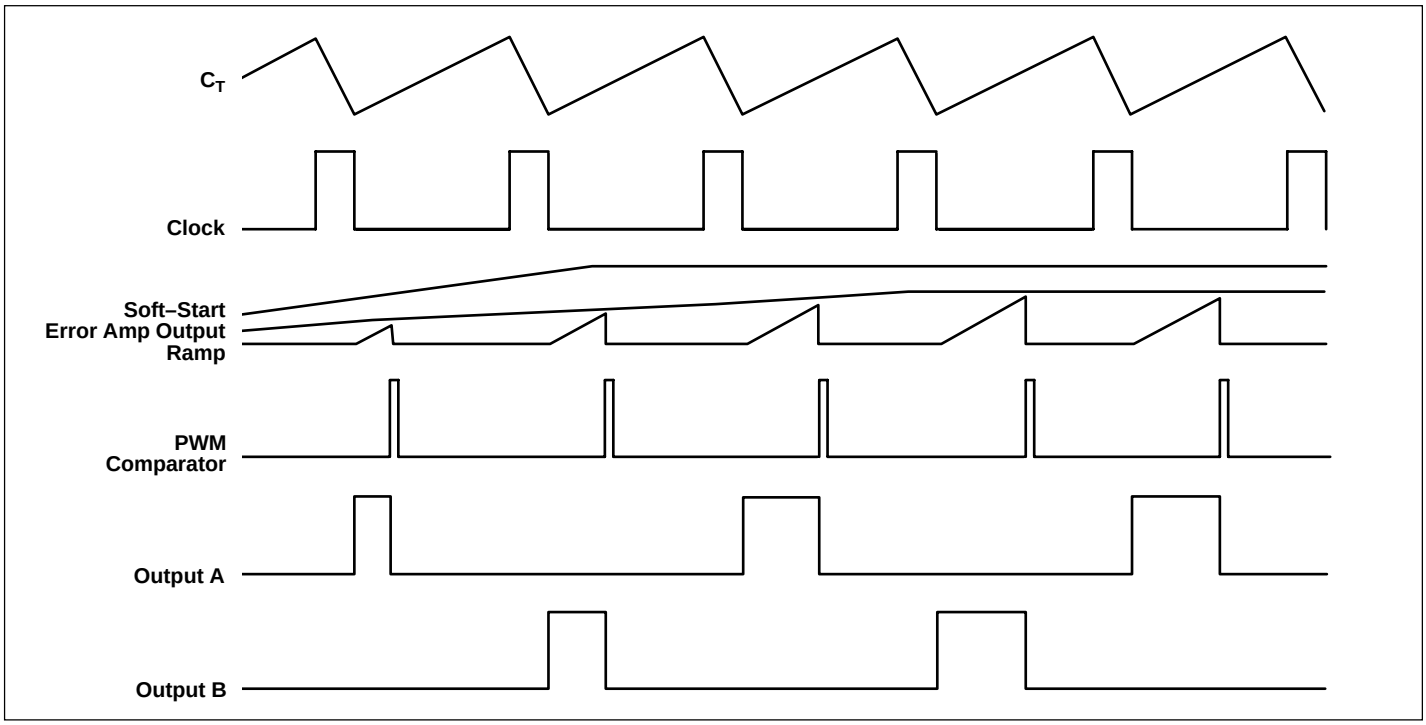


Figure 2. Current Limit Operating Waveforms

TC33025

OPERATING DESCRIPTION

The TC33025 is a high speed, fixed frequency, double–ended pulse width modulator controller optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 1.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0V. By selecting the value of R_T, the charge current is set through a current mirror for the timing capacitor C_T. This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8V and discharged to 1.0V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip–flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T as shown in Figure 6. This changes the charge to discharge ratio of C_T which is set internally to I_{CHARGE}/10 I_{CHARGE}. The new charge to discharge ratio will be:

$$\% \text{ Deadtime} = \frac{I_{ADDITIONAL} + I_{CHARGE}}{10\ (I_{CHARGE})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of C_T. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge C_T. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 13 and 14 provide suggested synchronization.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95dB and a gain bandwidth product of 8.3MHz with 75 degrees of phase margin (Figure 24). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a Common Mode Voltage (V_{CM}) input range of 1.5V to 5.5V. The Error Amplifier Output is provided for external loop compensation.

Soft–Start Latch

Soft–Start is accomplished in conjunction with an external capacitor. The soft start capacitor is charged by an internal 9.0μA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle.

The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5)\ C_{SOFT\text{-}START}$$

A Soft–Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft–Start circuit to latch so that the Soft–Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{REF}. The second condition is when current sense input exceeds 1.4V. Since this latch is “set dominant”, it cannot be reset until either of these signals is removed, and the voltage at $C_{SOFT–START}$ is less than 0.5V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25V offset such that whenever the voltage at this pin exceeds the Error Amplifier Output voltage minus 1.25V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

A toggle flip flop connected to the output of the PWM latch controls which output is active. The flip flop is pulsed by an OR gate that gets its inputs from the oscillator clock and the output of the PWM latch. A pulse from either one will cause the flip flop to enable the other output.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. When the voltage at this pin exceeds 1.0V, one of the comparators is activated. The output of this comparator sets the PWM latch, which disables the output. In this way cycle–by–cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{SENSE} = \frac{1.0V}{I_{PK\ (switch)}}$$

If the voltage at this pin exceeds 1.4V, the second comparator is activated. This comparator sets a latch which, in turn, causes the Soft–Start capacitor to be discharged. In this way a “hiccup” mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a “hiccup” mode is given by:

$$I_{SHUTDOWN} = \frac{1.4V}{R_{SENSE}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{REF}. During power–up, V_{CC} must exceed 9.2V and V_{REF} must exceed 4.2V before the outputs can be enabled and the Soft–Start latch released. If V_{CC} falls below 8.4V or V_{REF} falls below 3.6V, the outputs are disabled and the Soft–Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off–line bootstrap start–up circuit. Typical start–up current is 500µA.

Reference

A 5.1V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing or snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_E) is added to the on–time ramp (S_N) of the current–sense waveform, stability can be achieved (see Figure 3).

One must be careful not to add too much ramp compensation. If too much is added, the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figures 11 and 12 show examples of two different ways in which external ramp compensation can be implemented.

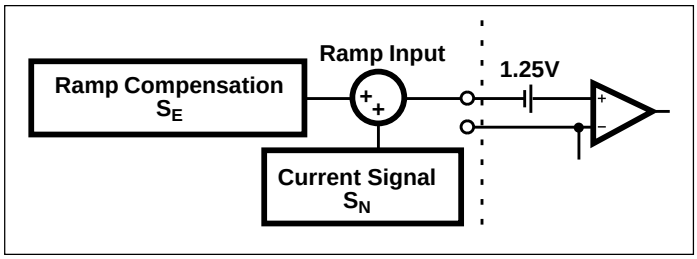


Figure 3. Ramp Compensation

A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 19 are also shown.

$$S_E = \frac{V_{OUT}}{L}\left(\frac{N_S}{N_P}\right)(R_S)A_I$$

where: V_{OUT} = DC output voltage
N_P, N_S = number of power transformer primary or secondary turns
A_I = gain of the current sense network (see Figures 8, 9 and 10)
L = output inductor
R_S = current sense resistance

For the application circuit:

$$S_E = \frac{5}{1.8\mu}\left(\frac{4}{16}\right)(0.3)(0.55)$$

$$= 0.115V/\mu sec$$

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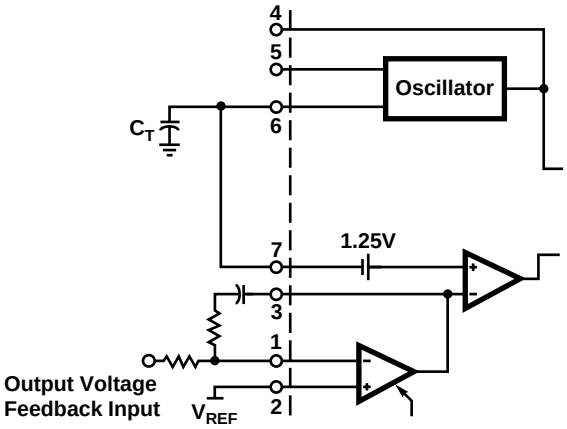
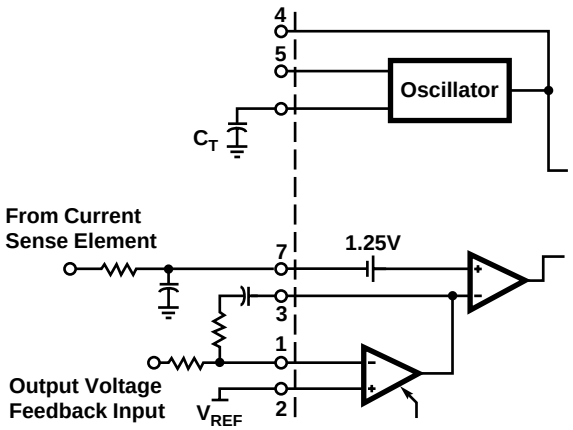


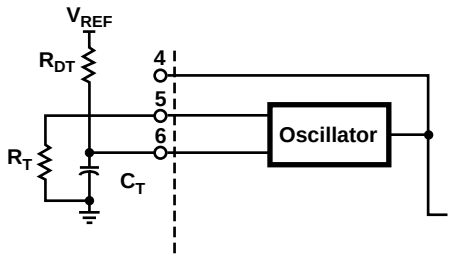
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25V to 4.05V.

Figure 4. Voltage Mode Operation



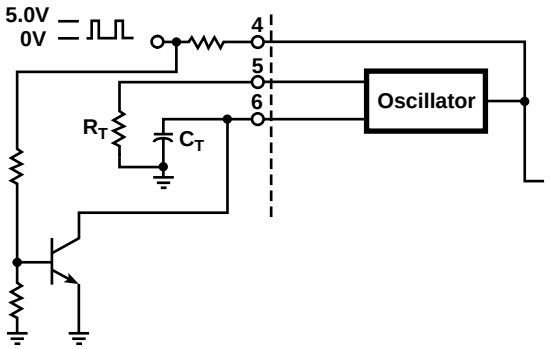
In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn—on of a power MOSFET.

Figure 5. Current Mode Operation



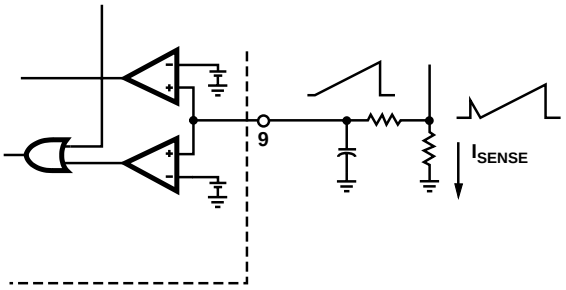
Additional dead time can be added by the addition of a dead time resistor from V_{REF} to C_T. See text on oscillator section for more information.

Figure 6. Dead Time Addition



The sync pulse fed into the clock pin must be at least 3.9V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

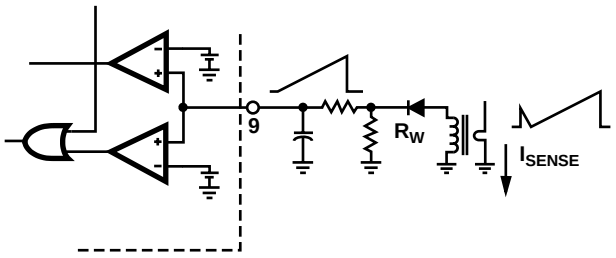
Figure 7. External Clock Synchronization



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_I = \frac{R_{SENSE}}{\text{turns ratio}}$$

Figure 8. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

$$A_I = \frac{R_W}{\text{turns ratio}}$$

Figure 9. Primary Side Current Sensing

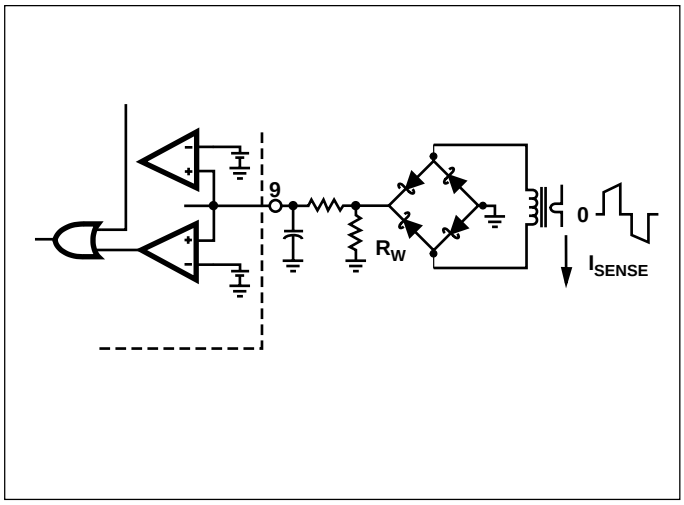
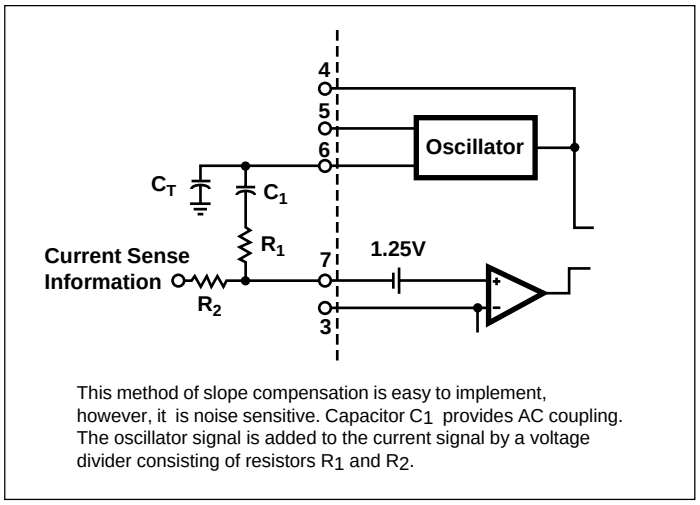
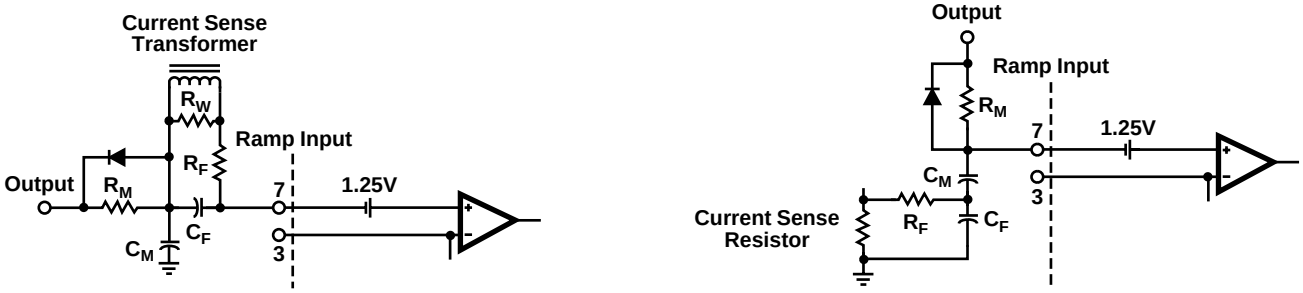


Figure 10. Primary or Secondary Side Current Sensing



This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 11. Slope Compensation (Noise Sensitive)



When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary . By choosing R_M and C_M with a larger time constant than the switching frequency, you can assumethat its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_E$. Then R_M can be calculated by $R_M = V_{CC}/I_M$.

Figure 12. Slope Compensation (Noise Immune)

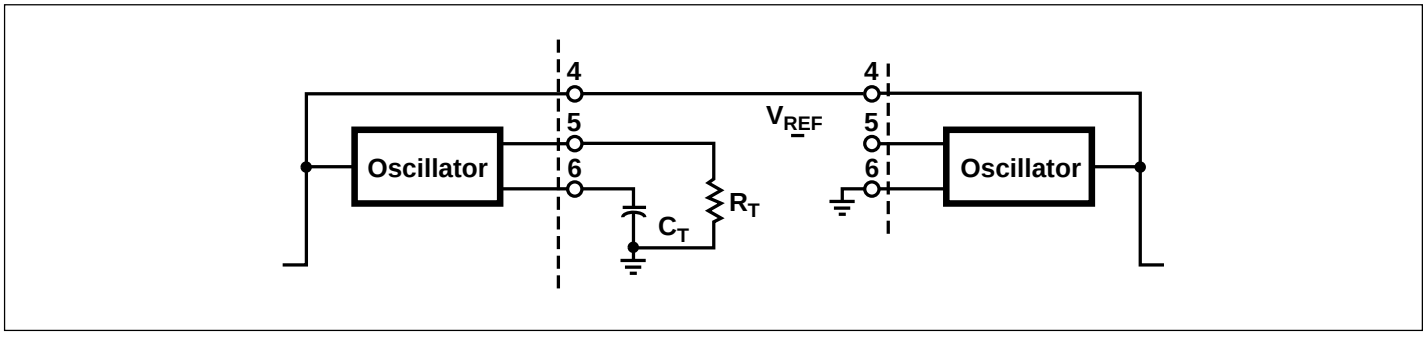


Figure 13. Current Mode Master/Slave Operation Over Short Distances

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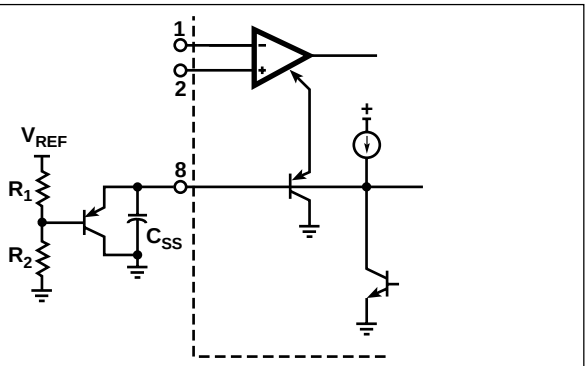
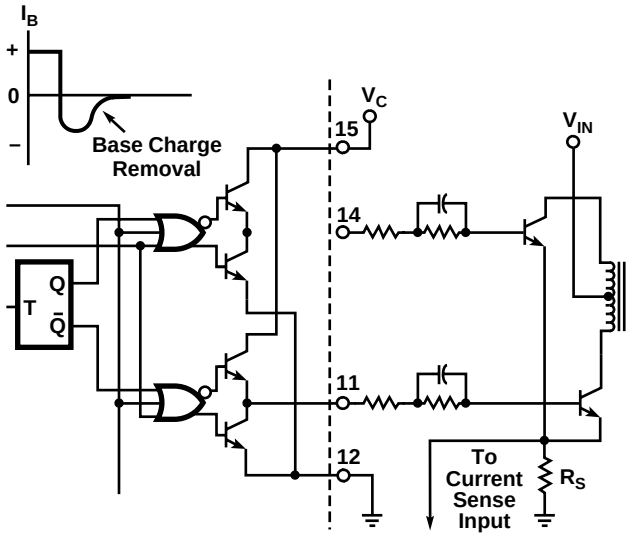


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft—Start curren is not affected by R_1.

The new equation for Soft—Start is $t \approx \frac{V_{CLAMP} + 0.6}{9.0\ A} (C_{SS})$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 14. Buffered Maximum Clamp Level



The totem pole output can furnish negative base current for enhanced transistor turn—of f, with the addition of the capacitor in series with the base

Figure 15. Bipolar Transistor Drive

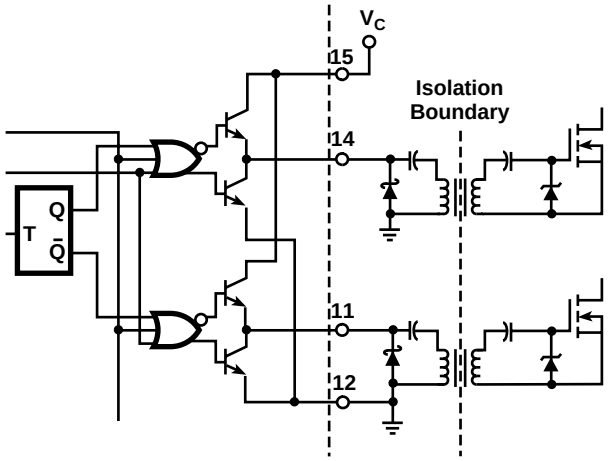


Figure 16. Isolated MOSFET Drive

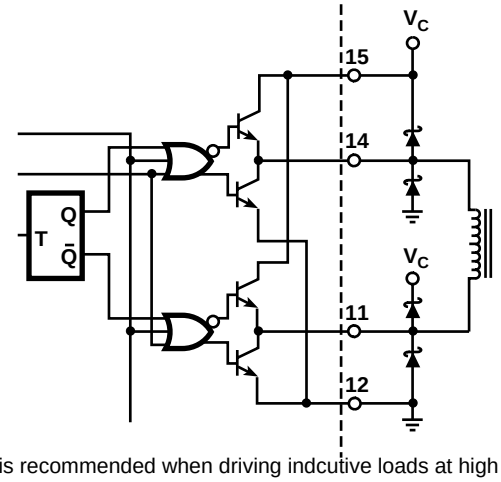
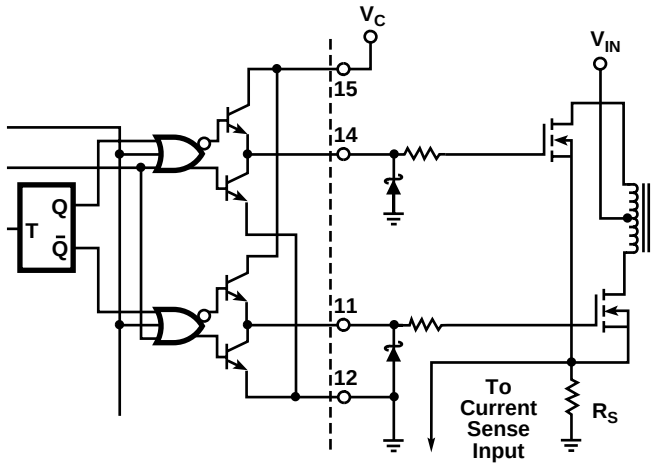


Figure 17. Direct Transformer Drive

The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving indcutive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being drien below ground.



A series gate resistor may be needed to damp high frequency parasitic oscillation caused by a MOSFET's input capacitance and any series wiring inductance in the gate—source circuit. The series resistor will also decrease the MOSFET's switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 18. MOSFET Parasitic Oscillations

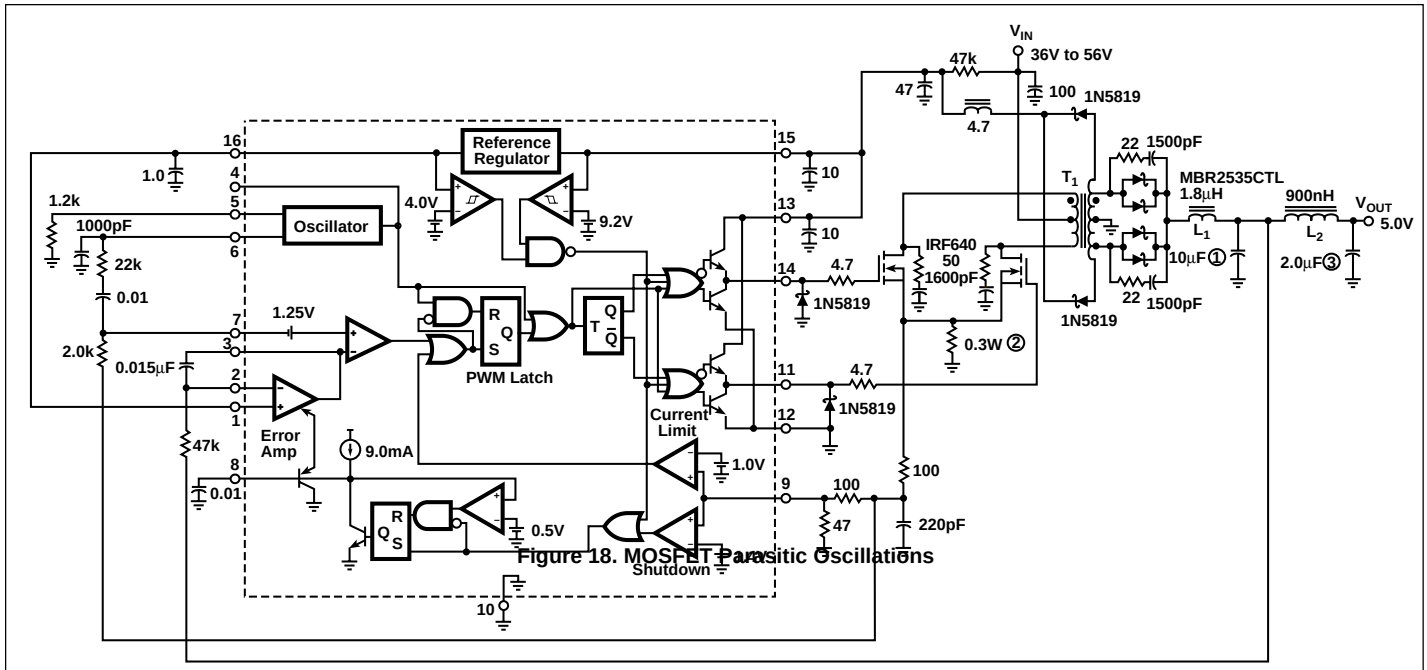


Figure 18. MOSFET Parasitic Oscillations

T_1 —Primary: 16 turns center tapped #48AV
Secondary: 4 turns center tapped 0.003" (2 layers) copper foil
Bootstrap: 1 turn added to each secondary output #36AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269—A

L_1 —2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10—3F3
Bobbin: Philips part #EP10PCB1—8
L = 1.8mH
Coilcraft P3270—A

L_2 —7 turns #18AWG, 1/2" diameter air core
Coilcraft P3271—A

Heatsinks —Power FET: AAVID Heatsink #533902B02554 with clip
Output Rectifiers: AAVID Heatsink #533402B02552 with clip

Insulators —All power devices are insulated with Berquist Sil—Pad 1500

① —10 (1.0mF) ceramic capacitors in parallel
② —5 (1.5‰) resistors in parallel
③ —2 (1.0mF) cearmic capacitors in parallel

Test	Condition	Result
Line Regulation	V_{IN} = 40V to 56V, I_{OUT} = 15A	14mV = –0.275%
Load Regulation	V_{IN} = 48V, I_{OUT} = 8.0V to 15A	54mV = –1.0%
Output Ripple	V_{IN} = 48V, I_{OUT} = 15A	50mVp—p
Efficiency	V_{IN} = 48V, I_{OUT} = 15A	71.2%

Figure 19. Application Circuit

TC33025

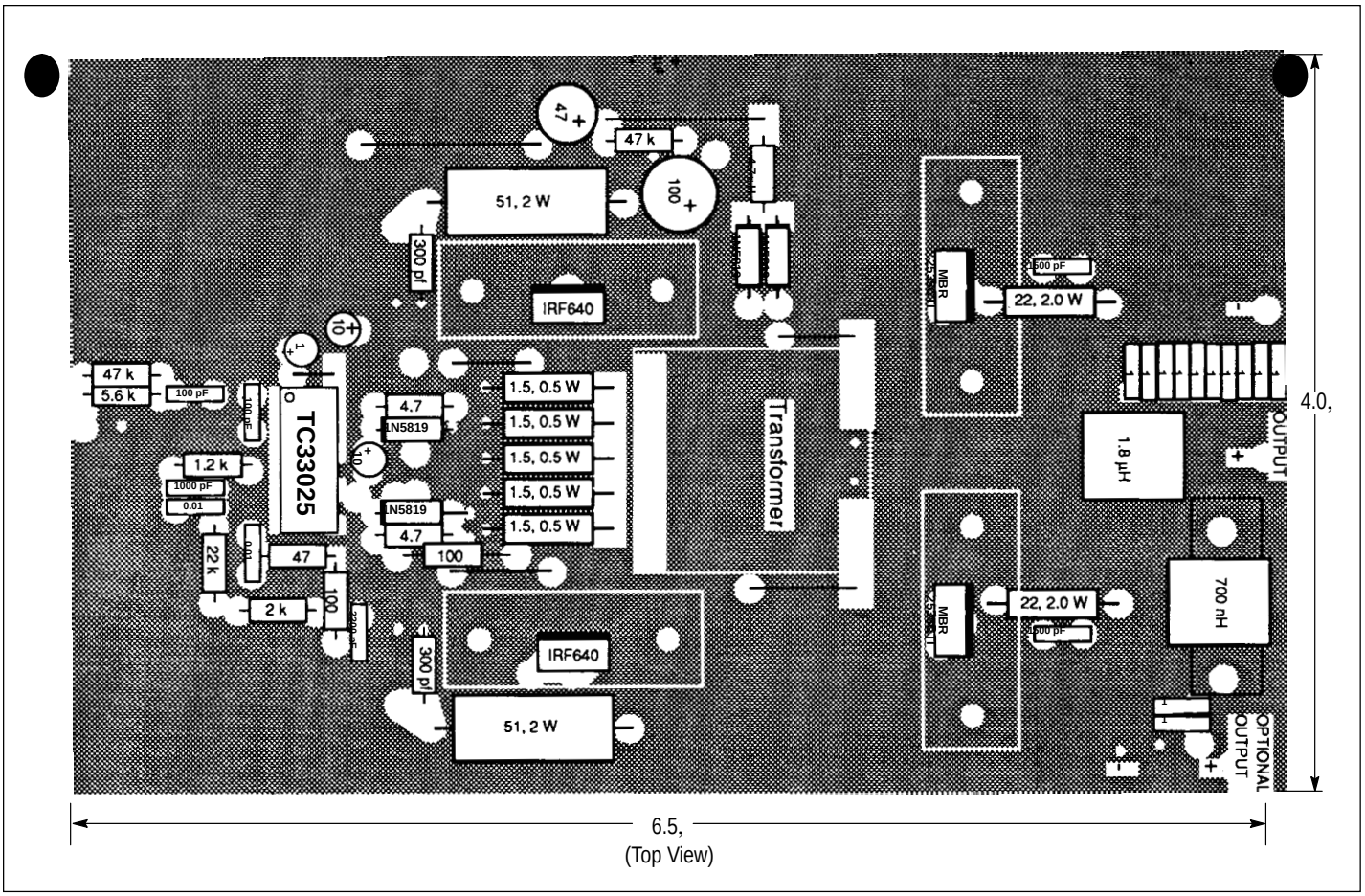
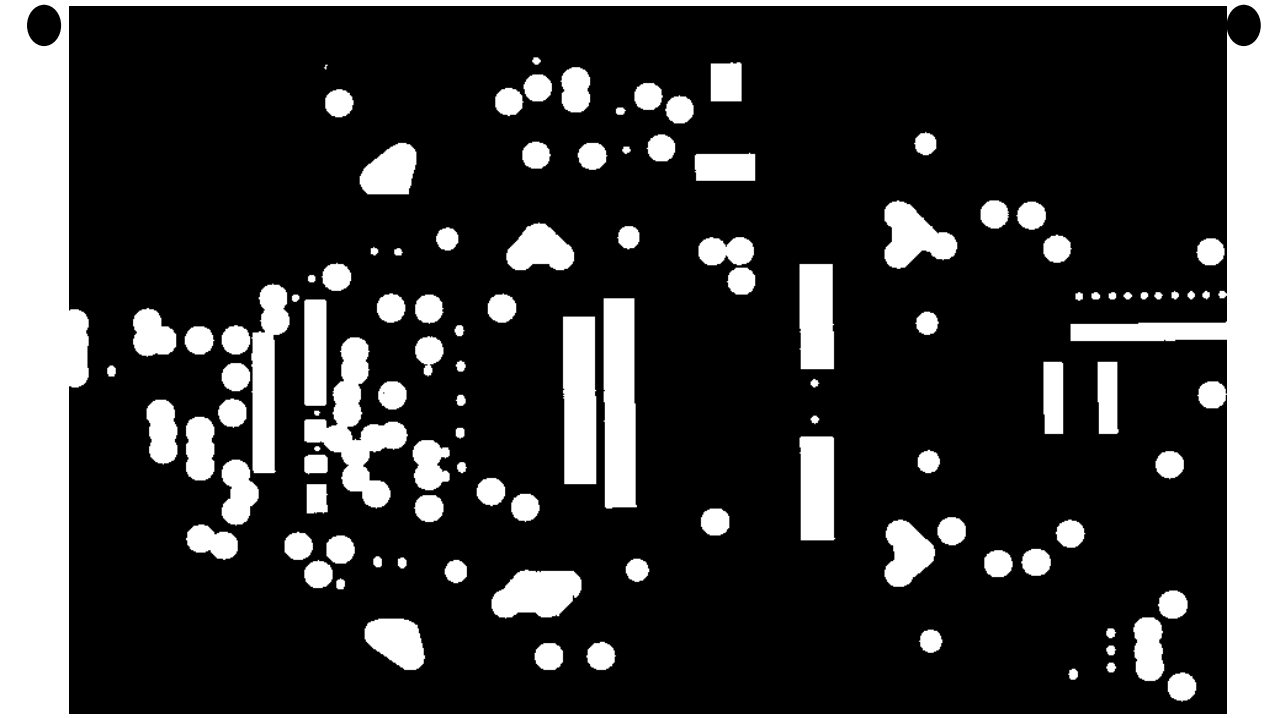
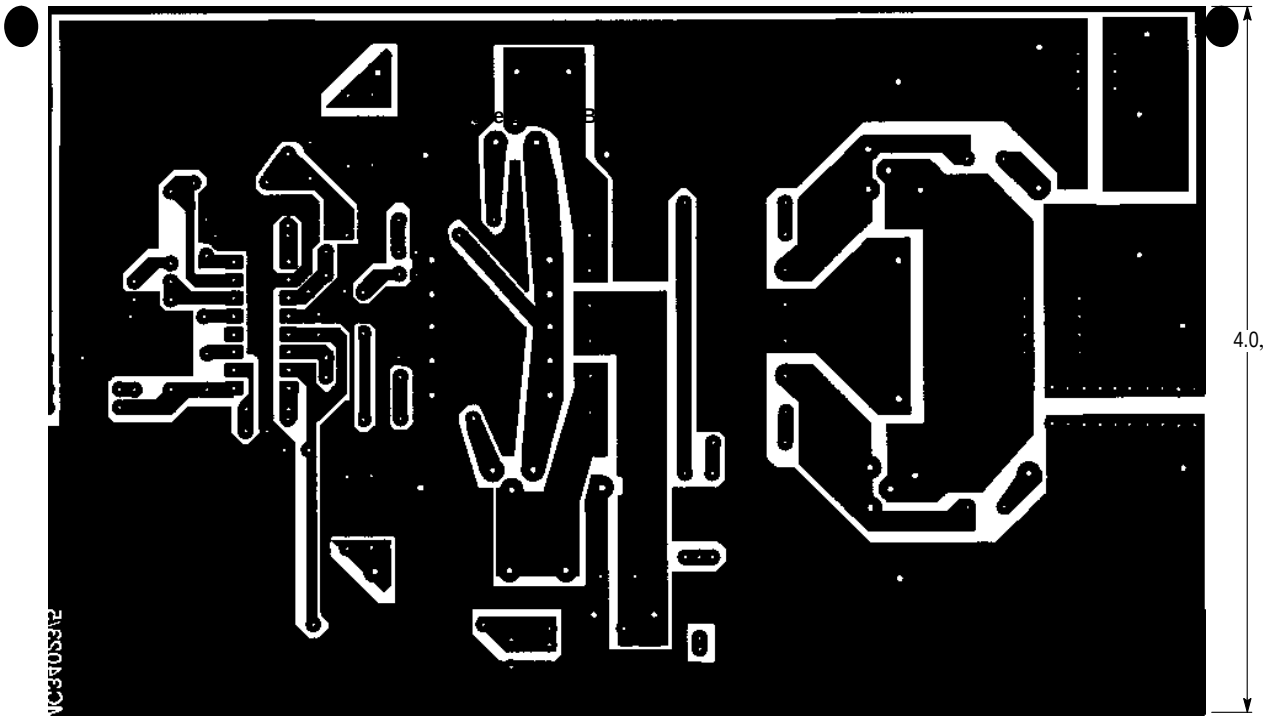


Figure 20. PC Board With Components



(Top View)



(Bottom View)

Figure 21. PC Board Without Components

TC33025

TYPICAL CHARACTERISTICS

Figure 22. Timing Resistor versus Oscillator Frequency

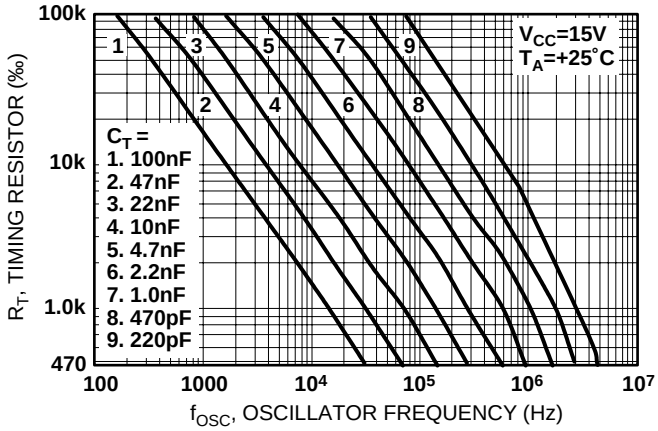


Figure 23. Oscillator Frequency versus Temperature

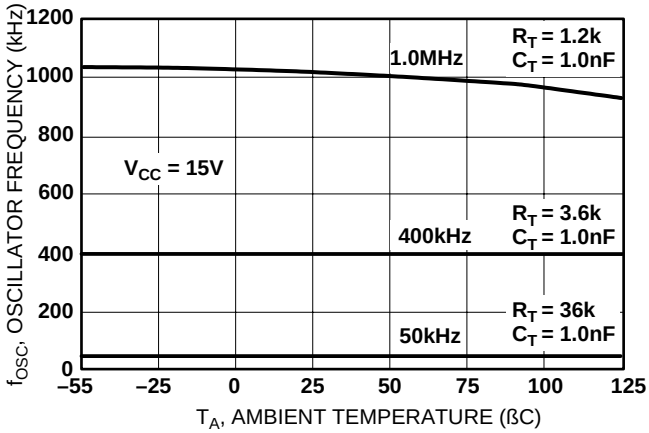


Figure 24. Error Amp Open Loop Gain and Phase versus Frequency

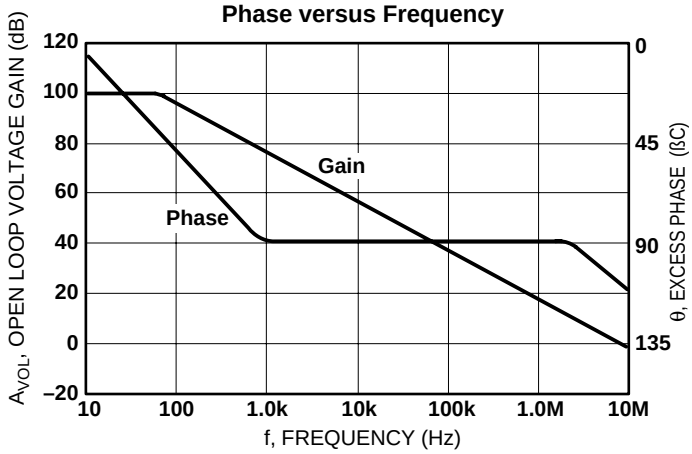


Figure 25. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

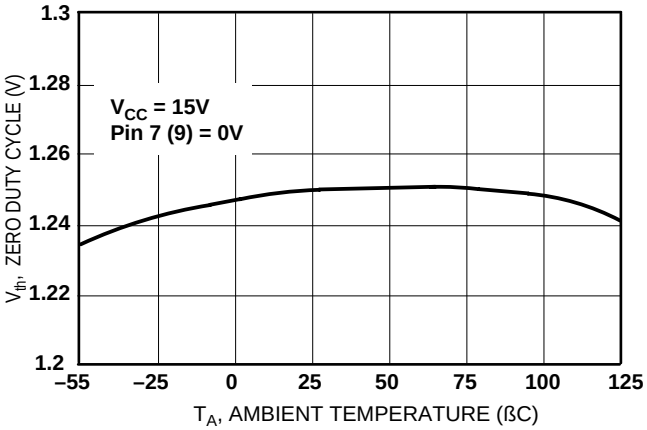


Figure 26. Error Amp Small Signal Transient Response

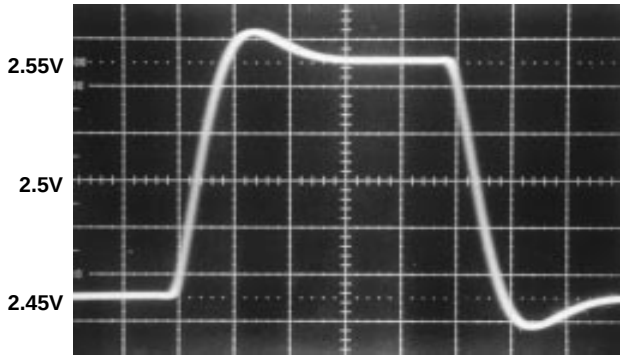
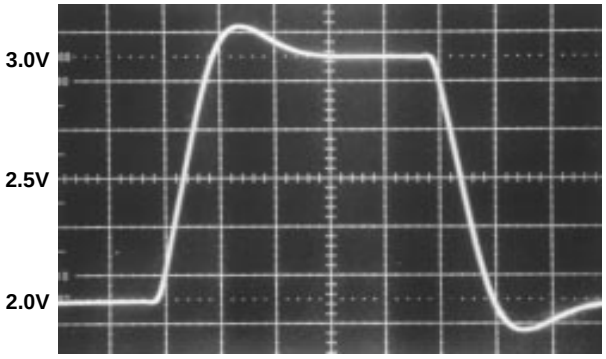


Figure 27. Error Amp Large Signal Transient Response



TYPICAL CHARACTERISTICS

Figure 28. Reference Voltage Change versus Source Current

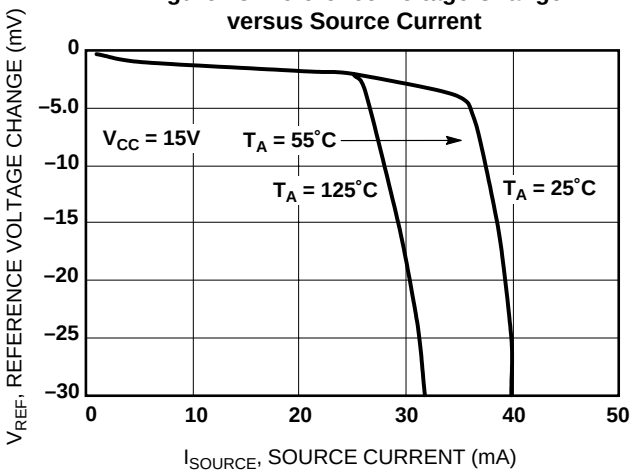


Figure 29. Reference Short Circuit Current versus Temperature

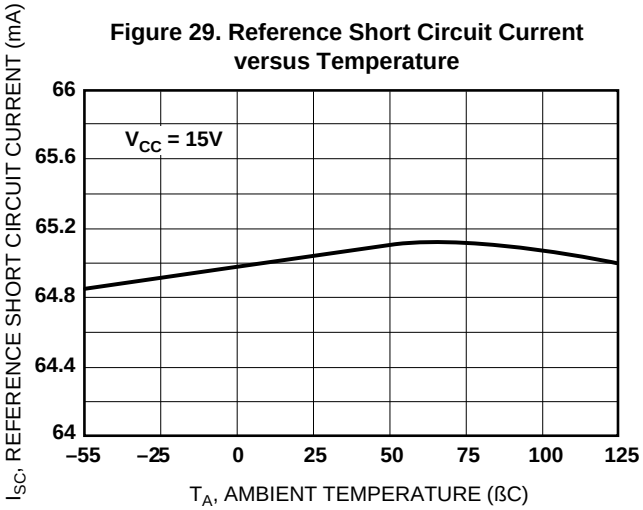
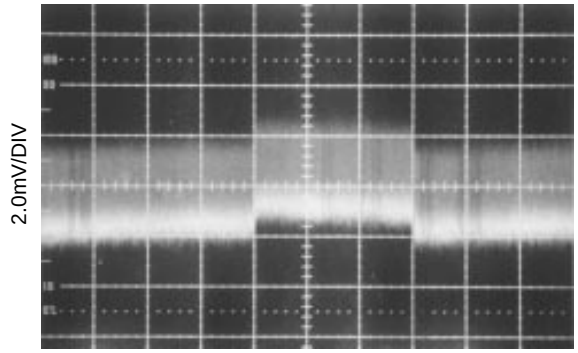
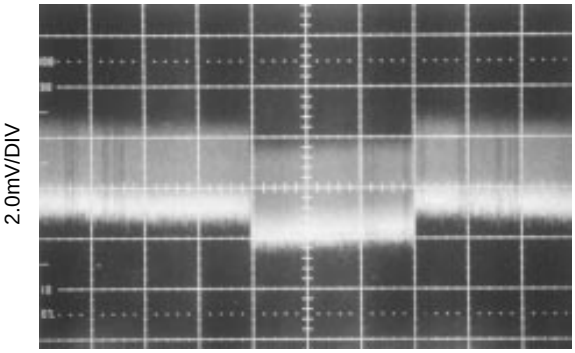


Figure 30. Reference Line Regulation



V_{REF} LINE REGULATION 10V — 24V
2.0msec /DIV

Figure 31. Reference Load Regulation



V_{REF} LINE REGULATION 1.0mA — 24mA
2.0msec/DIV

Figure 32. Current Limit Comparator Threshold Change versus Temperature

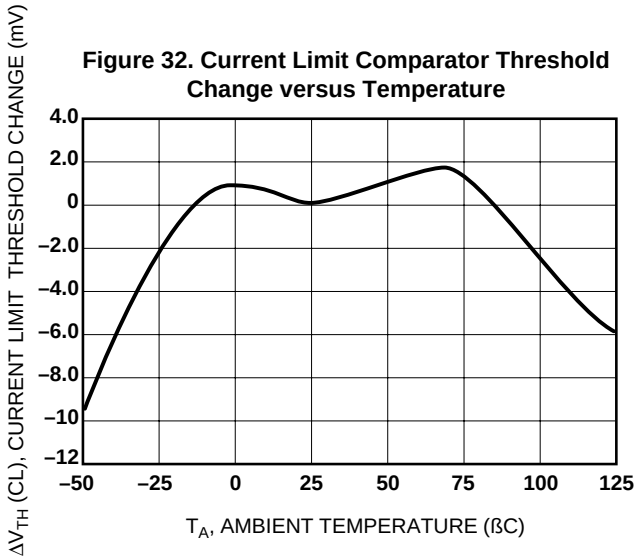
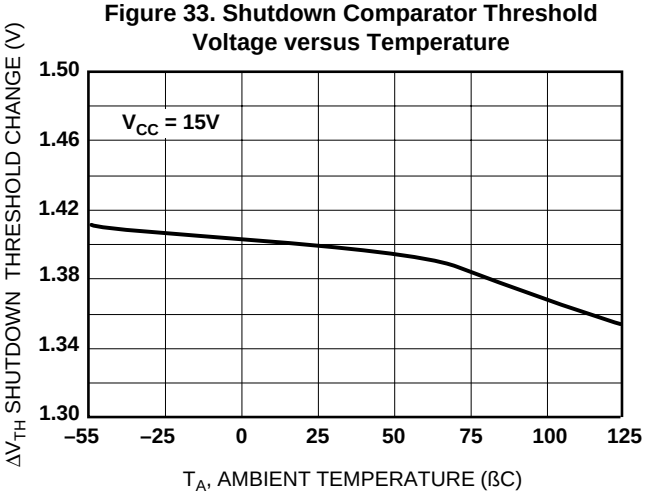


Figure 33. Shutdown Comparator Threshold Voltage versus Temperature



TC33025

TYPICAL CHARACTERISTICS

Figure 34. Soft–Start Charge Current versus Temperature

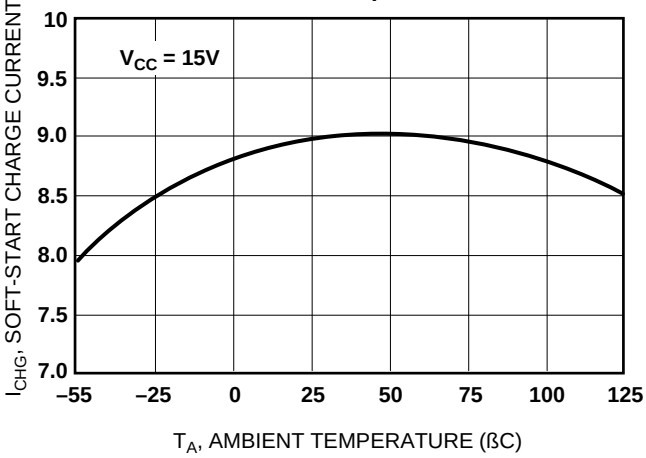


Figure 35. Output Saturation Voltage versus Load Current

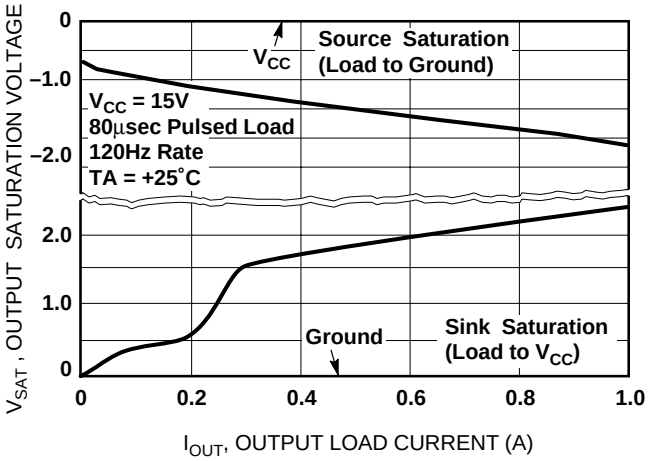
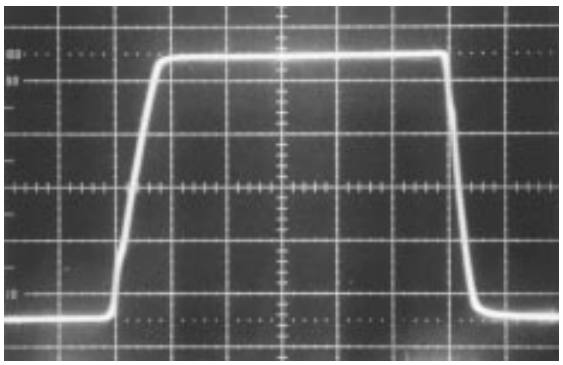
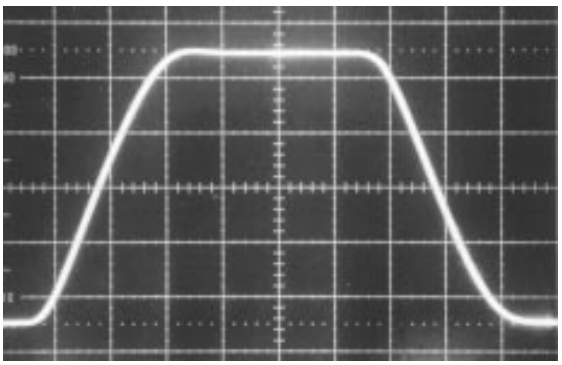


Figure 36. Drive Output Rise and Fall Time



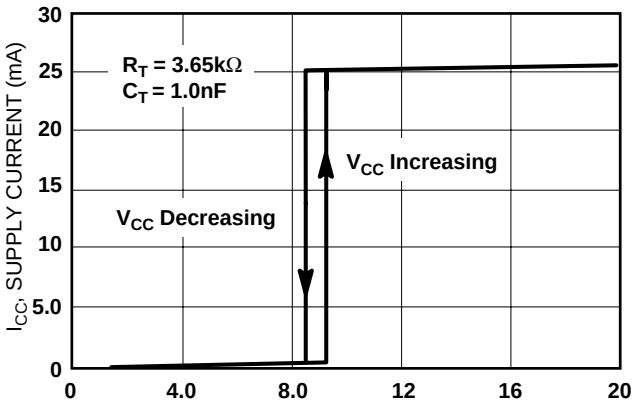
OUTPUT RISE & FALL TIME 1.0nF LOAD
50nsec/DIV

Figure 37. Drive Output Rise and Fall Time



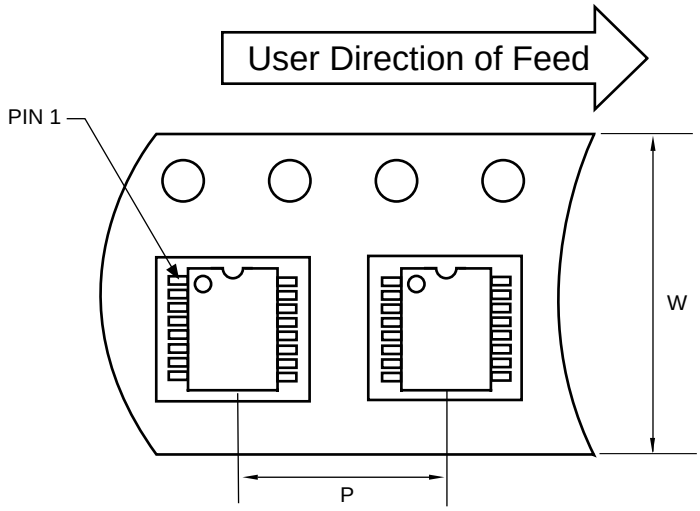
OUTPUT RISE & FALL TIME 10nF LOAD
50nsec/DIV

Figure 38. Supply Voltage versus Supply Current



TAPE AND REEL DIAGRAM

Component Taping Orientation for 16-Pin SOIC (Wide) Devices



Standard Reel Component Orientation
for TR Suffix Device

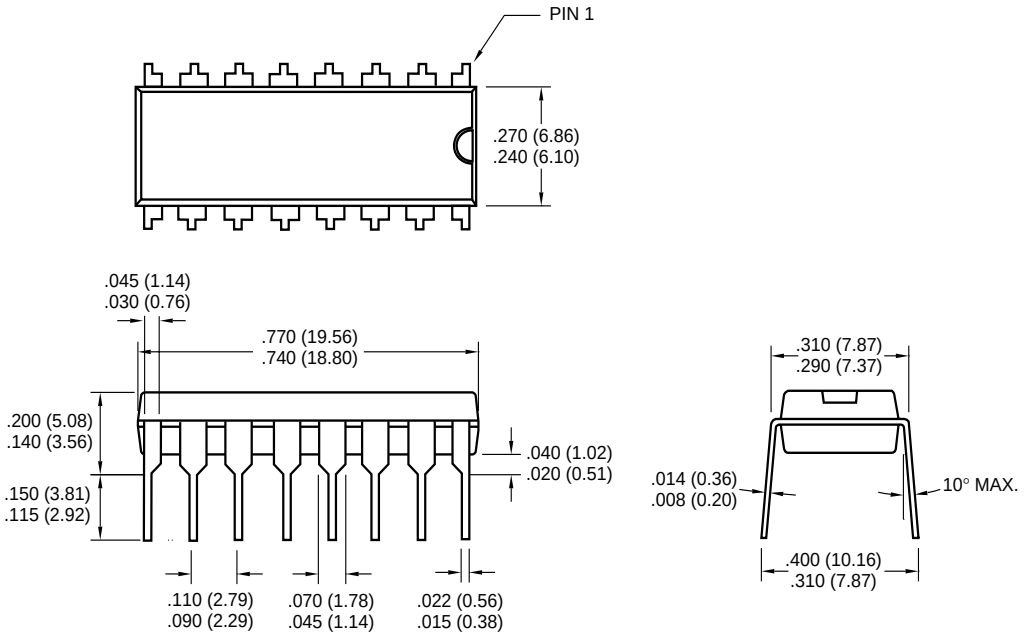
Carrier Tape, Reel Size, and Number of Components Per Reel

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin SOIC (W)	16 mm	12 mm	1000	13 in

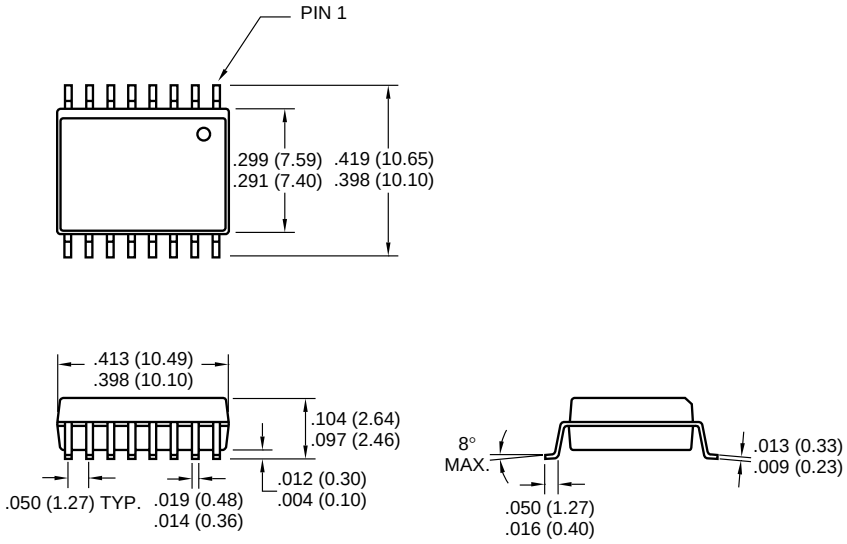
TC33025

PACKAGE DIMENSIONS

16-Pin PDIP (Narrow)



16-Pin SOIC (Wide)



Dimensions: inches (mm)

Sales Offices

TelCom Semiconductor, Inc.
1300 Terra Bella Avenue
P.O. Box 7267
Mountain View, CA 94039-7267
TEL: 650-968-9241
FAX: 650-967-1590
E-Mail: liter@telcom-semi.com

TelCom Semiconductor, GmbH
Lochhamer Strasse 13
D-82152 Martinsried
Germany
TEL: (011) 49 89 895 6500
FAX: (011) 49 89 895 6502 2

TelCom Semiconductor H.K. Ltd.
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San Po Kong, Kowloon
Hong Kong
TEL: (011) 852-2350-7380
FAX: (011) 852-2354-9957