November 2001 FN9043.1

Crusoe™ Processor Core-Voltage Regulator

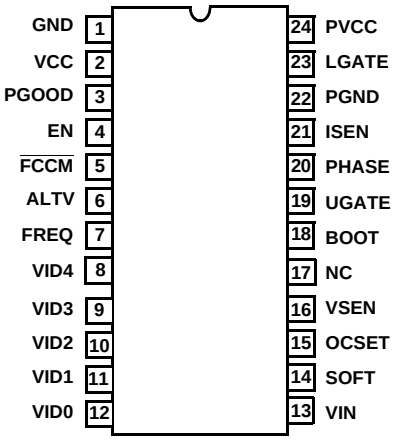
The ISL6211 is a single-output power-controller to power core of Transmeta's Crusoe™ CPU. The ISL6211 includes a 5-bit digital-to-analog converter (DAC) that adjusts the core PWM output voltage from 0.6VDC to 1.75VDC. The DAC settings may be changed during operation. Special measures are taken to allow such a transition with controlled slew rate to comply with Transmeta's LongRun™ technology. A precise reference and a proprietary architecture with integrated compensation provide excellent static and dynamic core voltage regulation.

In nominal currents, the controller operates at a selectable frequency of 300kHz or 600kHz. When the filter inductor current becomes discontinuous, the controller operates in a hysteretic mode dramatically improving system efficiency. The hysteretic mode of operation can be inhibited by a designated control pin.

The ISL6211 monitors the output voltage. A Power-Good signal is issued when soft start is completed and the output is in regulation. A built-in over-voltage protection prevents the load from seeing output voltages higher than 1.9V. Under-voltage protection latches the chip off when the output drops below 75% of the set value. The PWM controller's over-current circuitry monitors the converter load by sensing the voltage drop across the lower MOSFET. The overcurrent threshold is set by an external resistor. If precision overcurrent protection is required, an external current-sense resistor may optionally be used.

Pinout

ISL6211 (SSOP)
TOP VIEW



Features

- High Efficiency Over Wide Load Range
- Loss-Less Current-Sense Scheme
  - Uses MOSFET's $R_{DS(ON)}$
  - Optional Current-Sense Resistor for Higher Tolerance Overcurrent Protection
- Powerful Gate Drivers with Adaptive Dead Time
- Summing Current-Mode Control and On-Chip Active Droop for Optimum Transient Response
- TTL-Compatible 5-Bit Digital Output Voltage Selection
  - Wide Range - 0.6VDC to 1.0VDC in 25mV Steps, and from 1.0VDC to 1.75VDC in 50mV Steps
  - "On-the-Fly" VID code change with customer programmable slew rate
- Alternative Input to Set Output Voltage During Start-up or Power Saving Modes
- Selectable Forced Continuous Conduction Mode of Operation
- Power-Good Output Voltage Monitor
- No Negative Core Voltage on Turn-off
- Over-Voltage, Under-Voltage and Over-Current Fault Monitors
- 300/600kHz Selectable Switching Frequency

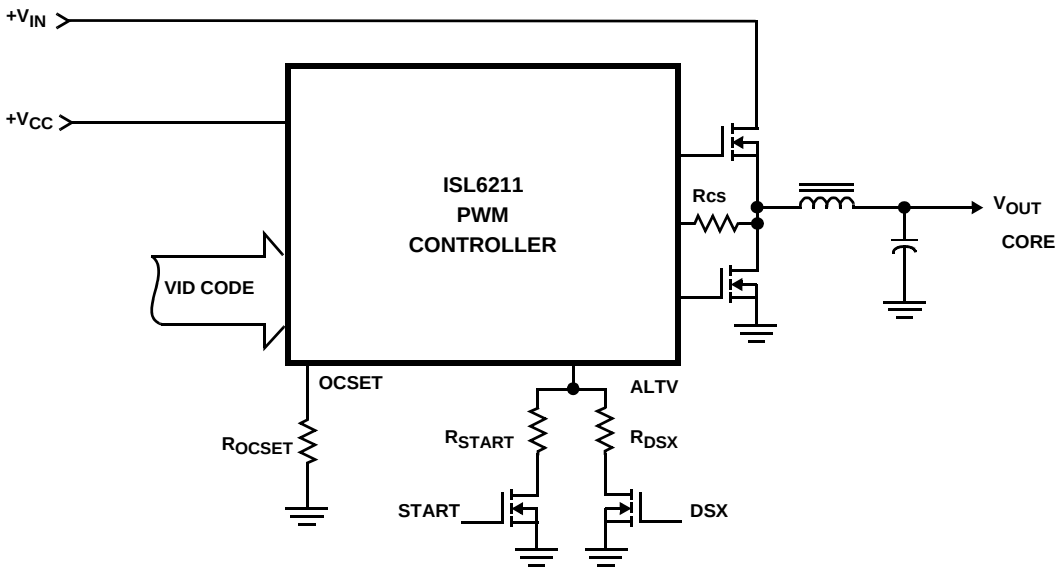
Applications

- Mobile PCs
- Web Tablets
- Internet Appliances

Ordering Information

PART NUMBER	TEMP. (^{o}C)	PACKAGE	PKG. NO.
ISL6211CA	-10 to 85	24 Ld SSOP	M24.15
ISL6211CA-T	-10 to 85	24 Ld SSOP, Tape and Reel	M24.15

Simplified Power Diagram



Absolute Maximum Ratings

Bias Voltage, V_{CC} . . . . . +6.5V
Input Voltage, V_{in} . . . . . +27.0V
PHASE, BOOT, ISEN, UGATE . . . . . GND-0.3V to +33.0V
BOOT with respect to PHASE . . . . . +6.5V
All Other Pins. . . . . GND - 0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class 1

Recommended Operating Conditions

Bias Voltage, V_{CC} . . . . . +5.0V ±5%
Input Voltage, V_{IN} . . . . . +5.0V to 24.0V
Ambient Temperature Range. . . . . -10^oC to 85^oC
Junction Temperature Range . . . . . -10^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SSOP Package	85

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

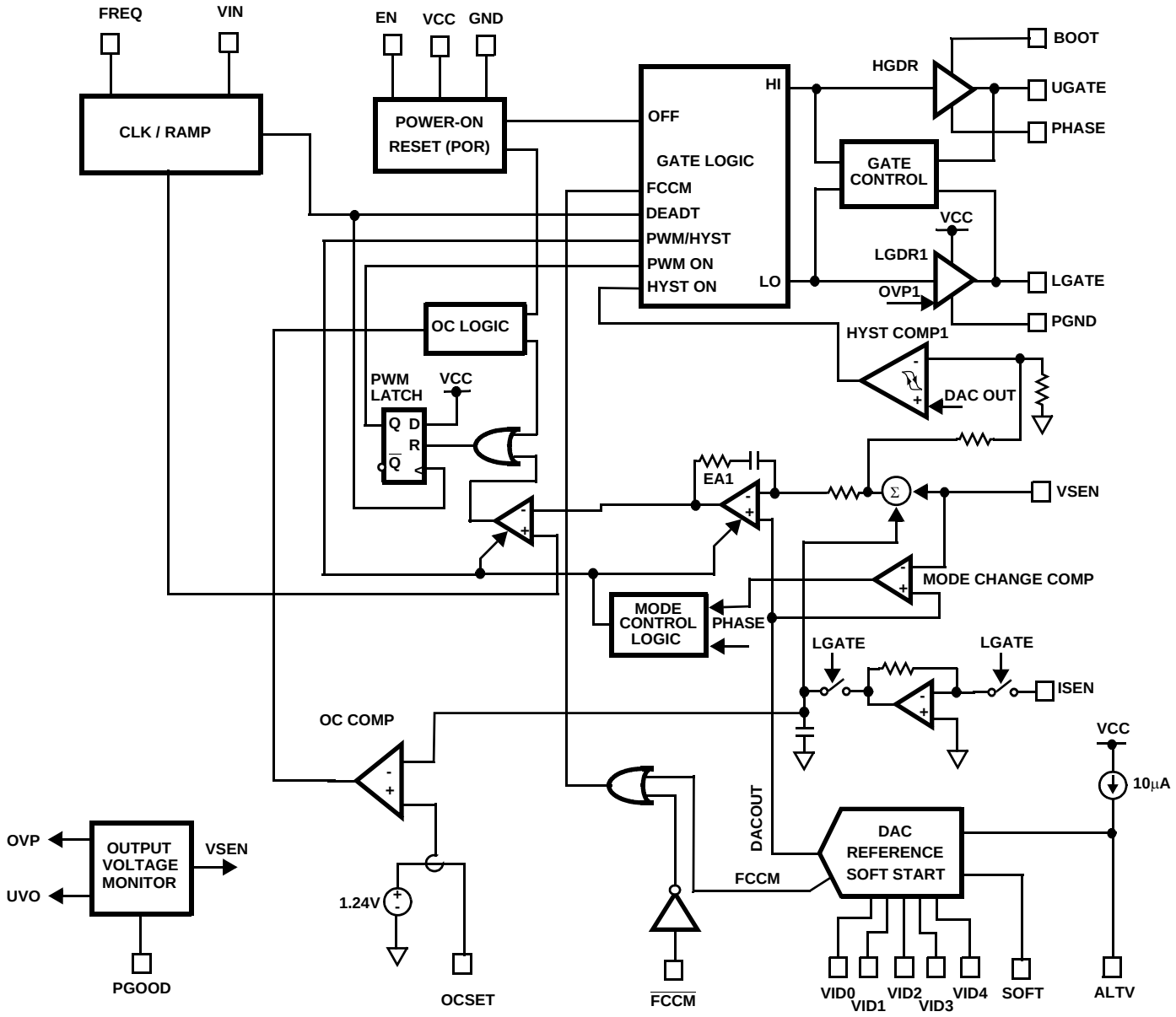
Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Nominal Supply Current	I_{CC}	GATE Open	-	2.7	3.2	mA
Shut-down Supply Current	I_{CCS}		-	6	30	µA
Battery Pin Supply Current	I_{VIN}		-	12	20	µA
Battery Pin Leakage Current at Shut-Down	I_{VINSD}		-	-	1	µA
POWER-ON RESET						
Rising VCC Threshold	V_{THU}		4.3	4.65	4.75	V
Falling VCC Threshold	V_{THD}		4.1	4.35	4.45	V
OSCILLATOR						
Free Running Frequency 1	F_{CLK1}	FREQ = 0	255	300	345	kHz
Free Running Frequency 2	F_{CLK2}	FREQ = 1	510	600	690	kHz
Ramp Amplitude, pk-pk		V_{IN} = 16V, FREQ = 0 or FREQ = 1, By design	-	2	-	V
Ramp Offset		By design	-	0.5	-	V
REFERENCE, DAC AND SOFT START						
VID0-VID4 Input Low Voltage			-	-	1.21	V
VID0-VID4 Input High Voltage			1.62	-	-	V
VID0-VID4 Pull-Up Current to Internal 2.5V			-	12	-	µA
DAC Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-Up	I_{SS}	Vsoft = 0V	20	26	32	µA
Soft-Start Current During Mode Change	I_{SSM}	Vsoft = 0.5V...1.75V	350	500	650	µA
ALTV Current	I_{ALTV}		-	-10	-	µA
ALTV Current Accuracy			-5.0	-	+5.0	%

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ALTV to VID Transition Voltage	V_{AVTH}		1.71	1.75	1.78	V
ENABLE						
Enable Voltage Low	V_{ENLOW}	IC Inhibited	-	-	1.2	V
Enable Voltage High	V_{ENHIGH}	IC Enabled	2.0	-	-	V
PWM CONVERTER						
Output Voltage	VOUT1	Defined by the VID code (Table 1) or ALTV pin	0.6	-	1.75	V
Under-Voltage Shut-Down Level	V_{UV1}	Percent of the voltage set by VID code or ALTV pin Disabled during dynamic VID code change	72	75	78	%
Under-Voltage Shut Down Delay	T_{DOC1}	By design	1.2	-	1.6	µs
Over-Voltage Threshold	V_{OVP1}		1.90	1.95	2.00	V
Over-Voltage Protection Delay	T_{DOV1}	By design	1.6	-	3.2	µs
ERROR AMPLIFIER						
DC Gain		By design	-	86	-	dB
Gain-Bandwidth Product	GBWP	By design	-	2.7	-	MHz
Slew Rate	SR	By design	-	1	-	V/µs
GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{1UGPUP}		-	3.8	5	Ω
Upper Drive Pull-Down Resistance	R1UGPDN		-	1.6	3	Ω
Lower Drive Pull-Up Resistance	R_{1LGPUP}		-	3.8	5	Ω
Lower Drive Pull-Down Resistance	R_{1LGPDN}		-	0.8	1.5	Ω
POWER GOOD						
V_{OUT} Upper Threshold		Percent of the voltage defined by the VID code	123	-	127	%
V_{OUT} Lower Threshold, Falling Edge		Percent of the voltage defined by the VID code	77	-	81	%
V_{OUT} Lower Threshold, Rising Edge		Percent of the voltage defined by the VID code	87	-	94	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.5	V
PGOOD Leakage Current	I_{PGILKG}	V_{PULLUP} = 5.0V	-	-	1	µA

Block Diagram



Functional Pin Description (Pins are referenced to SSOP package)

GND (Pin 1)

This is a signal ground for the IC. All voltage levels are measured with respect to this pin.

VCC (Pin 2)

This pin powers the chip. The IC starts to operate when voltage on this pin exceeds 4.6V and shuts down when it drops below 4.2V.

PGOOD (Pin 3)

PGOOD is an open drain output used to indicate the status of the output voltage. This pin is pulled low when the core output is not within +25% -10% of the VID reference voltage, or when any of the fault conditions have occurred. The PGOOD signal is kept asserted high during LongRun™ transitions.

EN (Pin 4)

This pin enables IC operation when left open or pulled-up to VCC. Also, it unlatches the chip after fault if being cycled.

$\overline{FCCM}$ (Pin 5)

This pin inhibits hysteretic mode of operation when set low.

ALTV (Pin 6)

Alternatively to VID code programming, the output voltage can be set by this pin. Such a requirement may occur during CPU initialization or during some power saving modes.

FREQ (Pin 7)

This pin sets the controller switching frequency. When connected to ground, the frequency is set to 300kHz. For 600kHz operation pin shall be connected to VCC.

VID0, VID1, VID2, VID3, VID4 (Pins 12, 11, 10, 9 and 8 respectively)

VID0-VID4 are the input pins to the 5-bit DAC. These five pins program the internal voltage reference, which sets the converter output voltage. It also sets the core PGOOD, UVP and OVP thresholds.

VIN (Pin 13)

VIN provides battery voltage to the oscillator for feed-forward rejection of input voltage variations.

SOFT (Pin 14)

This pin programs the soft start time during initialization and slew rate of core voltage during VID code change. Connect a capacitor from this pin to the ground. This capacitor (typically 0.2μF), along with an internal 25μA current source, sets the soft-start interval of the converter. When voltage on this pin exceeds 0.5V, the soft start is completed. After the soft-start is completed, the pin function has changed. The internal circuit regulates voltage on this pin to the value commanded by VID code. The pin now has 500μA source/sink capability that allows to set desired slew rate for upward and downward VID code changes.

OCSET (Pin 15)

A resistor from this pin to the ground sets the over-current protection level.

VSEN (Pins 16)

This pin provides sensing of CPU core voltage. The PGOOD, UVP and OVP comparators use voltage sensed by this pin for protection and monitoring.

BOOT (Pin 18)

This pin supplies power to the upper MOSFET driver. Connect this pin to the junction of the bootstrap capacitor and the cathode of the bootstrap diode. The anode of the bootstrap diode is are connected to pin 24, PVCC.

UGATE (Pin 19)

This pin provides gate drive to the upper MOSFET.

PHASE (Pin 20)

The PHASE node is a junction point of the upper MOSFET source, output filter inductor, and lower MOSFET drain.

ISEN (Pin 21)

This pin monitors the voltage drop across the lower MOSFET for current feedback and output voltage droop. To set the gain of the current sense amplifier, a resistor should be placed in series with ISEN input. For precise current detection, the optional current sense resistor placed in series with the source of the lower MOSFET can be used.

PGND (Pin 22)

This pin serves as a return path for the lower MOSFET gate driver. Tie the lower MOSFET source to this pin.

LGATE (Pin 23)

This pin provides gate drive to the lower MOSFET.

PVCC (Pin 24)

This pin powers the lower MOSFET gate driver.

Description

Operation Overview

The ISL6211 is a single output power management integrated circuit to address power needs of modern processors for notebook and sub-notebook PCs. The IC controls operation of a synchronous buck converter. The output voltage can be adjusted in the range from 0.6V to 1.75V by changing the DAC code settings (see Table 1). Alternatively, the output voltage can be set by an analog input. This feature is important in systems where VID code may not be determined during start-up or CPU core power saving modes. The output voltage of the core converter can be changed on-the-fly with programmable slew rate, which makes it especially suitable for Crusoe processors.

The converter can operate in two modes: fixed frequency PWM and variable frequency hysteretic depending on the load level. At loads lower than the critical where filter inductor current becomes discontinuous, hysteretic mode of operation is activated. Switchover from PWM to hysteretic operation at light loads improves the converters' efficiency and prolongs battery run time. As the filter inductor resumes continuous current, the PWM mode of operation is restored. The hysteretic mode of operation can be omitted by connecting the $\overline{FCCM}$ pin to GND.

The core converter incorporates Intersil's proprietary output voltage droop for optimum handling of fast load transients found in modern processors.

Initialization

The IPM6211 initializes upon receipt of input power assuming EN is high. The Power-On Reset (POR) function continually monitors the input supply voltage on the VCC pin and initiates soft-start operation after input supply voltage exceeds 4.6V. Should this voltage drop lower than 4.2V, POR disables the chip.

Soft-Start

When soft start is initiated, the voltage on the SOFT pin starts to ramp gradually due to the 25µA current sourced into the external capacitor.

When SOFT-pin voltage reaches 0.5V, the value of the sourcing current rapidly changes to 500µA charging the soft-start capacitor to the level determined by the DAC. This completes the soft start sequence, Figure 2. As long as the SOFT voltage is above 0.5V, the maximum value of the internal soft-start current is set to 500µA allowing fast rate-of-change in the core output voltage due to a VID code change. In this mode SOFT has both sourcing and sinking capabilities to maintain voltage across the soft-start capacitor conforming to the VID code.

This dual slope approach helps to provide safe rise of voltages and currents in the converters during initial start-up and at the same time sets a controlled speed of the core voltage change when the processor commands to do so.

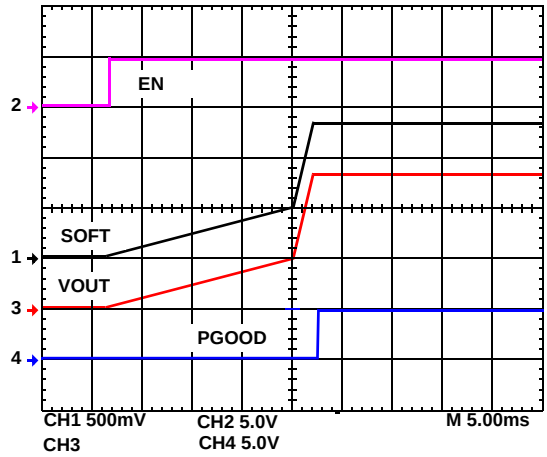


FIGURE 1.

The value of the soft-start capacitor can be estimated by the following equation:

$$Csoft = \frac{\Delta Issm}{\Delta Vdac}\Delta t$$

For the typical conditions when Vdac=0.05V, Dt=32µs

$$Csoft = \frac{500\mu A}{0.05V}32\mu s = 0.33\mu F$$

With this value of the soft-start capacitor, soft start time will be equal to:

$$Tsoft = \frac{0.33\mu F \cdot 0.5V}{25\mu A} = 6.6ms$$

The ramp up time to 1.2V will be equal to:

$$Tup = 6.6 + 0.46 = 7.06ms$$

Converter Operation

At the nominal current core converter operates in a fixed frequency PWM mode. The output voltage is compared with a reference voltage set by the DAC. The derived error signal is amplified by an internally compensated error amplifier and applied to the inverting input of the PWM comparator. To provide output voltage droop for enhanced dynamic load regulation, a signal proportional to the output current is added to the voltage feedback signal. This feedback scheme in conjunction with a PWM ramp proportional to the input voltage allows for fast and stable loop response over a wide range of input voltage and output current variations. For the sake of efficiency and maximum simplicity, the current sense signal is derived from the voltage drop across the lower MOSFET during its conduction time.

Output Voltage Program

The output voltage of the converter is programmed to discrete levels between $0.6V_{DC}$ and $1.75V_{DC}$ as specified in Table 1. This output is designed to supply the microprocessor core voltage. The voltage identification (VID) pins program an internal voltage reference (DAC) through a TTL-compatible 5-bit digital-to-analog converter. The level of the DAC voltage

also sets the PGOOD, UVP and OVP thresholds. The VID pins can be left open to set logic 1 as they are pulled up to the internal +2.5V voltage source by a 12μA current source.

TABLE 1.

PIN NAME					NOMINAL OUT1 VOLTAGE
VID4	VID3	VID2	VID1	VID0	
0	0	0	0	0	1.750
0	0	0	0	1	1.700
0	0	0	1	0	1.650
0	0	0	1	1	1.600
0	0	1	0	0	1.550
0	0	1	0	1	1.500
0	0	1	1	0	1.450
0	0	1	1	1	1.400
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.900
1	0	1	0	0	0.875
1	0	1	0	1	0.850
1	0	1	1	0	0.825
1	0	1	1	1	0.800
1	1	0	0	0	0.775
1	1	0	0	1	0.750
1	1	0	1	0	0.725
1	1	0	1	1	0.700
1	1	1	0	0	0.675
1	1	1	0	1	0.650
1	1	1	1	0	0.625
1	1	1	1	1	0.600

NOTE: 0 = connected to GND or V_{SS}, 1 = open or connected to Vcc or voltage source of 2.5V...5.0 through pull-up resistors.

Alternative Voltage Programming Input

Alternatively to VID code programming, the output voltage can be set by an ALTV pin. The necessity of such input is dictated by the fact that during power-up and some power saving modes of operation, the voltage on the processor is insufficient to provide correct VID codes to the controller. The required core voltage should be set by some means external to the processor. One of the most common approaches to this problem is to provide hard wired VID code via multiplexer controlled by the CPU. Providing high degree of flexibility, the approach lacks simplicity and takes many external components and valuable motherboard area. The ISL6211 uses the simpler way to set the core voltages when the CPU is incapable of doing that.

The resistor-MOSFET network is connected to the ALTV pin as it is shown on Simplified Power Diagram and in the Figure 2. The calibrated current source of 10μA from ALTV pin creates the voltage drop on the resistor when the MOSFET conducts being activated by the input logic signal, for example DSX. The controller regulates the output voltage to the level established on the ALTV pin when this voltage is lower than the highest VID programmed voltage (1.75V). When the MOSFET in series with the resistor is turned off by the gate signal, the ALTV pin voltage rises to VCC signaling the chip that DSX signal is de-asserted. This high level signal commands the controller to regulate the output voltage to the level programmed by the VID code. This programming technique relies on the tolerance of the internal pull-up current and provides +/-5% accuracy of the voltage set.

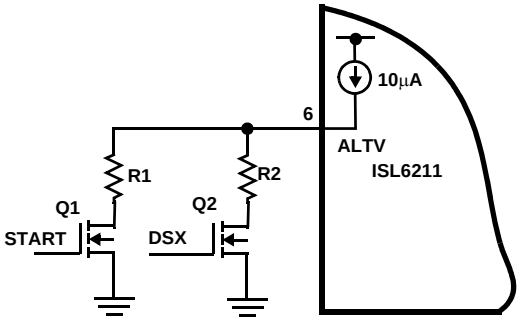


FIGURE 2. CIRCUIT FOR MORE PRECISE PROGRAMMING OF START AND DSX VOLTAGES

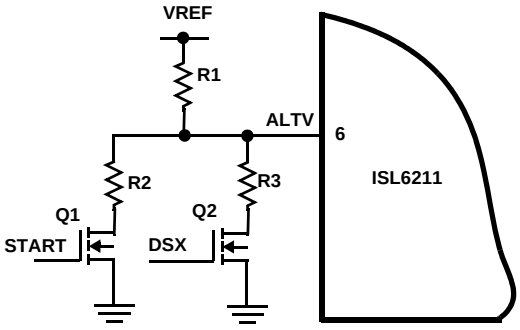


FIGURE 3. CIRCUIT FOR MORE PRECISE PROGRAMMING OF START AND DSX VOLTAGES

If a better accuracy is required, the circuit shown in the Figure 3 can be used instead. With this approach the set point accuracy depends mainly on the tolerance of an external reference voltage source.

$$R2 = \frac{V_{START} \bullet R1}{V_{REF} - V_{START} + R1 \bullet 10\mu A}$$

$$R3 = \frac{V_{DSX} \bullet R1}{V_{REF} - V_{DSX} + R1 \bullet 10\mu A}$$

Output Voltage Droop

An output voltage 'droop' or an active voltage positioning is now widely used in the computer power applications. The technique is based on raising the converter voltage at light load in anticipation of a possible load current step, Figure 4. Conversely, the output voltage is lowered at high load in anticipation of possible load drop. The output voltage varies with the load as if a resistor were connected in series with the converter's output. When done as a part of the feedback in a closed loop, the droop is not associated with substantial power losses, though, because there is no such resistor in the real circuit, rather the feature is emulated through feedback.

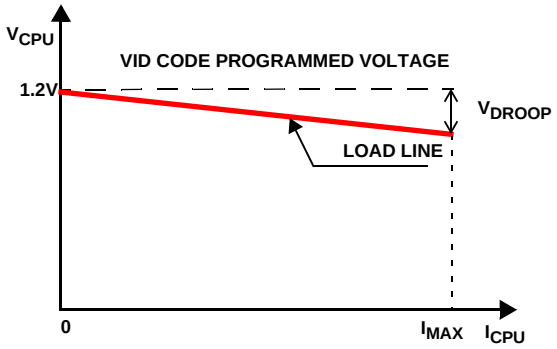


FIGURE 4. OUTPUT VOLTAGE DROOP

To get the most from the droop, its value should be scaled with capacitor's ESR voltage drop.

$$V_{DROOP} = I_{MAX} \bullet ESR$$

As Figure 5 shows, droop allows reduced size and cost of the output capacitors required to handle CPU current transients.

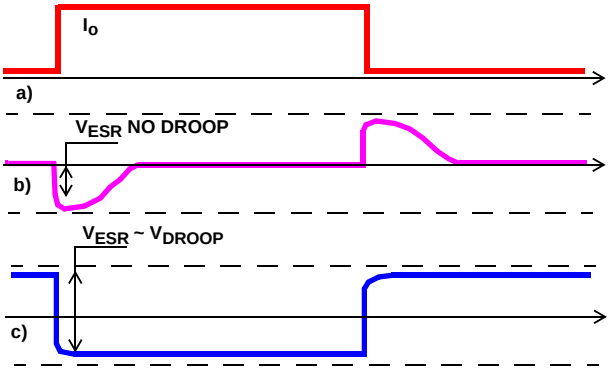
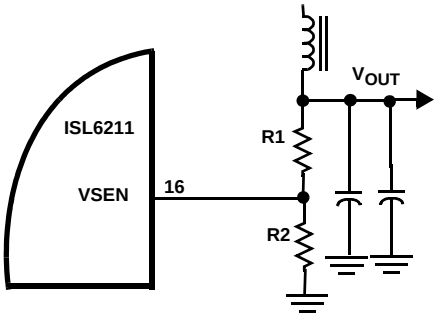


FIGURE 5. ADAPTIVE VOLTAGE POSITIONING

The reduction may be almost two times when compared to a system without the droop. Additionally, the CPU power dissipation is also slightly reduced as it is proportional to the applied voltage squared and even slight voltage decrease translates in a measurable reduction in power dissipated.

The Crusoe processor regulation window including transients is specified as +5%...-2%. To accommodate the droop, the output voltage of the converter is raised ~3.5% at no load conditions as it is shown in the Figure 6.



Vrise,% = R1/(R1+R2)

FIGURE 6. SETTING THE OUTPUT VOLATGE RISE AT NO LOAD CONDITIONS

The value of the resistor connected between the ISEN pin and the drain of the lower MOSFET sets the droop value.;

$$R_{CS} = \frac{2083 \bullet I_{MAX} \bullet R_{DS(ON)}}{V_{DROOP}} - 100\Omega$$

Where, V_{DROOP} is a desired value of the droop at maximum CPU current, I_{MAX} is a peak value of the inductor current in maximum load, $R_{DS(ON)}$ is a lower MOSFET impedance in conducting state.

The converter response to a load step is shown in the Figure 7. At zero load current, the output voltage is raised ~50mV above nominal value of 1.35V. When the load current increases, the output voltage droops down approximately 55mV. Due to use of droop, the converter's output voltage adoptively changes with the load current allowing better utilization of the regulation window.

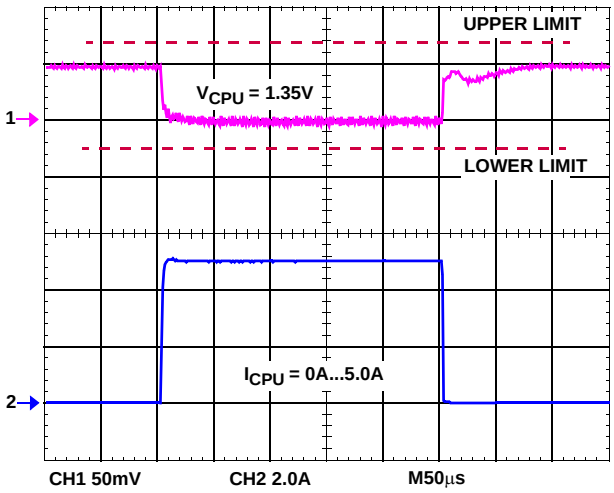


FIGURE 7. CONVERTER RESPONSE TO LOAD STEP

Operation Mode Control

In nominal load currents the synchronous buck converter operates in continuous conduction mode. Continuous conduction mode is also sustained during all upward and downward transitions commanded by either VID code change, or during transitions from alternatively programmed voltage to VID code set voltage, or vice versa. This mode of operation achieves higher efficiency due to the substantially lower voltage drop across the MOSFET compared to a Shottky diode. In contrast, continuous-conduction operation in load currents lower than the inductor critical value results in lower efficiency. In this case, during a fraction of a switching cycle, the direction of the inductor current changes to the opposite actively discharging the output filter capacitor. To maintain the output voltage in regulation, this voltage should be restored during the consequent cycle of operation by the cost of increased circulating current and losses associated with it.

The critical value of the inductor current can be estimated by the following expression.

$$I_{HYS} = \frac{(V_{IN} - V_O) \bullet V_O}{2 \bullet F_{SW} \bullet L_O \bullet V_{IN}}$$

To improve converter efficiency in loads lower than critical, the switch-over to variable frequency hysteretic operation with diode emulation is implemented into the PWM scheme. The switch-over is provided automatically by the mode control circuit that constantly monitors the inductor current and alters the way the PWM signal is generated.

The voltage across the synchronous MOSFET at the moment of time just before the upper-MOSFET turns on is monitored for purposes of mode change. When the converter operates in currents higher than critical, this voltage is always positive as shown in the Figures 8, 9. In currents lower than critical, the voltage is always negative. The mode control circuit uses a sign of voltage across the synchronous devices to determine if the load current is higher or lower than the critical value.

To prevent chatter between operating modes, the circuit looks for eight sequential matching sign signals before it makes its decision to perform a mode change. The same algorithm is true for both CCM-hysteretic and hysteretic-CCM transitions.

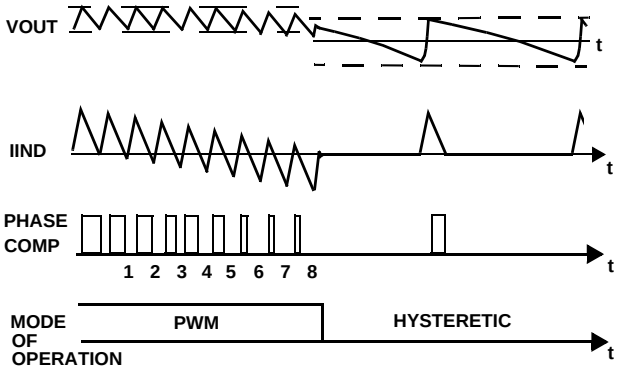


FIGURE 8. CCM -- HYSTERETIC TRANSITION

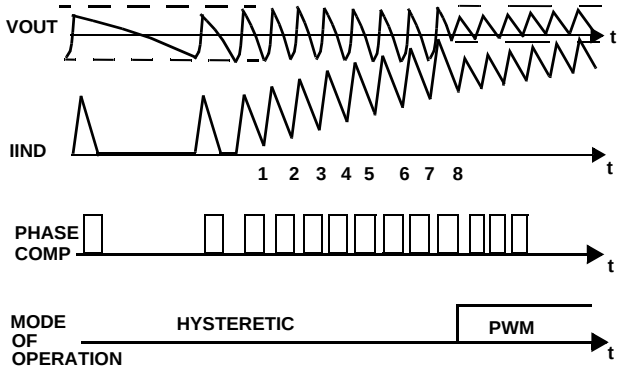


FIGURE 9. HYSTERETIC - CCM TRANSITION

Hysteretic Operation

When the critical inductor current is detected, the IC enters hysteretic mode. The PWM comparator and the error amplifier that provided control in the CCM mode are inhibited and the hysteretic comparator is now activated. A change is also made to the gate logic. In hysteretic mode the synchronous rectifier MOSFET is controlled in diode emulation mode, hence conduction in the second quadrant is prohibited.

The hysteretic comparator initiates the PWM signal when the output voltage gets below the lower threshold and terminates the PWM signal when the output voltage rises over the upper threshold. A spread or hysteresis between these two thresholds determines the switching frequency and the peak value of the inductor current. A transition to a constant frequency CCM mode will happen when the load current gets to a level higher than the critical:

$$I_{CCM} \approx \frac{\Delta V_{hys}}{2 \bullet ESR}$$

Where, ΔV_{hys}= 15mV, is a hysteretic comparator window, ESR is the equivalent series resistance of the output capacitor.

Because of different control mechanisms, the value of the load current where transition into CCM operation takes place

is usually higher compared to the load level at which transition into hysteretic mode had occurred.

The hysteretic mode of operation can be disabled by the $\overline{FCCM}$ pin when it is set low. The presence of this pin enhances applicability of the controller.

The Figure 10 shows the example of an application circuit where the hysteretic mode of operation is only allowed in a Deep Sleep Extension (DSX) mode. In this mode the CPU has stopped and its current is significantly lower compared to other modes of operation. Using the $\overline{FCCM}$ pin simplifies control of converter modes of operation and increases the efficiency.

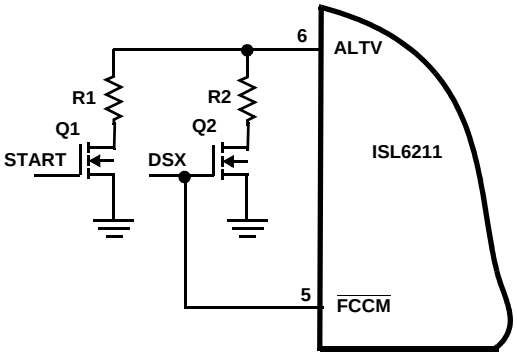


FIGURE 10. CONFIGURATION FOR HYSTERETIC OPERATION IN DSX MODE ONLY

Gate Control Logic

The gate control logic translates generated PWM signals into gate drive signals providing necessary amplification, level shift and shoot-through protection. It helps optimize the IC performance over a wide range of the operational conditions. As MOSFET switching time can very dramatically from type to type and with input voltage, the gate control logic provides adaptive dead time by monitoring the actual gate voltages of both the upper and the lower MOSFETs.

Feedback Loop Compensation

Due to the implemented current mode control, the modulator has a single pole response with -1 slope at frequency determined by load ,

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O}$$

where Ro is load resistance, Co is load capacitance. For this type of modulator Type 2 compensation circuit is usually sufficient. To reduce number of external components and remove the burden of determining compensation components from the system designer, the PWM controller has an internally compensated error amplifier.

The Figure 11 shows a Type 2 amplifier and its response along with the responses of a current mode modulator and of the converter. The Type 2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 6kHz$$

$$F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 600kHz$$

This region is also associated with phase ‘bump’ or reduced phase shift. The amount of phase shift reduction depends on how wide the region of flat gain is and has a maximum value of 90 degrees. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of V_{IN} to the oscillator ramp.

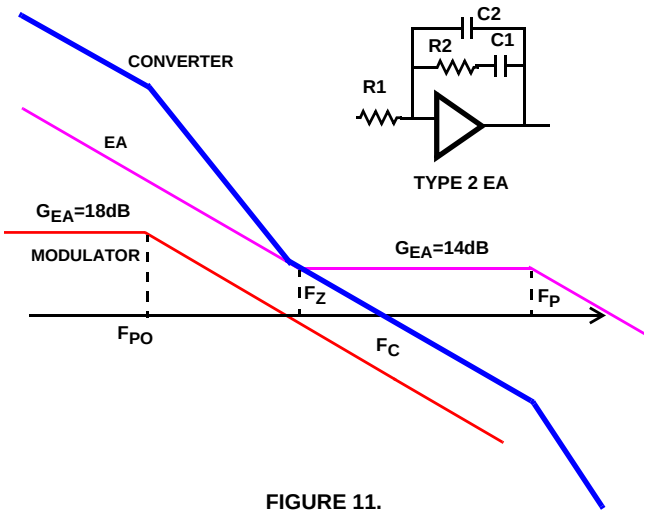


FIGURE 11.

The zero frequency, the amplifier high-frequency gain and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10kHz...50kHz range gives some additional phase ‘boost’.

Protections

The converter output is monitored and protected against extreme overload, short circuit, over-voltage and under-voltage conditions.

A sustained overload on the output sets the PGOOD pin low and latches-off the whole chip. The controller operation can be restored by cycling the VCC voltage or enable (EN) pin.

Over-Current Protection

The converter uses the lower MOSFET's on-resistance, $R_{DS(ON)}$, to monitor the current for protection against shorted outputs. The sensed current from the ISEN pin is compared with a current set by a resistor connected from the OCSET pin to the ground,.

$$R_{OCSET} = \frac{11.2V \bullet (R_{CS} + 100\Omega)}{I_{OC} \bullet R_{DS(ON)}}$$

Where, I_{OC} is a desired over-current protection threshold and R_{CS} is the value of the current sense resistor connected to the I_{SEN} pin.

If the lower MOSFET current exceeds the over-current threshold, a pulse skipping circuit is activated. The upper MOSFET will not be turned on as long as the sensed current is higher then the threshold value. This limits the current supplied by the DC voltage source. This condition keeps on for eight clock cycles after the over-current comparator was tripped for the first time. If after these first eight clock cycles the current exceeds the over-current threshold again in a time interval of another eight clock cycles, the overcurrent protection latches and disables the chip. If the over-current condition goes away during the first eight clock cycles, normal operation is restored and the over-current circuit resets itself sixteen clock cycles after the over-current threshold was exceeded the first time, Figure 12.

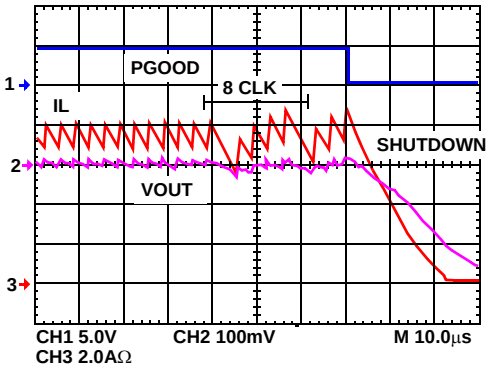


FIGURE 12. OVER-CURRENT PROTECTION WAVEFORMS

If the load step is strong enough to pull output voltage lower than the under-voltage threshold, the chip shuts down immediately.

Because of the nature of the current sensing technique, and to accommodate wide range of the $R_{DS(ON)}$ variation, the value of the over-current threshold should represent overload current about 150%...180% of the nominal value. If accurate current protection is desired, current sense resistor placed in series with the lower MOSFET source can optionally be used.

Over-Voltage Protection

Should the output voltage increase over 1.9V due to an upper MOSFET failure, or for other reasons, the over-voltage protection comparator will force the synchronous rectifier gate driver high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a 'soft' crowbar function which helps to tackle severe load transients and does not invert the output voltage when activated -- a common problem for OVP schemes with a latch.

Over-Temperature Protection

The chip incorporates an over temperature protection circuit that shuts the chip down when a die temperature of $150^{o}C$ is reached. Normal operation is restored at die temperature below $125^{o}C$ with a full soft-start cycle.

Design Procedure and Component Selection Guidelines

As an initial step, define operating voltage range and minimum and maximum load currents for the controller.

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current somewhere from 10% to 25% of the nominal current. At light load, the controller can automatically switch to hysteretic mode of operation to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor.

$$\Delta I = 2 \cdot I_{min}$$

$$\Delta I = \frac{\Delta Vout}{ESR}$$

$$L = \frac{Vin - Vout}{Fs \times \Delta I} \times \frac{Vout}{Vin}$$

MOSFET Selection and Considerations

Requirements for the upper and lower MOSFETs are different in mobile applications. The reason for that is the 10:1 difference in conduction time of the lower and the upper MOSFETs driven by a difference between the input voltage which is nominally in the range from 8V to 20V, while nominal output voltage is usually lower than 1.5V.

Requirements for the lower MOSFET are simpler than those to the upper one. The lower the Rdson of this device, the lower the conduction losses, the higher the converter's efficiency. Switching losses and gate drive losses are not significant because of zero-voltage switching conditions inherent for this device in the buck converter. Low reverse recovery charge of the body diode is important because it causes shoot-trough current spikes when the upper MOSFET turns on. Also, important is to verify that the lower MOSFET gate voltage does not reach threshold when high dV/dt transition occurs on the phase node. To minimize this effect, ISL6211 has a low, 0.8Ω typical, pull-down resistance of the synchronous rectifier driver.

Requirements for the upper MOSFET Rdson are less stringent than for the lower MOSFET because its conduction time is significantly shorter and switching losses are predominant especially at higher input voltages. It is recommended to have approximately equal conduction losses in the lower MOSFET and the switching losses in the upper MOSFET at the nominal input voltage and load current. Then the maximum of the converter efficiency is tuned to the operating point where it is most desired. Also, this provides the most cost effective solution.

Precise calculation of power dissipation in the MOSFETs is very complex because many parameters affecting turn-on and turn-off times such as gate reverse transfer charge, gate internal resistance, body diode reverse recovery charge, package and layout impedances and their variation with the operation conditions are not available to a designer. The following equations are provided only for rough estimation of the power losses and should be accompanied by a detailed breadboard evaluation. Attention should be paid to the input voltage extremes where power dissipation in the MOSFETs is usually higher.

$$Pupper = \frac{Io^2 \times Rdson \times Vout}{Vin} + \frac{Io \times Vin \times Fs \times (ton + toff)}{2}$$

$$Plower = Io^2 \times Rdson \times \left(1 - \frac{Vout}{Vin}\right)$$

Table 2 provides some component information for several typical applications. Applications 2 and 3 intended for CPUs other than Transmeta's Crusoe.

TABLE 2.

COMPONENT	APPLICATION 1	APPLICATION 2	APPLICATION 3
Maximum CPU Current	6.0A	12.0A	18.0A
Inductor	1.8µH Sumida CEP1231R8MH	1.0µH Panasonic ETQP6F1R0BFA	0.8µH Panasonic ETQP6F0R8BFA
Output Capacitor	4x220µF Sanyo POSCAP 2R5TPC220M or 3x270µF Panasonic EEFUE0271R	6x220µF Sanyo POSCAP 2R5TPC220M or 5x270µF Panasonic EEFUE0271R	6x270µF Panasonic EEFUE0D271R
High-Side MOSFET	uPA1707	HUF76112SK8	2x HUF76112SK8
Low-Side MOSFET	uPA1707	2x ITF86130SK8T	2x ITF86130SK8T
Current-Input Resistor for ~3% Droop	3.57kΩ	2.80kΩ	3.00kΩ

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor it filters the sequence of pulses produced by the switcher, and it supplies the load transient currents. The filtering requirements are a function of the switching frequency and the ripple current allowed, and are usually easy to satisfy in high frequency converters.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. Modern microprocessors produce transient load rates in excess of 10A/µs. High frequency ceramic capacitors placed beneath the processor socket initially supply the transient and reduce the slew rate seen by the bulk capacitors. The bulk capacitor values are generally determined by the total allowable ESR rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the processor power pins as physically possible. Consult with the processor manufacturer for specific decoupling requirements. Use only specialized low-ESR electrolytic capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a transient. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current which could cause substantial ringing and be a source of EMI pollution if layout constrains are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and are noise generators. The low power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller island of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing such as PHASE, UGATE and LGATE, for example. All surrounding circuitry will tend to couple the noise from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces. It is not recommended to use High Density Interconnect Systems, or micro-vias on these signals. The use of blind or buried vias should be limited to the low current signals only. The use of normal thermal vias is left to the discretion of the designer.

Keep the wiring traces from the control IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like the soft-start capacitor and current sense resistors as close as possible to the respective pins of the IC.

The ISL6211 utilizes advanced packaging technology that will have lead pitch of 0.6mm. High performance analog semiconductors utilizing narrow lead spacing may require special considerations in PWB design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices. It is not recommended to use any type of rosin or acid core solder, or the use of flux in either the manufacturing or touch up process as these may contribute to corrosion or enable electromigration and/or eddy currents near the sensitive low current signals. When chemicals such as these are used on or near the PWB, it is suggested that the entire PWB be cleaned and dried completely before applying power.

ISL6211 DC-DC Converter Application Circuit

The Figure 13 shows an application circuit of a power supply for a notebook PC. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9989. Also see Intersil's web site (www.intersil.com) for the latest information.

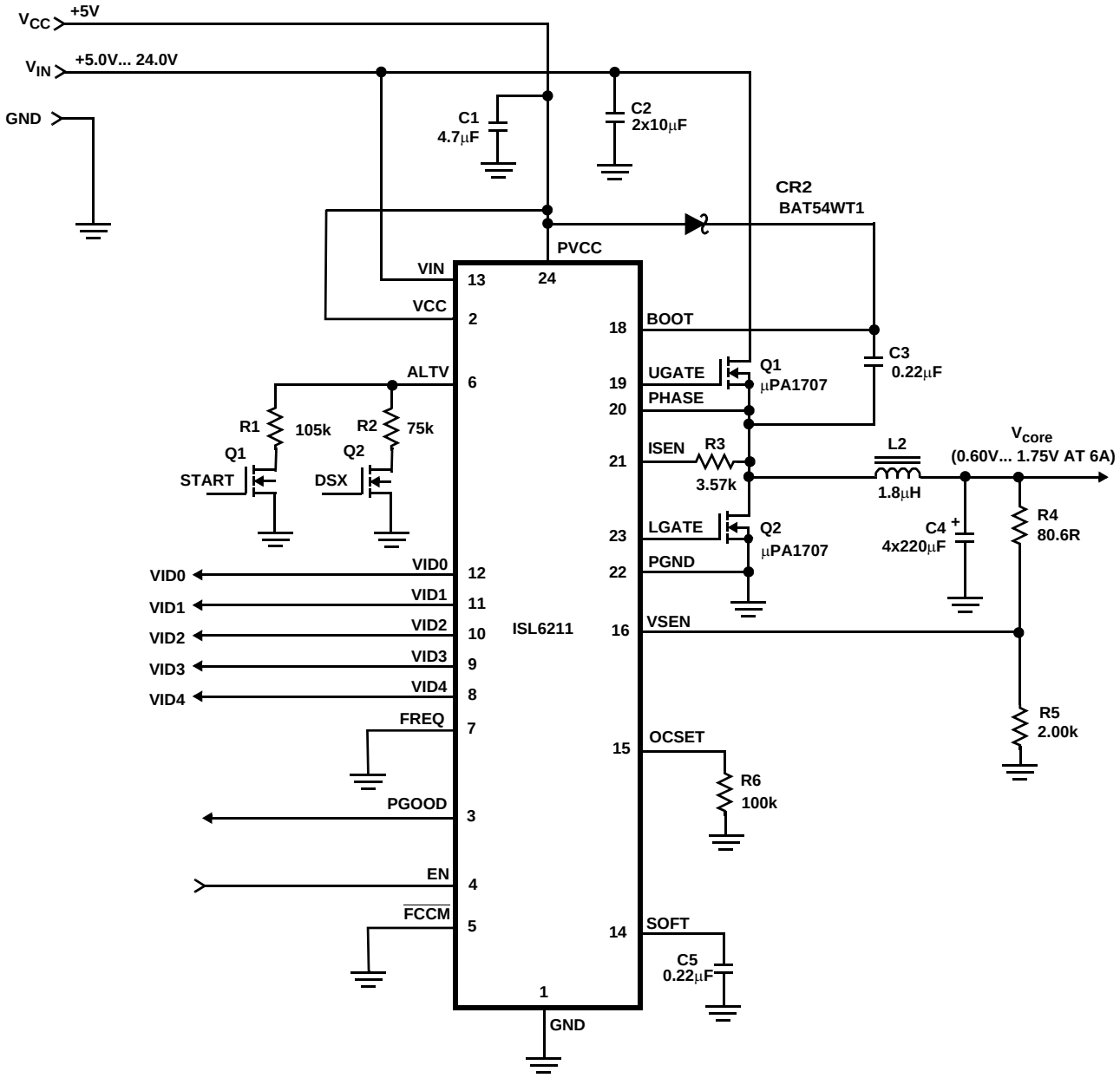
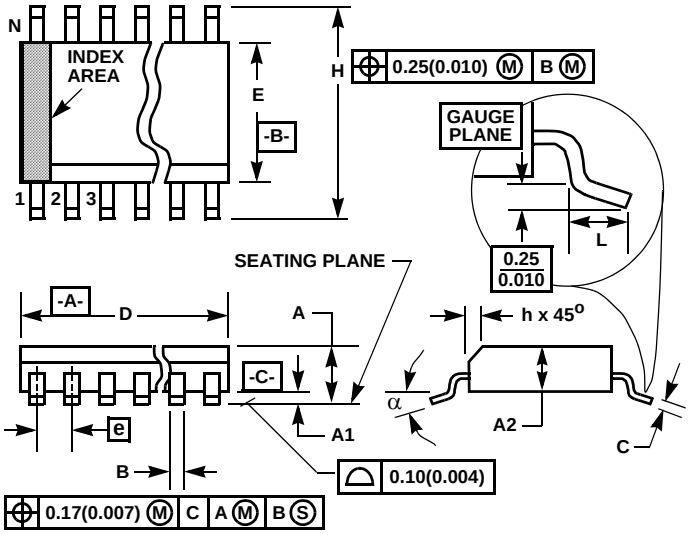


FIGURE 13. APPLICATION CIRCUIT

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M24.15

24 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.55	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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