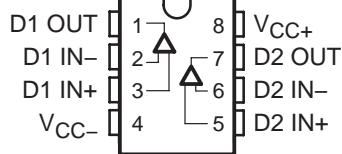


THS6052, THS6053 175 mA, ± 12 V ADSL CPE LINE DRIVERS

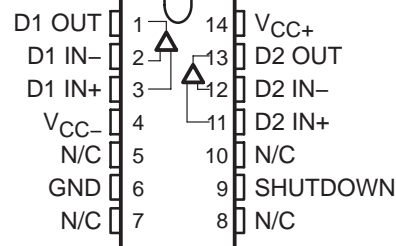
SLOS293D – JUNE 2000 – REVISED DECEMBER 2001

- **Remote Terminal ADSL Line Driver**
 - Ideal for Both Full Rate ADSL and G.Lite
 - Compatible With 1:1 Transformer Ratio
- **Low 2.7 pA/ $\sqrt{\text{Hz}}$ Noninverting Current Noise**
 - Reduces Noise Feedback Through Hybrid Into Downstream Channel
- **Wide Supply Voltage Range ± 5 V to ± 15 V**
 - Ideal for ± 12 -V Operation
- **Wide Output Swing**
 - 42 Vpp Differential Output Voltage, $R_L = 200 \Omega$, ± 12 -V Supply
- **High Output Current**
 - 175 mA (typ)
- **High Speed**
 - 110 MHz (-3 dB, $G=8$, ± 12 V)
 - 1500 V/ μs Slew Rate ($G = 8$, ± 12 V)
- **Low Distortion, Single-Ended, $G = 8$**
 - -83 dBc (250 kHz, 2 Vpp, 100- Ω load)
- **Low Power Shutdown (THS6053)**
 - 300- μA Total Standby Current
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6052
SOIC (D) AND
SOIC PowerPAD™ (DDA) PACKAGE
(TOP VIEW)

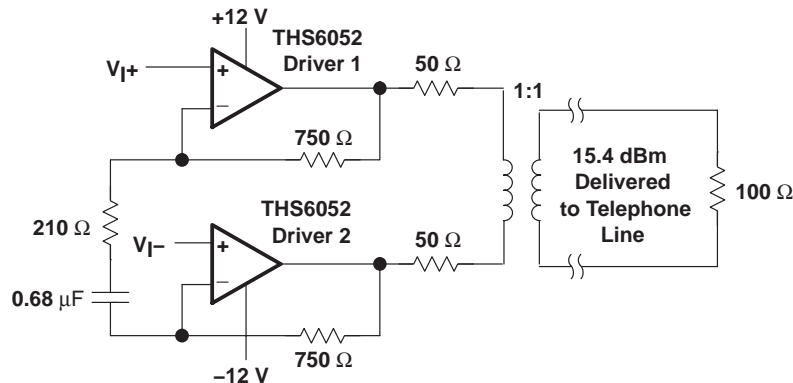


THS6053
SOIC (D) AND
TSSOP PowerPAD™ (PWP) PACKAGE
(TOP VIEW)



description

The THS6052/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from ± 12 -V supply voltages while drawing only 5.2 mA of supply current per channel. It offers low -83 dBc total harmonic distortion driving a 100- Ω load (2 Vpp). The THS6052/3 offers a high 42-Vpp differential output swing across a 200- Ω load from a ± 12 -V supply. The THS6053 features a low-power shutdown mode, consuming only 300 μA quiescent current per channel. The THS6052/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ packages.



RELATED PRODUCTS

DEVICE	DESCRIPTION
THS6042/3	350-mA, ± 12 V ADSL CPE line driver
THS6092/3	275-mA, +12 V ADSL CPE line driver
OPA2677	380-mA, +12 V ADSL CPE line driver
THS6062	Low noise ADSL receiver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

THS6052, THS6053 175 mA, ±12 V ADSL CPE LINE DRIVERS

SLOS293D – JUNE 2000 – REVISED DECEMBER 2001

AVAILABLE OPTION

T _A	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8 (D)	SOIC-8 PowerPAD (DDA)	SOIC-14 (D)	TSSOP-14 (PWP)	
0°C to 70°C	THS6052CD	THS6052CDDA	THS6053CD	THS6053CPWP	THS6052EVM THS6053EVM
-40°C to 85°C	THS6052ID	THS6052IDDA	THS6053ID	THS6053IPWP	—

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{CC+} to V _{CC-}	33 V
Input voltage	± V _{CC}
Output current (see Note 1)	275 mA
Differential input voltage	± 4 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T _A : Commercial	0°C to 70°C
Industrial	-40°C to 85°C
Storage temperature, T _{stg} : Commercial	-65°C to 125°C
Industrial	-65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6052 and THS6053 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	θ _{JA}	θ _{JC}	T _A = 25°C T _J = 150°C POWER RATING
D-8	95°C/W‡	38.3°C/W‡	1.32 W
DDA	45.8°C/W‡	9.2°C/W‡	2.73 W
D-14	66.6°C/W‡	26.9°C/W‡	1.88 W
PWP	37.5°C/W	1.4°C/W	3.3 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is 168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC+} to V _{CC-}	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T _A	C-suffix	0		70	°C
	I-suffix	-40		85	



electrical characteristics over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_{FEEDBACK} = 750\ \Omega$, $R_L = 100\ \Omega$ (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	$R_L = 50\ \Omega$	G= 1, $R_F = 1\ \text{k}\Omega$	$V_{CC} = \pm 5\ \text{V}$	110		MHz
				$V_{CC} = \pm 12\ \text{V}$	120		
			G= 2, $R_F = 680\ \Omega$	100			
				G= 8, $R_F = 330\ \Omega$	$V_{CC} = \pm 5\ \text{V}, \pm 12\ \text{V}$		
		$R_L = 100\ \Omega$	G= 1, $R_F = 1\ \text{k}\Omega$		$V_{CC} = \pm 5\ \text{V}$	150	
				$V_{CC} = \pm 12\ \text{V}$	170		
			G= 2, $R_F = 680\ \Omega$	135			
				G= 8, $R_F = 330\ \Omega$	$V_{CC} = \pm 5\ \text{V}, \pm 12\ \text{V}$		
SR	Slew rate (see Note 2), G=8	$V_O = 4\ \text{V}_{PP}$	$V_{CC} = \pm 5\ \text{V}$		$V_{CC} = \pm 5\ \text{V}$	650	
			$V_{CC} = \pm 12\ \text{V}$	$V_{CC} = \pm 12\ \text{V}$	850		
			$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	950		
		$V_O = 16\ \text{V}_{PP}$	$V_{CC} = \pm 12\ \text{V}$	$V_{CC} = \pm 12\ \text{V}$	1500		
			$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	1700		
				$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	1700	

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion (single-ended configuration)	Gain = 8, $R_L = 100\ \Omega$, $V_{CC} = \pm 12\ \text{V}$, $f = 250\ \text{kHz}$	$V_O(pp) = 2\ \text{V}$	–83		dBc	
			$V_O(pp) = 16\ \text{V}$	–78			
		Gain = 8, $R_L = 50\ \Omega$, $V_{CC} = \pm 5\ \text{V}$, $f = 250\ \text{kHz}$	$V_O(pp) = 2\ \text{V}$	–74			
			$V_O(pp) = 6\ \text{V}$	–72			
V_n	Input voltage noise	$V_{CC} = \pm 5\ \text{V}$, $f = 10\ \text{kHz}$, $\pm 12\ \text{V}$		2.1		nV/ $\sqrt{\text{Hz}}$	
I_n	Input current noise	+Input	$f = 10\ \text{kHz}$, $V_{CC} = \pm 5\ \text{V}$, $V_{CC} = \pm 12\ \text{V}$, $V_{CC} = \pm 15\ \text{V}$	2.7		pA/ $\sqrt{\text{Hz}}$	
		–Input		10.7			
X_T	Crosstalk	$f = 250\ \text{kHz}$, G = 2, $R_L = 100\ \Omega$	$V_{CC} = \pm 12\ \text{V}$, $R_L = 100\ \Omega$	$V_O = 2\ \text{V}_{p-p}$	–79		dBc
		$f = 250\ \text{kHz}$, G = 2, $R_L = 50\ \Omega$	$V_{CC} = \pm 5\ \text{V}$, $R_L = 50\ \Omega$	$V_O = 2\ \text{V}_{p-p}$	–71		

THS6052, THS6053

175 mA, ±12 V ADSL CPE LINE DRIVERS

SLOS293D – JUNE 2000 – REVISED DECEMBER 2001

electrical characteristics over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_{\text{FEEDBACK}} = 750\ \Omega$, $R_L = 100\ \Omega$ (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Input offset voltage	V _{CC} = ±12 V, V _{CC} = ±6 V	T _A = 25°C	5	10	mV
			T _A = full range		15	
	Differential offset voltage		T _A = 25°C	3	6	
			T _A = full range		8	
Offset drift	T _A = full range		30	μV/°C		
I _{IB}	– Input bias current	V _{CC} = ±12 V, V _{CC} = ±6 V	T _A = 25°C	5	10	μA
			T _A = full range		12	
	+ Input bias current		T _A = 25°C	2	5	
			T _A = full range		6	
	Differential input bias current		T _A = 25°C	5	10	
T _A = full range			12			
Z _{OL}	Open loop transimpedance	V _{CC} = ±12 V, V _{CC} = ±6 V R _L = 1 kΩ,		1		MΩ

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{ICR}	Input common-mode voltage range	V _{CC} = ±12 V	±9.7	±10.1		V
		V _{CC} = ±6 V	±3.8	±4.2		
CMRR	Common-mode rejection ratio	V _{CC} = ±12 V, V _{CC} = ±6 V	T _A = 25°C	59	66	dB
			T _A = full range	57		
R _I	Input resistance	+ Input		1.5		MΩ
		– Input		15		Ω
C _I	Input capacitance			2		pF

output characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Output voltage swing	R _L = 50 Ω, V _{CC} = ±6 V		±4.2	±4.6	V
			R _L = 100 Ω		±10.1	
			V _{CC} = ±6 V	±4.4	±4.8	
I _O	Output current	R _L = 25 Ω, V _{CC} = ±12 V	150	175		mA
		R _L = 10 Ω, V _{CC} = ±6 V	150	175		
I _{SC}	Short-circuit current	R _L = 0 Ω, V _{CC} = ±12 V		250		mA
	Output resistance	Open loop		14		Ω



THS6052, THS6053

175 mA, ±12 V ADSL CPE LINE DRIVERS

SLOS293D – JUNE 2000 – REVISED DECEMBER 2001

electrical characteristics over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_{FEEDBACK} = 750\ \Omega$, $R_L = 100\ \Omega$ (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (each driver)	$V_{CC} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$		5.2	7	mA
			$T_A = \text{full range}$			8	
		$V_{CC} = \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$		4.5	6.5	
			$T_A = \text{full range}$			7.5	
PSRR	Power supply rejection ratio	$V_{CC} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	-64	-62		dB
			$T_A = \text{full range}$		-61	-	
		$V_{CC} = \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$	-60	-70		
			$T_A = \text{full range}$		-58		

shutdown characteristics (THS6053 only)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IL}(\text{SHDN})$	Shutdown pin voltage for power up	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$ GND = 0 V, (GND Pin as Reference)				0.8	V
$V_{IH}(\text{SHDN})$	Shutdown pin voltage for power down	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$, GND = 0 V, (GND Pin as Reference)		2			V
$I_{CC}(\text{SHDN})$	Total quiescent current when in shutdown state	$V_{GND} = 0\text{ V}$, $V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$			0.3	0.7	mA
t_{DIS}	Disable time (see Note 3)	$V_{CC} = \pm 12\text{ V}$			0.1		μs
t_{EN}	Enable time (see Note 3)	$V_{CC} = \pm 12\text{ V}$			0.4		μs
$I_{IL}(\text{SHDN})$	Shutdown pin input bias current for power up	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$			40	100	μA
$I_{IH}(\text{SHDN})$	Shutdown pin input bias current for power down	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$, $V(\text{SHDN}) = 3.3\text{ V}$			50	100	μA

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

THS6052, THS6053 175 mA, ± 12 V ADSL CPE LINE DRIVERS

SLOS293D – JUNE 2000 – REVISED DECEMBER 2001

APPLICATION INFORMATION

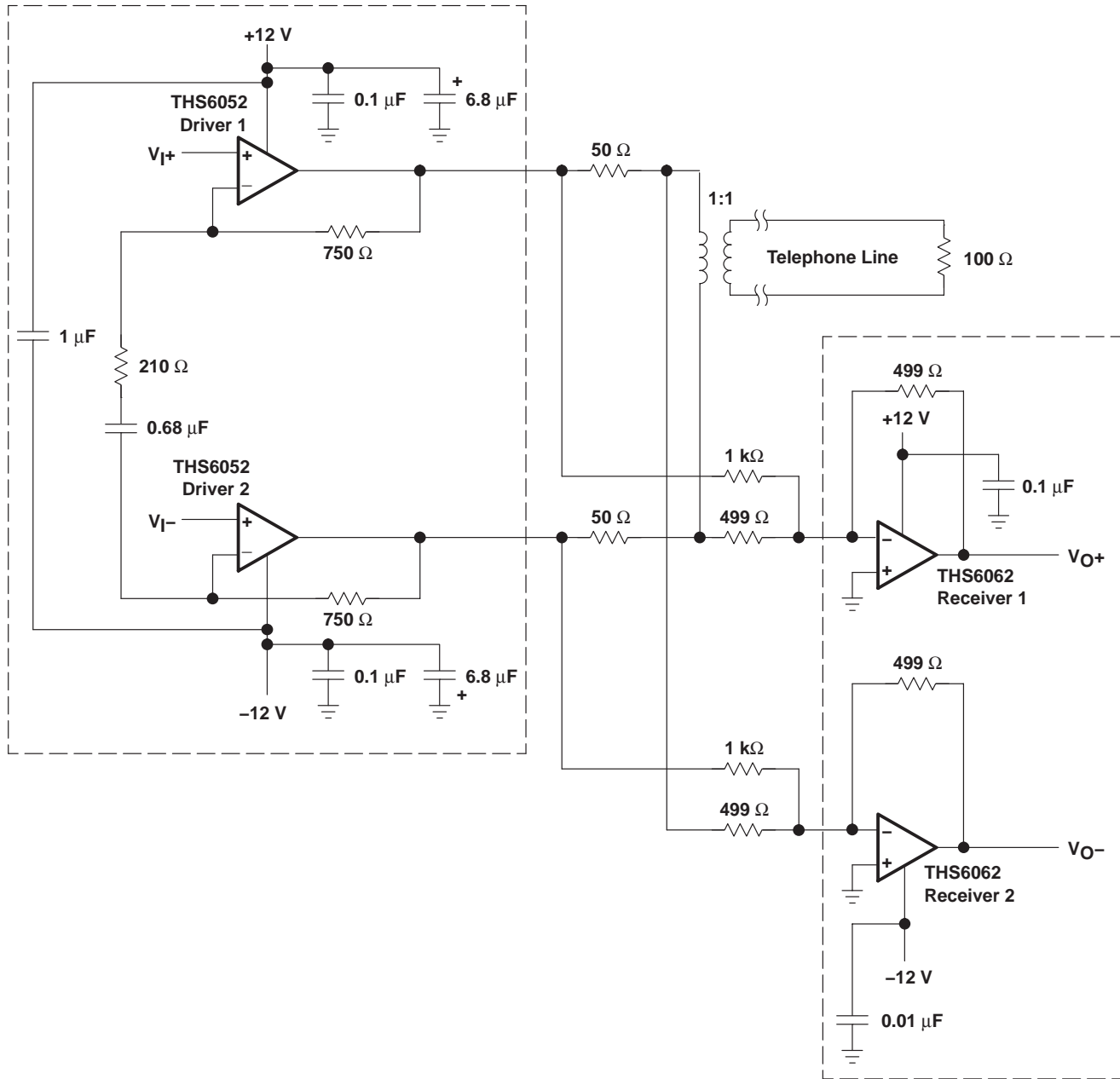


Figure 1. THS6052 ADSL Application With 1:1 Transformer Ratio

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6052CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	6052C	Samples
THS6052CDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	6052C	Samples
THS6052ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6052I	Samples
THS6052IDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	6052I	Samples
THS6052IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6052I	Samples
THS6053CPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6053C	Samples
THS6053ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS6053I	Samples
THS6053IPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6053I	Samples
THS6053IPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6053I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6053CPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

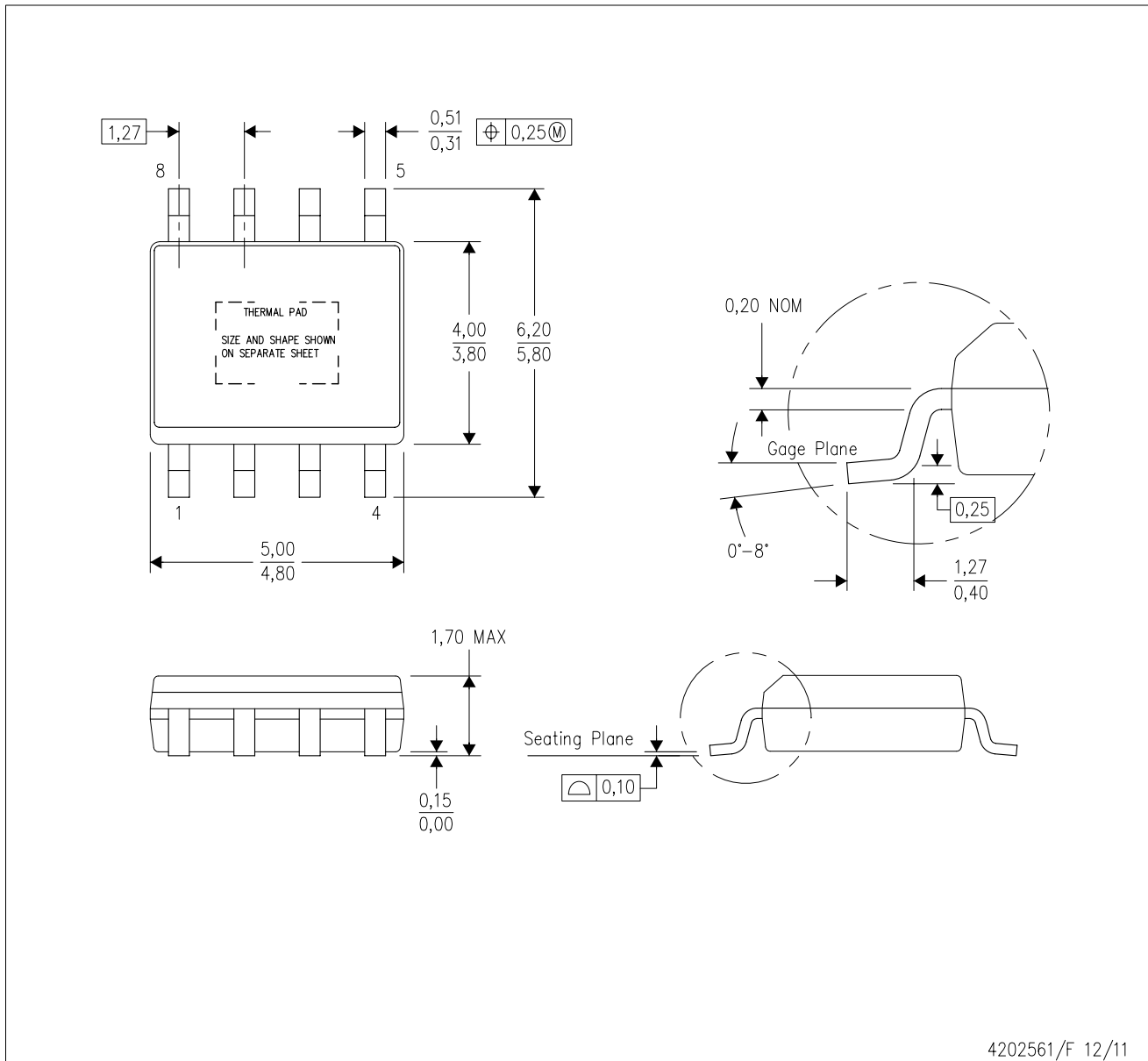


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6053CPWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

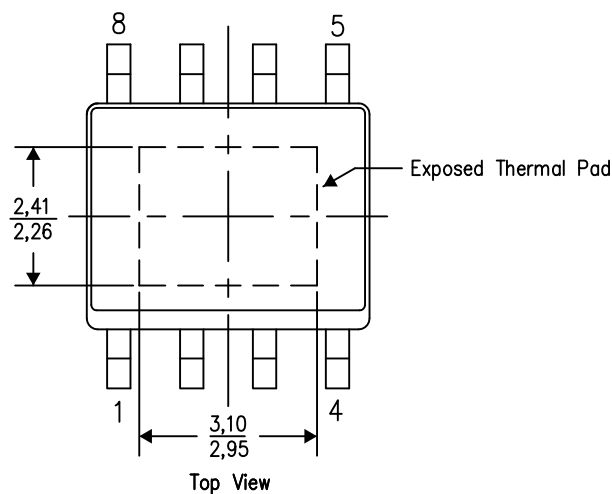
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

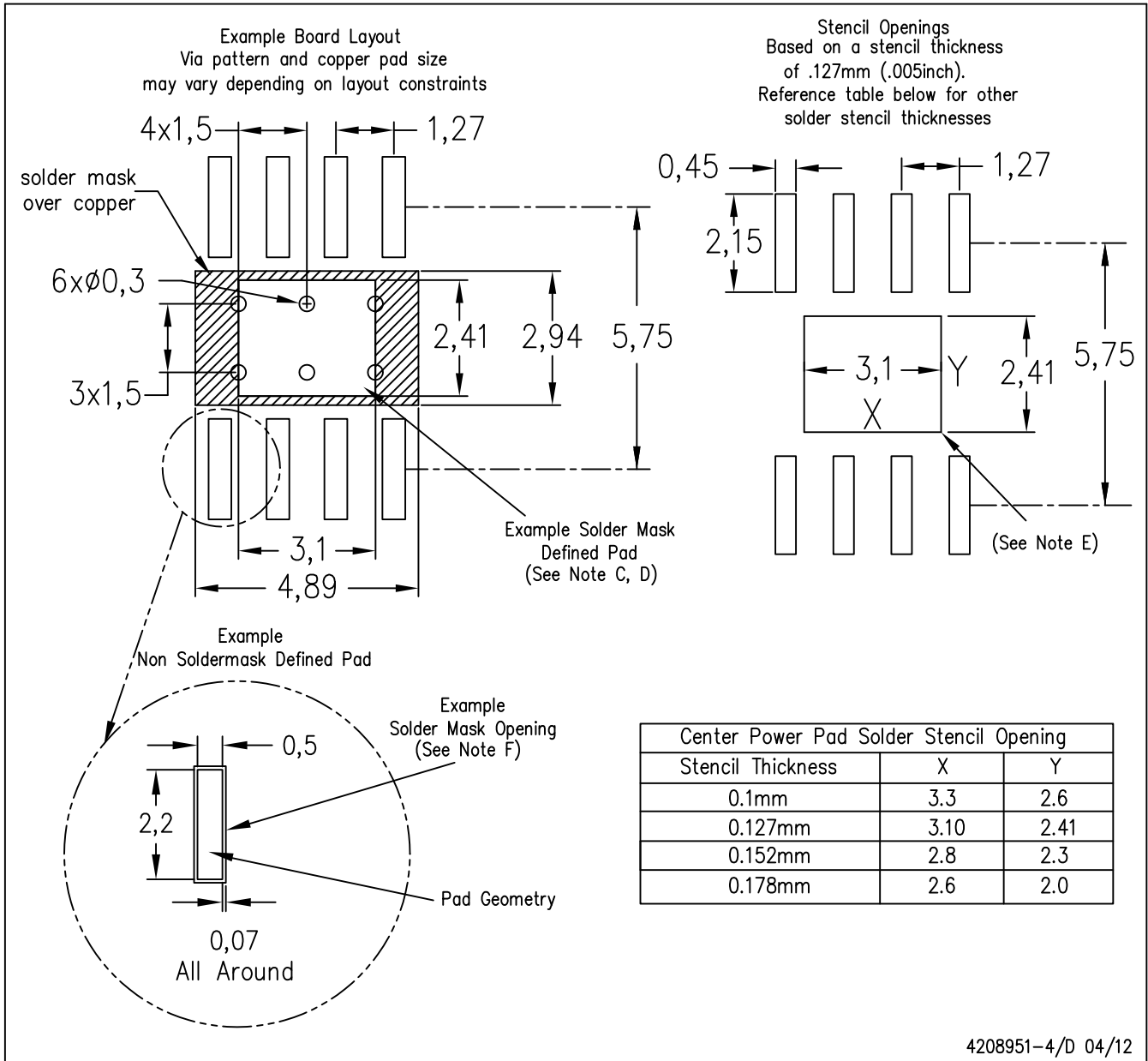


Exposed Thermal Pad Dimensions

4206322-4/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

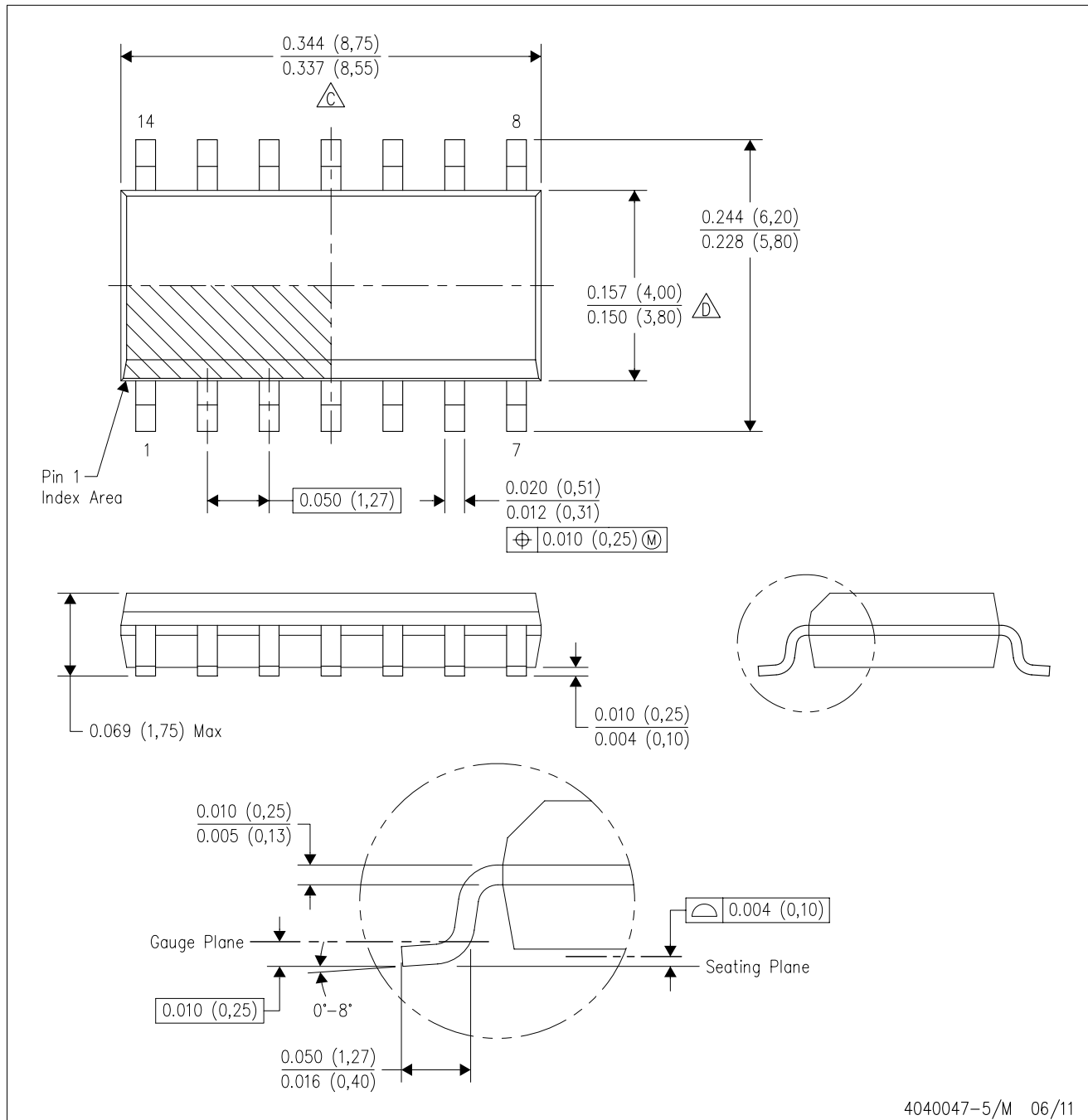


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

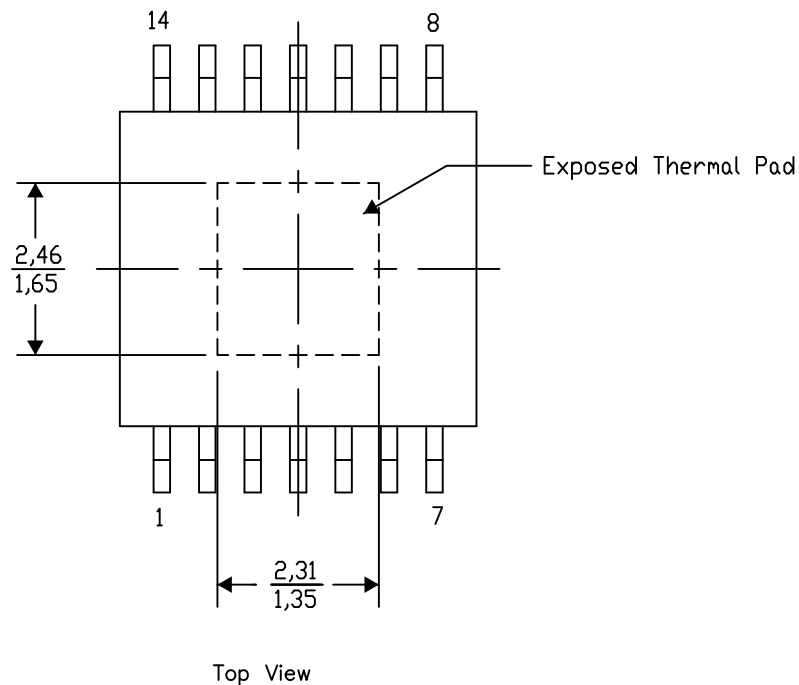
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



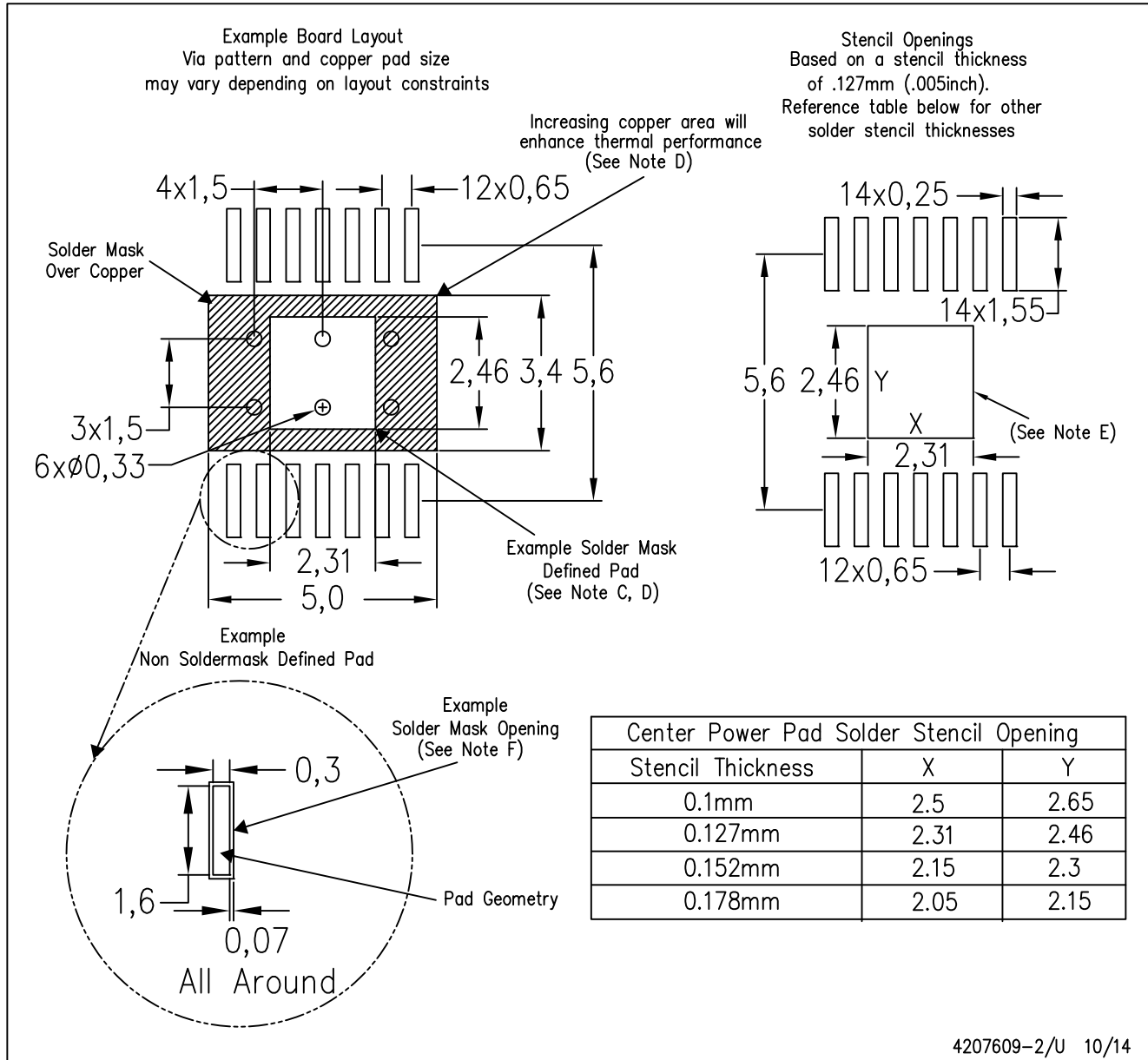
4206332-2/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

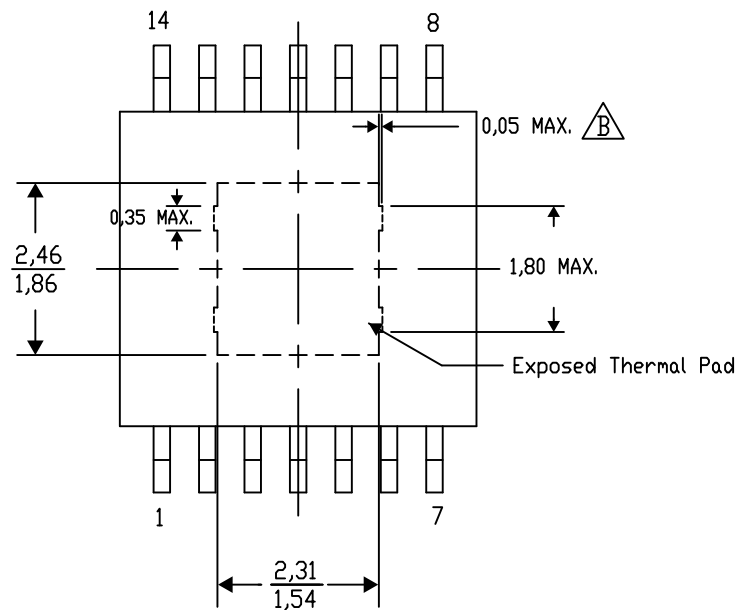
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206332-44/AJ 10/14

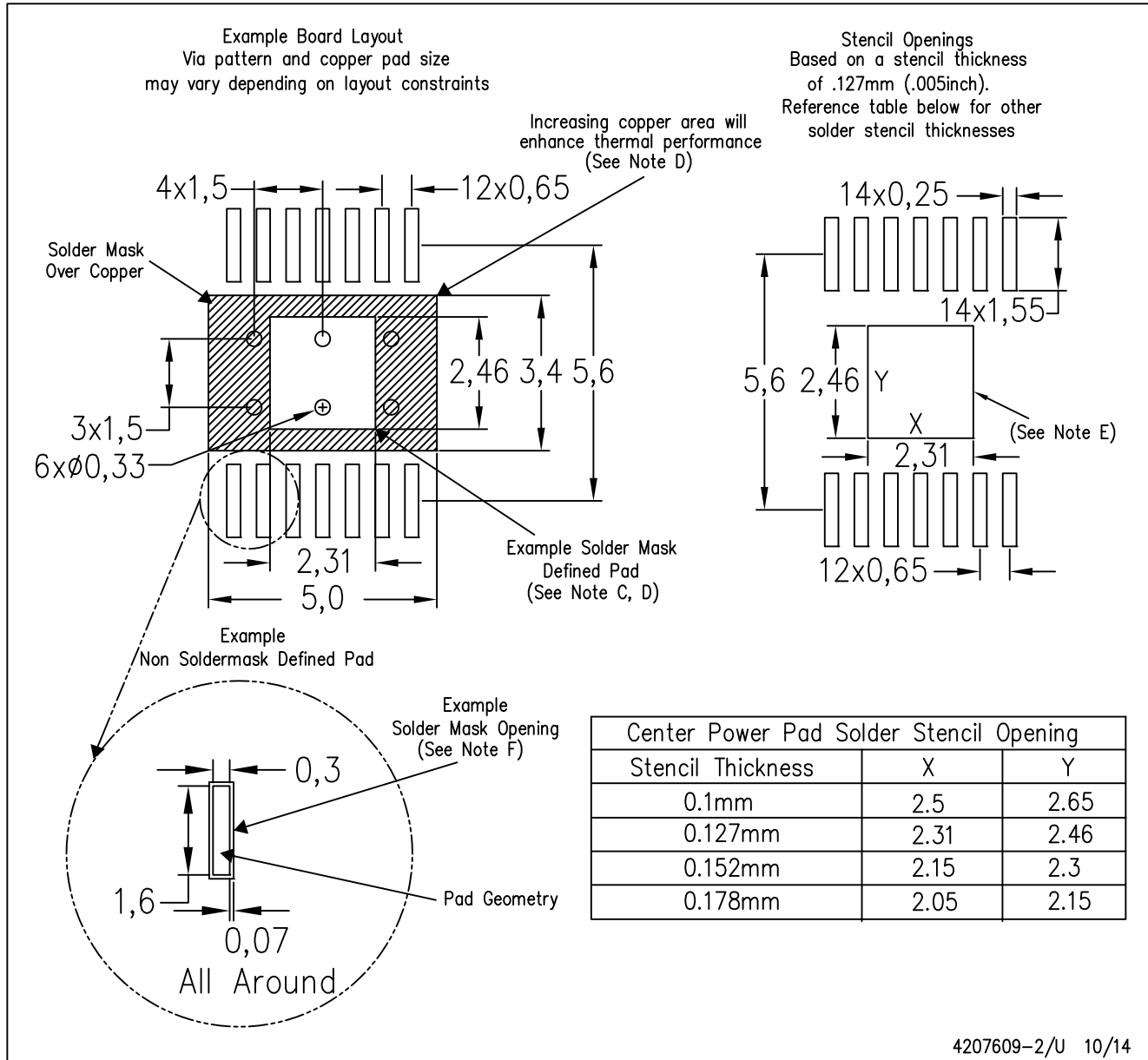
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-2/U 10/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com