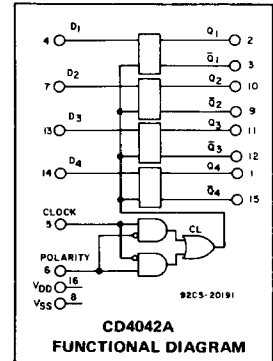


CMOS Quad Clocked "D" Latch

The RCA-CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical. Information present at the data input is transferred to outputs Q and \bar{Q} during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK MAXIMUM RATINGS, Absolute-Maximum Values:

and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition occurs.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



Features:

- Clock polarity control
- Q and \bar{Q} outputs
- Common clock
- Low power TTL compatible
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

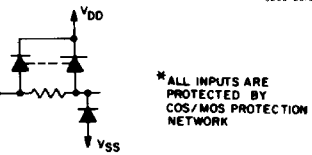
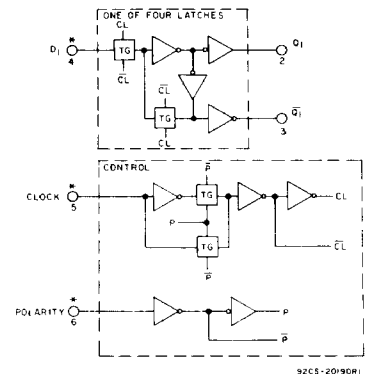
Applications:

- Buffer storage
- Holding register
- General digital logic

STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to +150°C
 OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPES D, F, K, H -55 to +125°C
 PACKAGE TYPE E -40 to +85°C
 DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (Voltages referenced to V_{SS} Terminal): -0.5 to +15 V
 POWER DISSIPATION PER PACKAGE (P_D):
 FOR $T_A = -40$ to +60°C (PACKAGE TYPE E) 500 mW
 FOR $T_A = +60$ to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K) 500 mW
 FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
 DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) 100 mW
 INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V
 LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ K Ω

CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	150	300	150	400	ns
	10	75	150	75	200	
Data In to \bar{Q}	5	250	500	250	600	ns
	10	100	200	100	250	
Clock to Q	5	300	600	300	750	ns
	10	125	250	125	300	
Clock to \bar{Q}	5	400	800	400	1000	ns
	10	175	350	175	400	
Transition Time: t_{THL}, t_{TLH}	5	100	200	100	300	ns
	10	50	100	50	150	
Minimum Clock Pulse Width, t_{W}	5	175	250	175	350	ns
	10	60	120	60	175	
Minimum Hold Time, t_H	5	150	300	150	350	ns
	10	60	120	60	150	
Minimum Setup Time, t_S	5	0	50	0	50	ns
	10	0	30	0	30	
Minimum Clock Rise or Fall Time: t_r, t_f	5	Not rise or fall time sensitive.				μ s
	10	Not rise or fall time sensitive.				
Input Capacitance, C_i (Any Input)	-	5	-	5	-	pF



CLOCK	POLARITY	Q
0	0	D
	0	LATCH
1	1	D
	1	LATCH

Fig. 1 - Logic block diagram & truth table.

CD4042A Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range)	—	3	12	3	12	V
Clock Pulse Width, t_W	5	350	—	250	—	ns
	10	175	—	120	—	
Setup Time, t_S	5	50	—	50	—	ns
	10	30	—	30	—	
Hold Time, t_H	5	350	—	300	—	ns
	10	150	—	120	—	
Clock Rise or Fall Time: t_r, t_f	5	Not rise or fall time sensitive.				μs
	10					

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures ($^\circ\text{C}$)								Units	
				D, F, K, H Packages				E Package					
				-55	+25		+125	-40	+25		+85		
Quiescent Device Current, I_L Max.	—	—	5		1	0.005			1	60		10	0.01
				2	0.005	2	120	20	0.02	20	280		
				25	0.25	25	1000	250	2.5	250	2500		
Output Voltage: Low-Level, V_{OL}	—	0, 5	10	0 Typ.; 0.05 Max.								V	
				0 Typ.; 0.05 Max.									
Output Voltage: High Level, V_{OH}	—	0, 5	10	4.95 Min.; 5 Typ.								V	
				9.95 Min.; 10 Typ.									
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V	
				9	—	10	3 Min.; 4.5 Typ.						
							1.5 Min.; 2.25 Typ.						
Noise Margin: Inputs Low, V_{NML}	4.5	—	5	1 Min.								V	
				9	—	10	1 Min.						
							1 Min.						
Output Drive Current: n-Channel (Sink), I_{DN} Min.	0.5	—	5	0.5	1	0.4	0.27	0.24	1	0.2	0.18	mA	
				1.25	2	1	0.7	0.6	2	0.5	0.45		
	0.5	—	10	-0.45	-1	-0.35	-0.25	-0.2	-1	-0.175	-0.15		
p-Channel (Source), I_{DP} Min.	4.5	—	5	-0.45	-1	-0.35	-0.25	-0.2	-1	-0.175	-0.15	mA	
				9.5	—	10	-1.15	-2	-0.9	-0.6	-0.34		-2
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input	15	$\pm 10^{-5}$ Typ.; 1 Max.								μA		

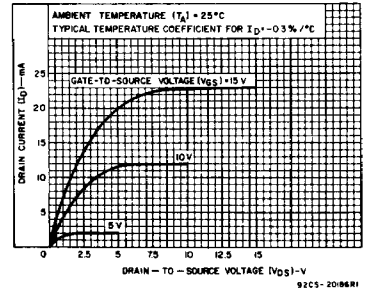


Fig. 2 — Typical output n-channel drain characteristics.

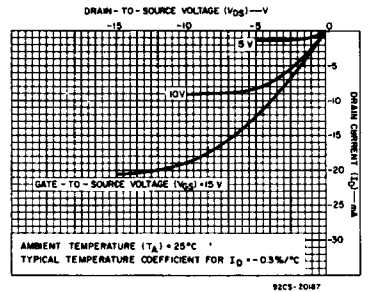


Fig. 3 — Typical output p-channel drain characteristics.

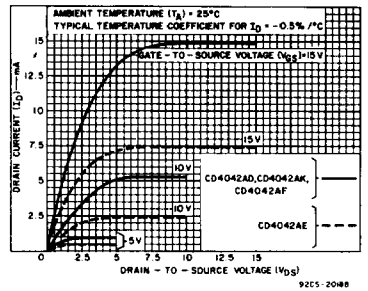


Fig. 4 — Minimum n-channel drain characteristics.

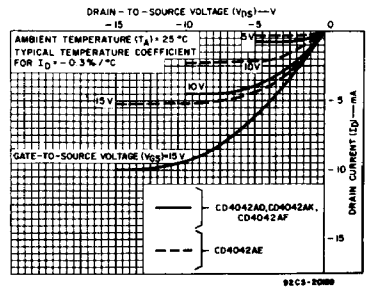
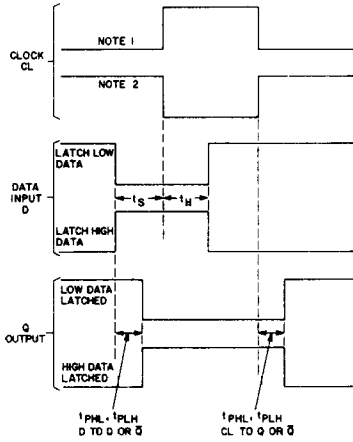


Fig. 5 — Minimum p-channel drain characteristics.



NOTES:
 1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW
 2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

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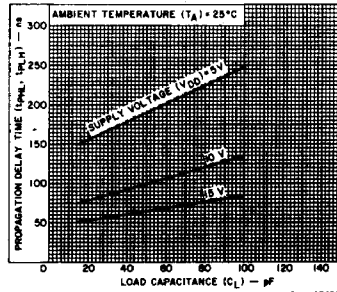


Fig. 7 - Typical propagation delay time vs. load capacitance - data to Q.

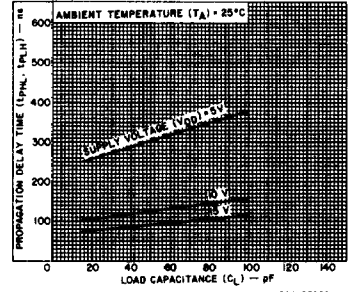


Fig. 8 - Typical propagation delay time vs. load capacitance - data to \bar{Q} .

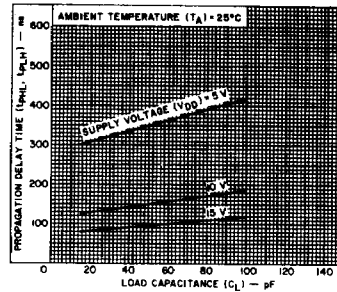


Fig. 9 - Typical propagation delay time vs. load capacitance - clock to Q.

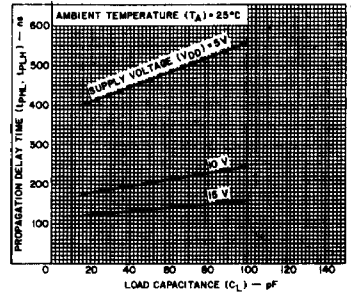


Fig. 10 - Typical propagation delay time vs. load capacitance - clock to \bar{Q} .

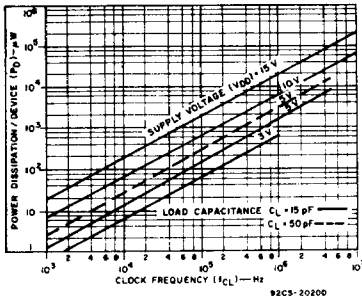


Fig. 11 - Typical dissipation characteristics.

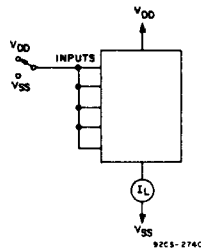


Fig. 12 - Quiescent device current test circuit.

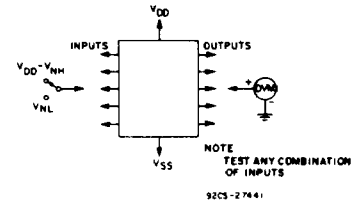


Fig. 13 - Noise immunity test circuit.

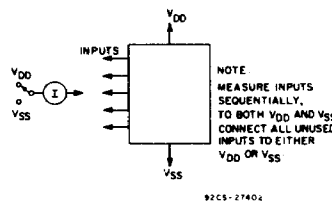


Fig. 14 - Input leakage current test circuit.