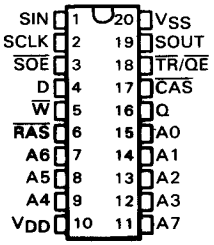
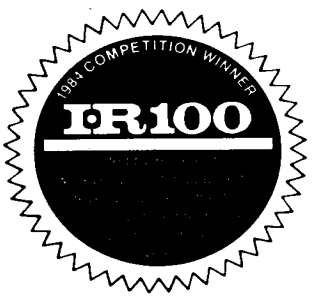
JUNE 1985 – REVISED FEBRUARY 1988

- MIL-STD-883C High-Reliability Processed and −55°C to 100°C (S Designator) Temperature Range, 20-Pin 300-Mil Ceramic Sidebrazed Package
- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q, and Address Lines to Simplify System Design
- Random-Access Port Looks Exactly Like a SMJ4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Supported by TI's Video System Controller (VSC)
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 240 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation (SMJ4161-15)
  - Operating . . . 250 mW (Typical)
  - Standby . . . 80 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Random-Access Data In
Q	Random-Access Data Out
$\overline{RAS}$	Row-Address Strobe
SCLK	Serial Data Clock
SIN	Serial Data In
$\overline{SOE}$	Serial Output Enable
SOUT	Serial Data Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable



description

The SMJ4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each, like the SMJ4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four cascaded 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One, two, three, or four 64-bit shift registers can be sequentially read out after a transfer cycle, depending on a two-bit code applied to the two most significant column address inputs. The SMJ4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4161 is offered in a 20-pin ceramic dual-in-line package. It is guaranteed for operation from $T_A = -55°C$ to $T_C = 100°C$. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

random access address space to sequential address space mapping

The SMJ4161 is designed with each row divided into four, 64-column sections (see functional block diagram). The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent binary 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11, only the most significant registers can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level 0 as $\overline{RAS}$ falls) a total of 256 bits can be sequentially read out.

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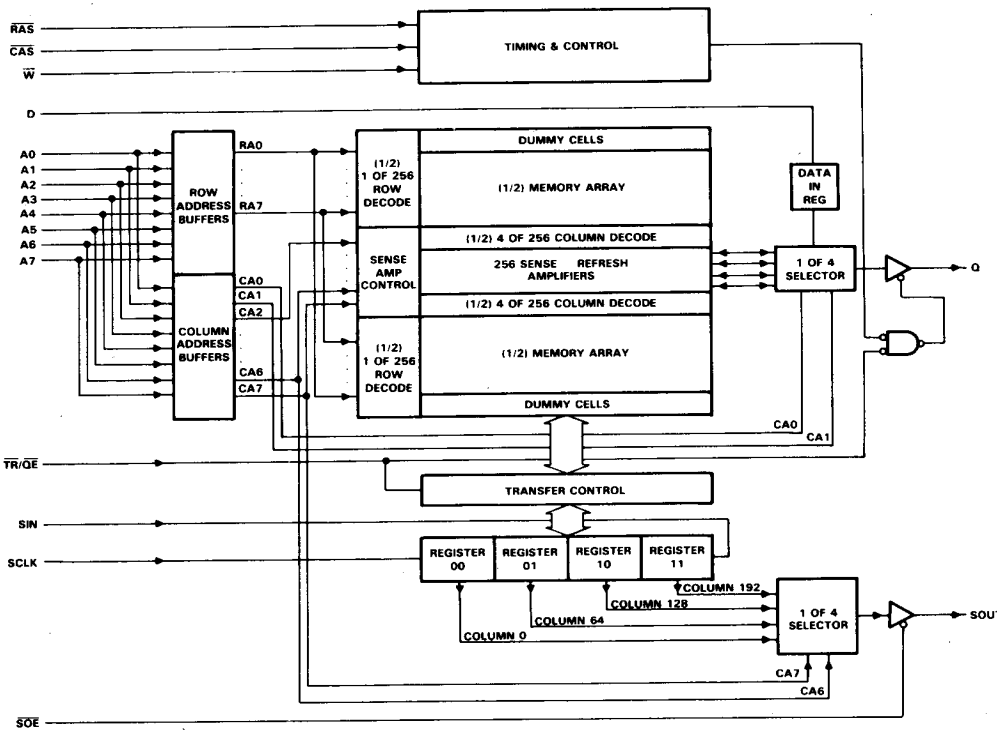
functional block diagram



random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, if this is a random-access operation, it functions as an output enable after CAS falls.

To use the SMJ4161 in the random-access mode, TR/QE must be high as RAS falls. Holding TR/QE high as RAS falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be transferred, the shift registers must be connected to the bit lines. Holding TR/QE low as RAS falls enables the 256 switches that connect the shift register to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever TR/QE is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output, making it possible to connect the address lines to the Q and D lines (use of this organization prohibits the use of the early write cycle).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatability (no pull-up resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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sequential access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift register are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and register address signals need not be supplied every cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though they were made of 256 rising edge D flip-flops connected D to Q. The SMJ4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The SMJ4161 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 6 ns after SCLK rises. These features make it possible to easily connect SMJ4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SCLK cycle time to allow manipulation of the serial data. If SOUT is connected to SIN, the SCLK cycle time must include $t_{su(SI)}$. When loading data into the shift register from the serial input in preparation for a shift-register-to-memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial output, allowing multiplexing of more than one bank of SMJ4161 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, SOUT will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, SOUT will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 100°C
Storage temperature range . . . . . −65°C to 150°C

†Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		V_{DD}+0.3	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	−55			°C
T_C	Operating case temperature			100	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4161-15			SMJ4161-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (Q, SOUT)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (Q, SOUT)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, Outputs = open			±10			±10	μA
I_O‡	Output current (leakage) (Q, SOUT)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls,§ SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		50	75		45	75	mA
I_{DD2}¶	Standby current	After 1 −$\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		16	25		16	25	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR}/\overline{QE}$ high, No load on Q and SOUT		42	60		37	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		45	75		40	75	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, No load on Q and SOUT, $t_{c(SCLK)}$ = $t_{c(SCLK)}$ min		30	45		30	45	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, No load on Q and SOUT		85	100		85	100	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡SOUT output current (leakage) is guaranteed but not tested.
§See appropriate timing diagram.
¶V_{IL} > −0.6 V.

capacitance over recommended supply voltage and operating temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4		pF
$C_{i(D)}$	Input capacitance, data input	4		
$C_{i(RC)}$	Input capacitance, strobe inputs	8		
$C_{i(W)}$	Input capacitance, write enable input	8		
$C_{i(CK)}$	Input capacitance, serial clock	8		
$C_{i(SI)}$	Input capacitance, serial in	4		
$C_{i(SOE)}$	Input capacitance, serial output enable	4		
$C_{i(TR)}$	Input capacitance, register transfer input	4		
$C_{o(Q)}$	Output capacitance, random-access data	5		
$C_{o(SOUT)}$	Output capacitance, serial out	5		

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS‡	ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low				40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = max, C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{RAS}$ high	C_L = 80 pF, I_{OL} = 4.2 mA, I_{OH} = −5 mA			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT				45		50	
$t_{a(SO)}$	Access time from SCLK				45		55	
$t_{dis(CH)}$	Q output disable time from $\overline{CAS}$ high		t_{OFF}		40		40	
$t_{dis(QE)}$	Q output disable time from $\overline{TR}/\overline{QE}$ high				30		40	
$t_{dis(SOE)}$	Serial output disable time from $\overline{SOE}$ high				20		25	

‡Figure 1 shows the load circuit; C_L values shown are typical for test system used.

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timing requirements over recommended supply voltage range and operating temperature range

PARAMETER		ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	265		330		ns
$t_{c(SCLK)}$	Serial clock cycle time (see Note 4)	t_{SCC}	45	50,000	55	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low¶	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low#	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low‖		20		20		ns
$t_{w(CKH)}$	Pulse duration, SCLK high‖		20		20		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		50		50		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	5		5		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		5		5		ns
$t_{su(SI)}$	Serial data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial data in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns

Continued next page.

NOTES: 4. $t_{c(SCLK)}$ min is tested by connecting SIN to SOUT and test conditions include $t_{su(SI)}$; see paragraph entitled SIN and SOUT on page 5.

5. Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

6. System transition times (rise and fall) for $\overline{RAS}$, $\overline{CAS}$, and SCLK are to be a minimum of 3 ns and a maximum of 50 ns.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 1-μs $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

¶In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

#In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

‖This parameter is guaranteed but not tested.

timing requirements over recommended supply voltage range and operating temperature range (concluded)

PARAMETER		ALT. SYMBOL	SMJ4161-15		SMJ4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial data out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low‖		30		30		ns
$t_{h(SO)}$	Serial data out hold time after SCLK high		6		6		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (tansfer)		40		40		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time $\overline{CAS}$ low to QE high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		75		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to QE low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80		80		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	135		150		ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low☆		10		10		ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register□	t_{REF2}		50,000		50,000	ns

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

‖ This parameter is guaranteed but not tested.

☆SCLK may be high or low during $t_{w(RL)}$, but there cannot be any positive edge transitions on SLCK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

□See "refresh" on page 5.

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PARAMETER MEASUREMENT INFORMATION

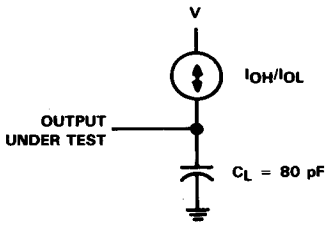
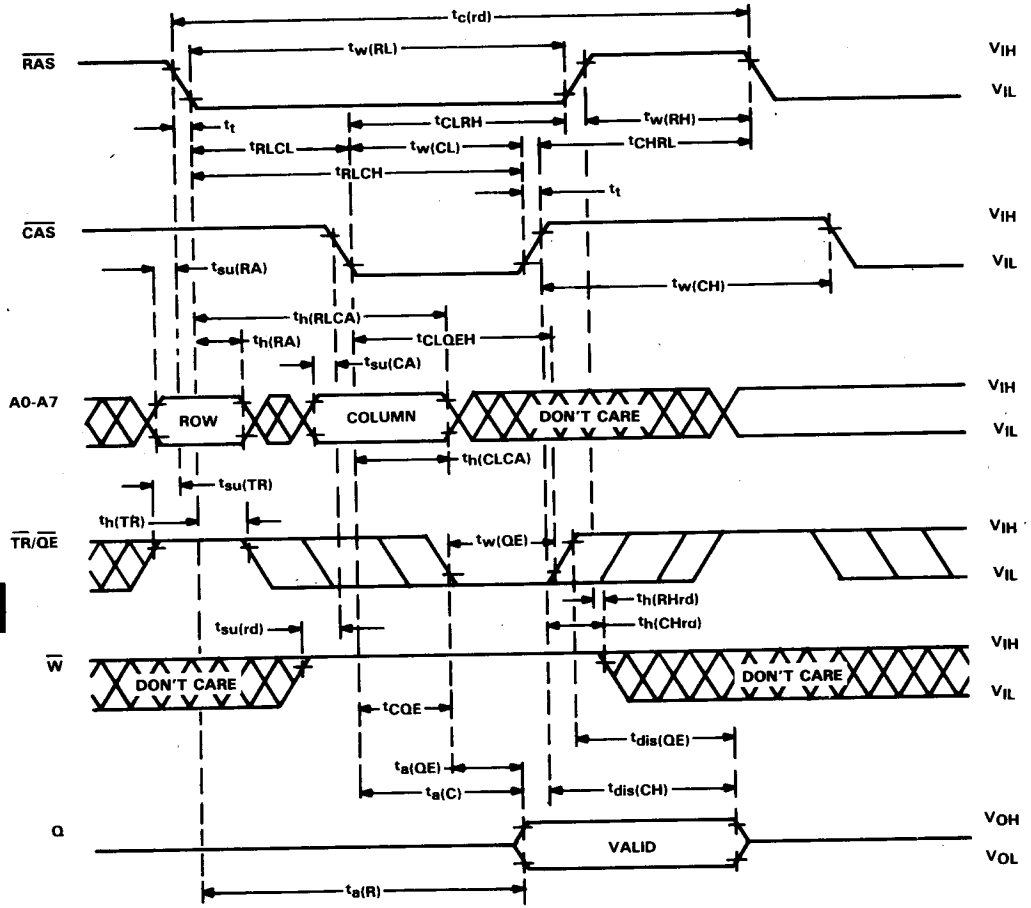


FIGURE 1. EQUIVALENT LOAD CIRCUIT

read cycle timing



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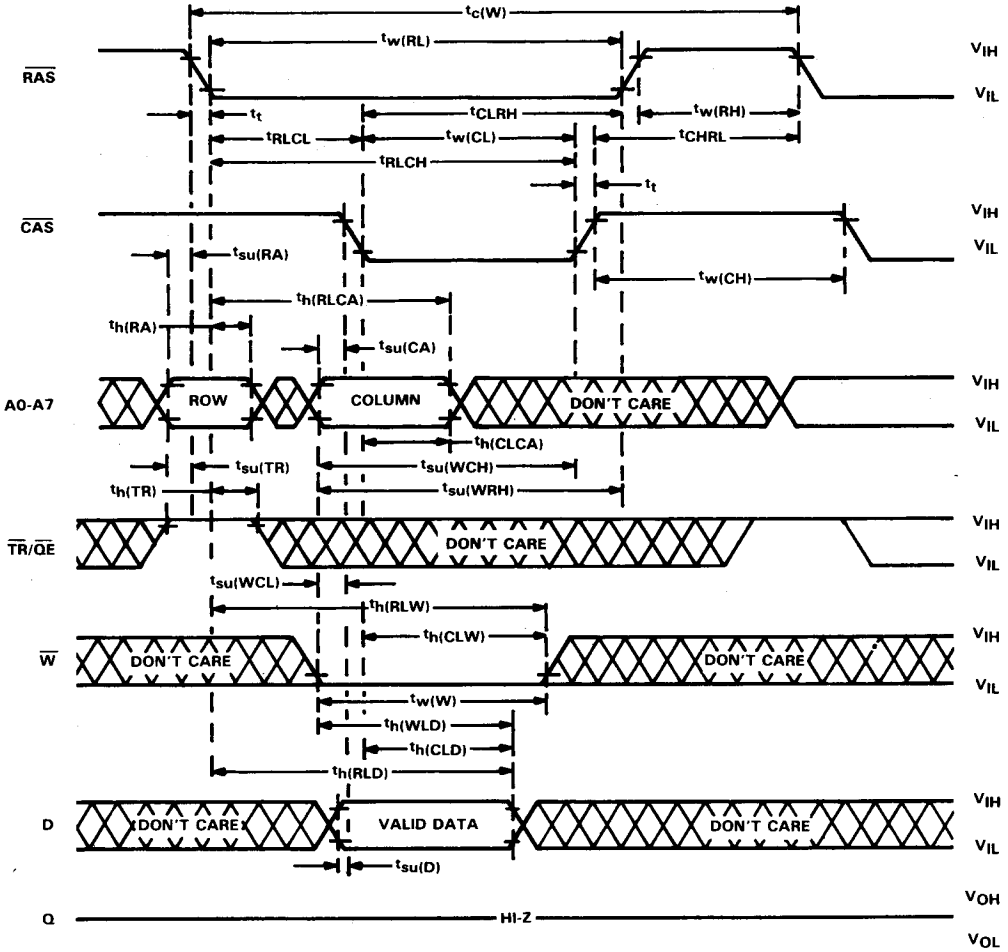
early write cycle timing



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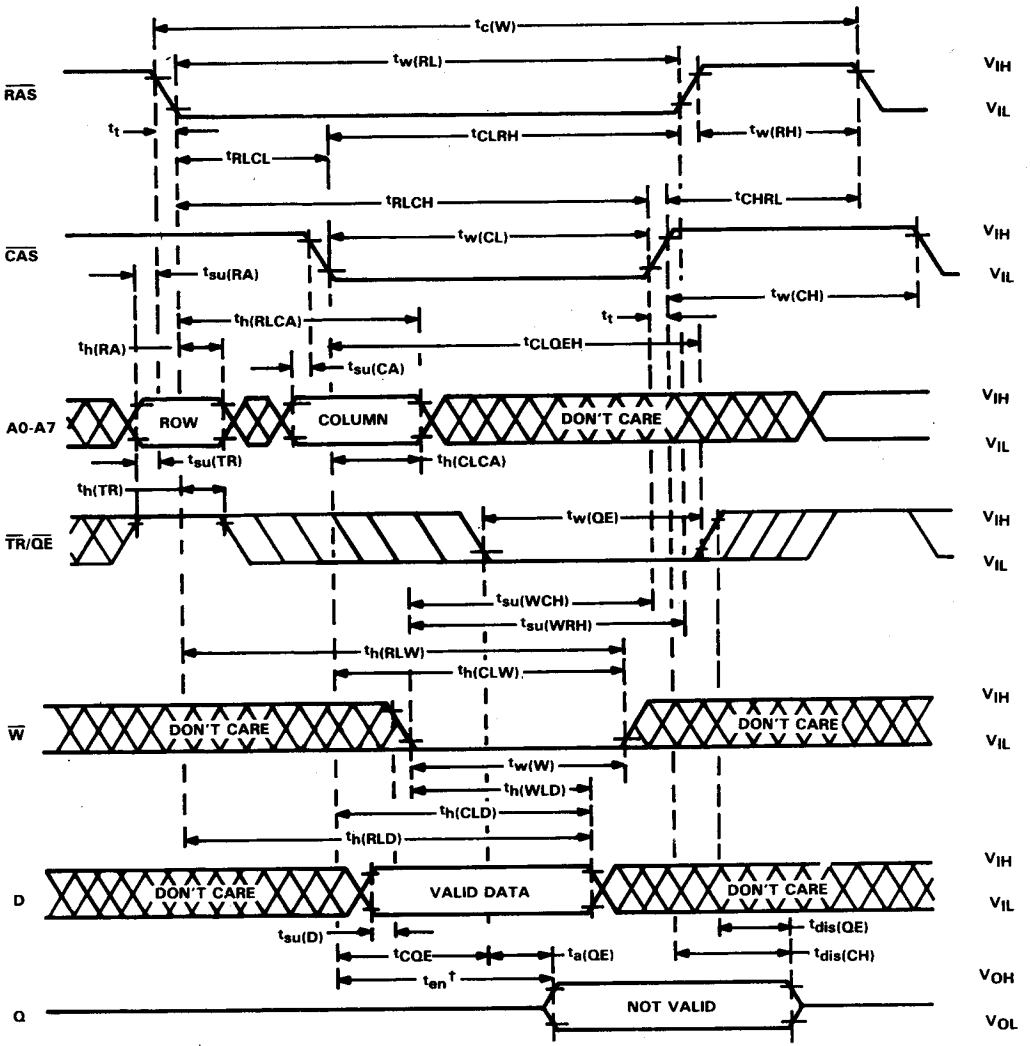
write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels a the output are invalid.

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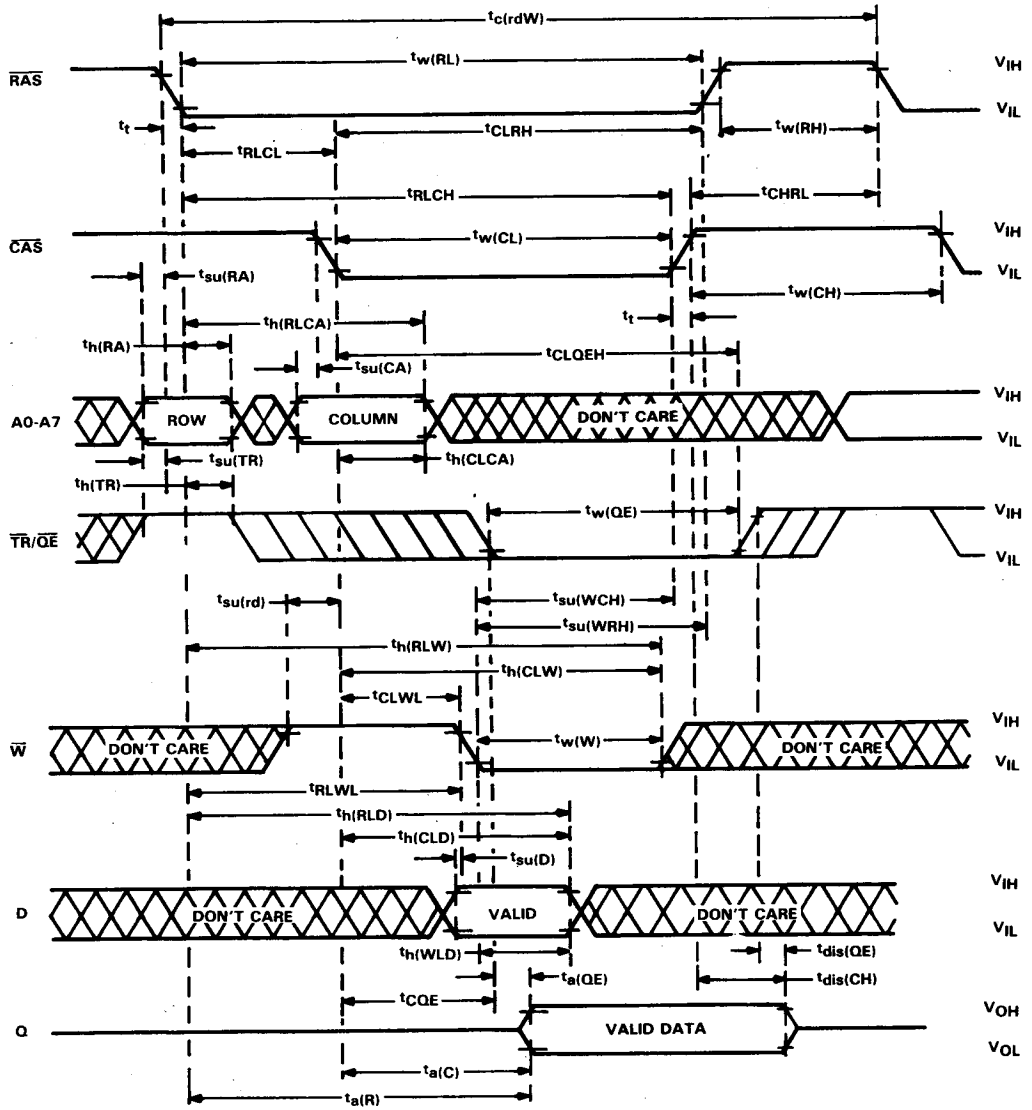
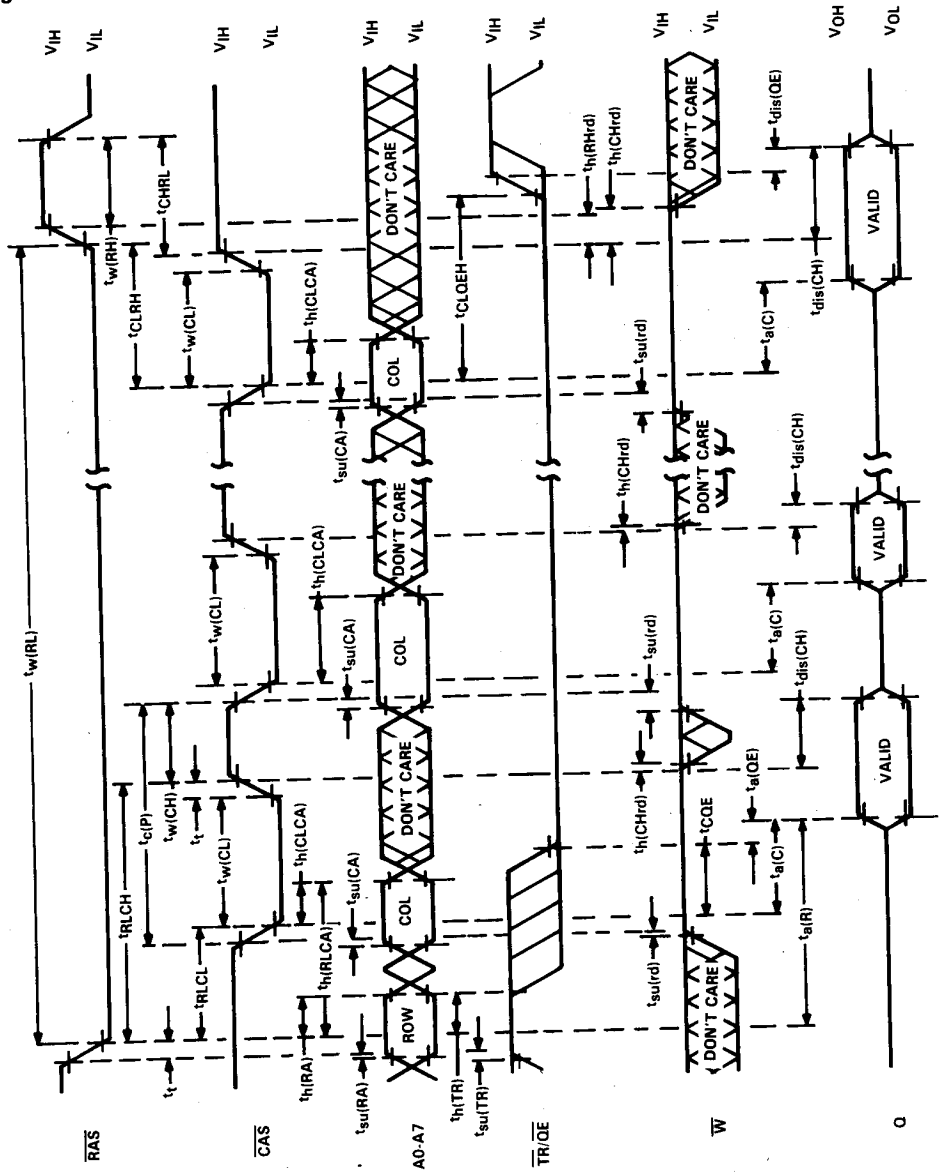
read-write/read-modify-write cycle timing

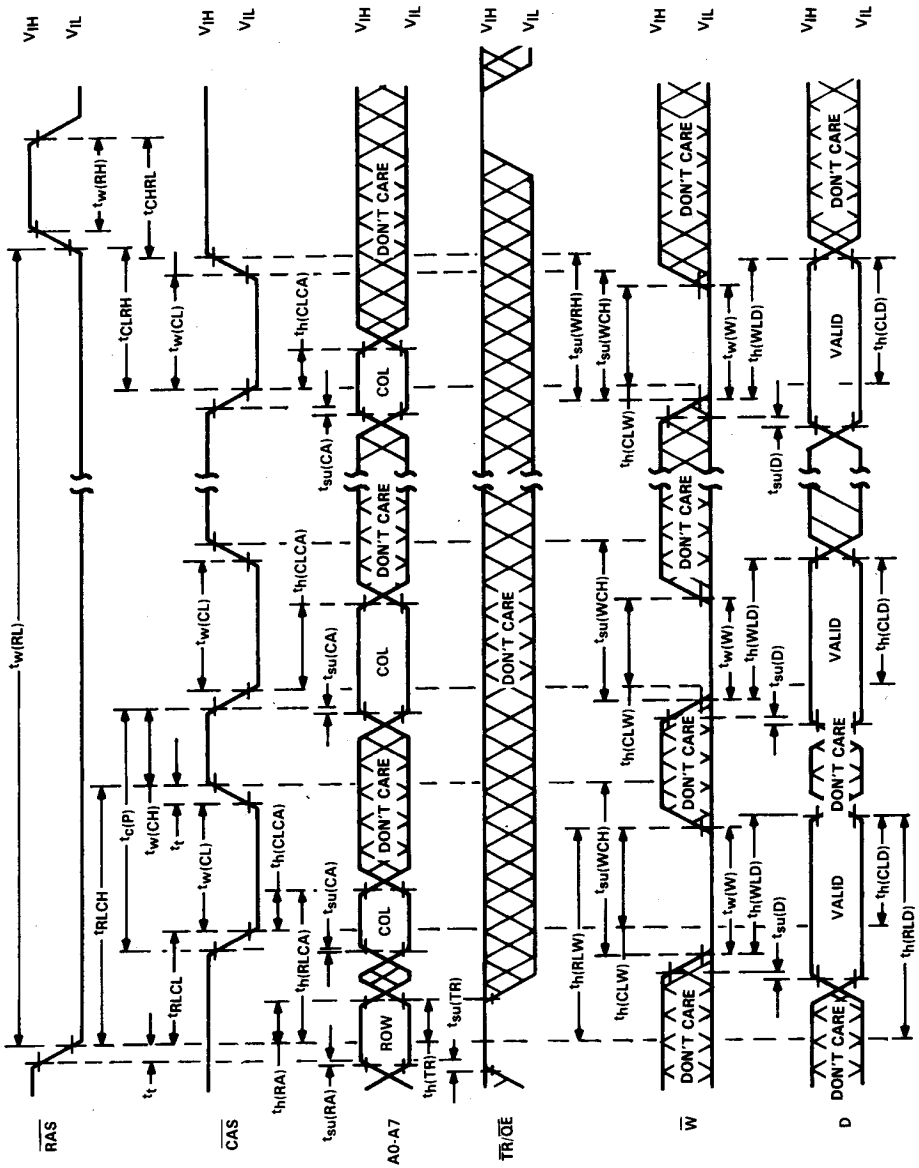


page-mode read cycle timing



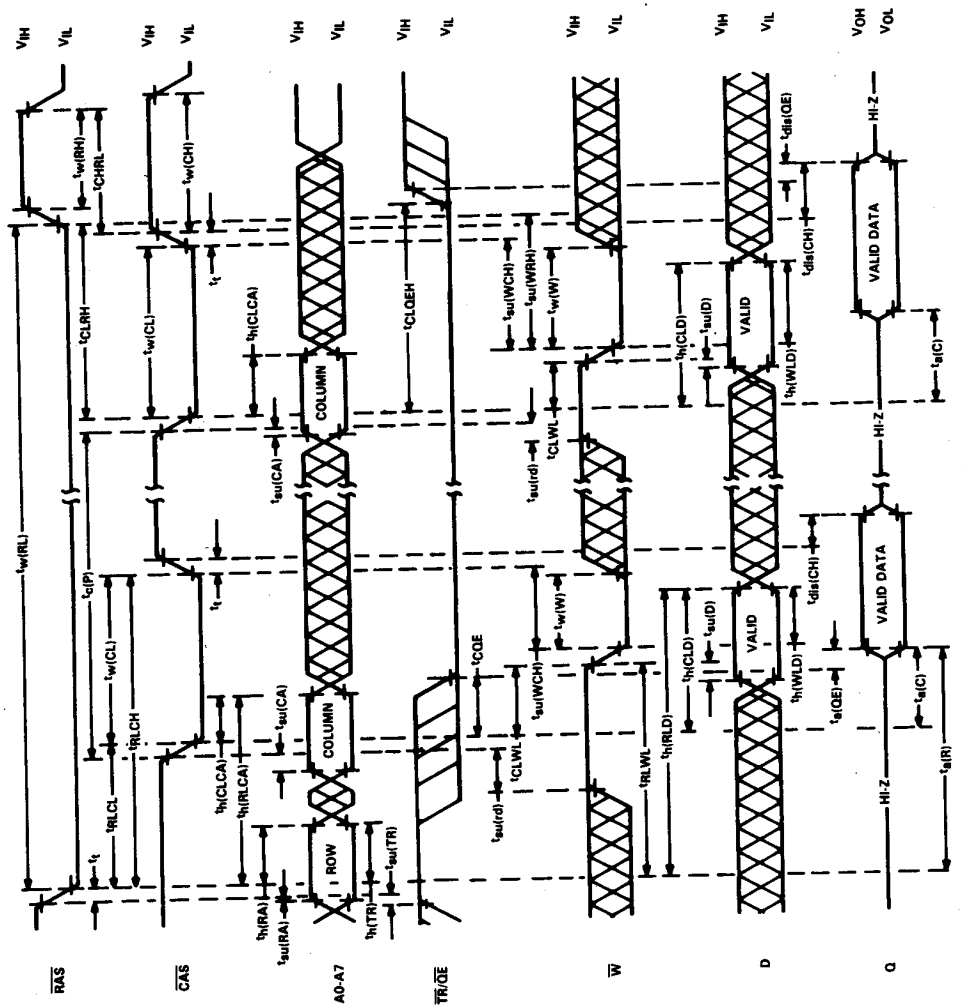
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.

page-mode write cycle timing



NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
9. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
10. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

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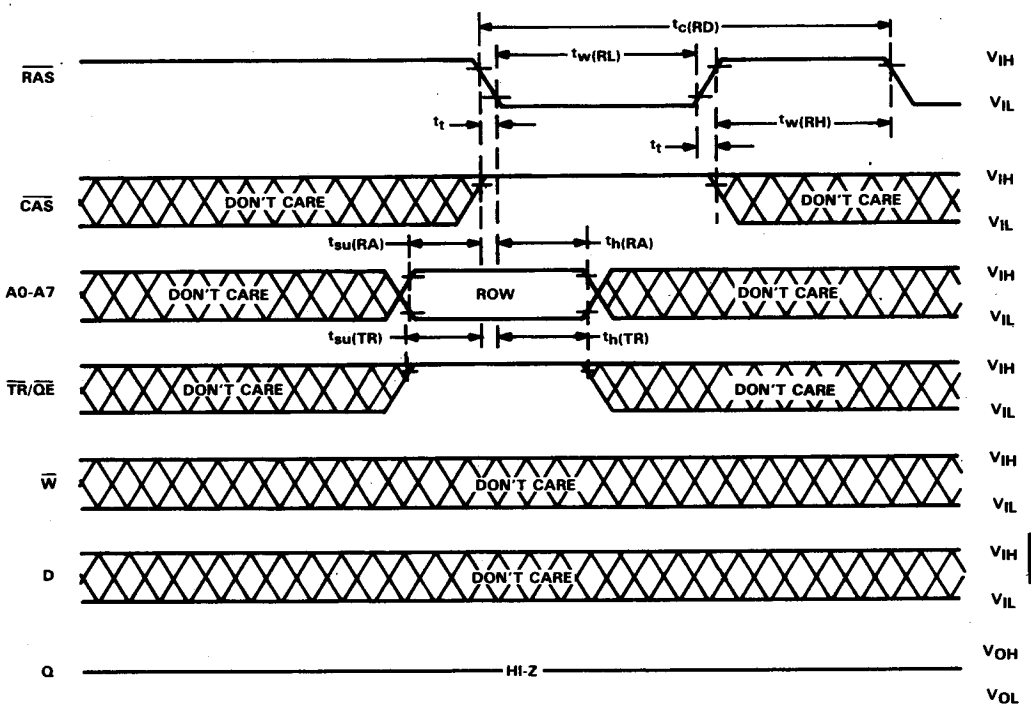
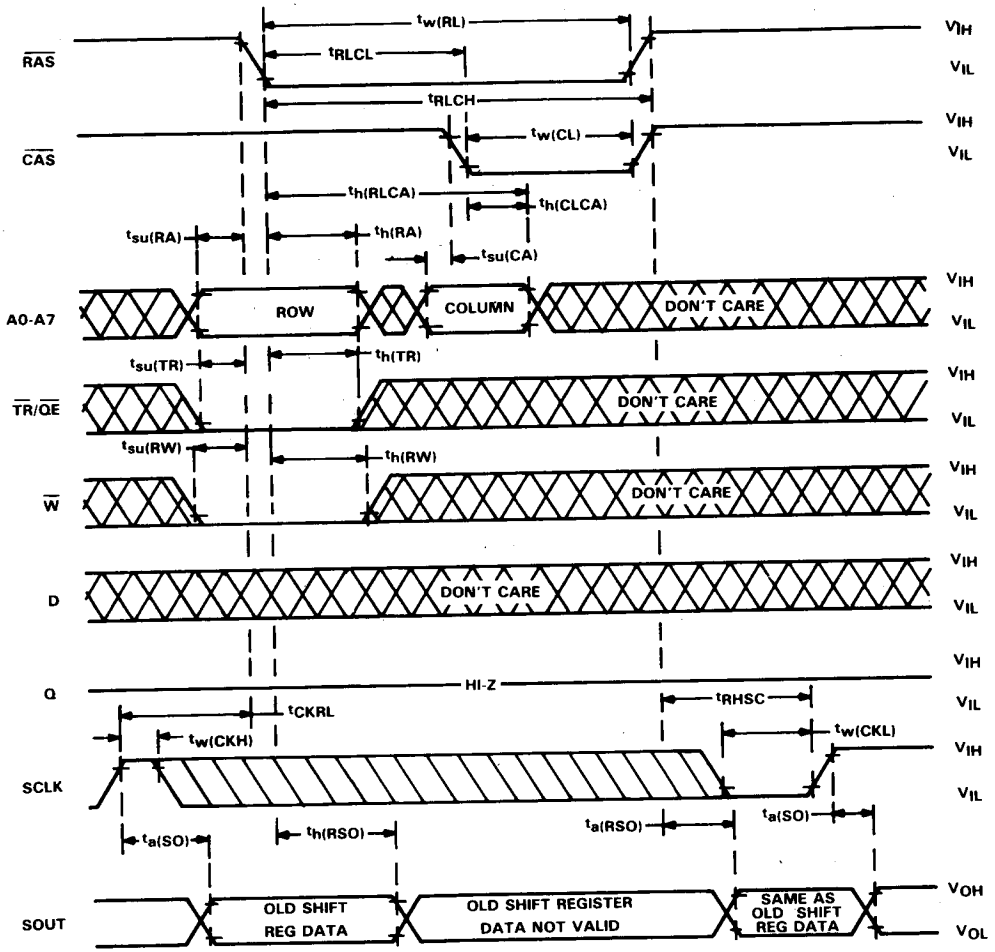
$\overline{\text{RAS}}$-only refresh timing



shift register to memory timing



NOTES: 11. The shift register to memory cycle is used to transfer data from the shift register to the memory array. Every one of the 256 locations in the shift register is written into the 256 columns of the selected row. Note that the data that was in the shift register may have resulted either from a serial shift in or from a parallel load of the shift register from one of the memory rows.

12. $\overline{SOE}$ assumed low.

13. SCLK may be high or low during $t_{w(RL)}$.

14. Multiple transfer write cycles require either a 1-μs $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$ cycle before initiation of the transfer write cycles and separation between any two consecutive transfer write cycles.

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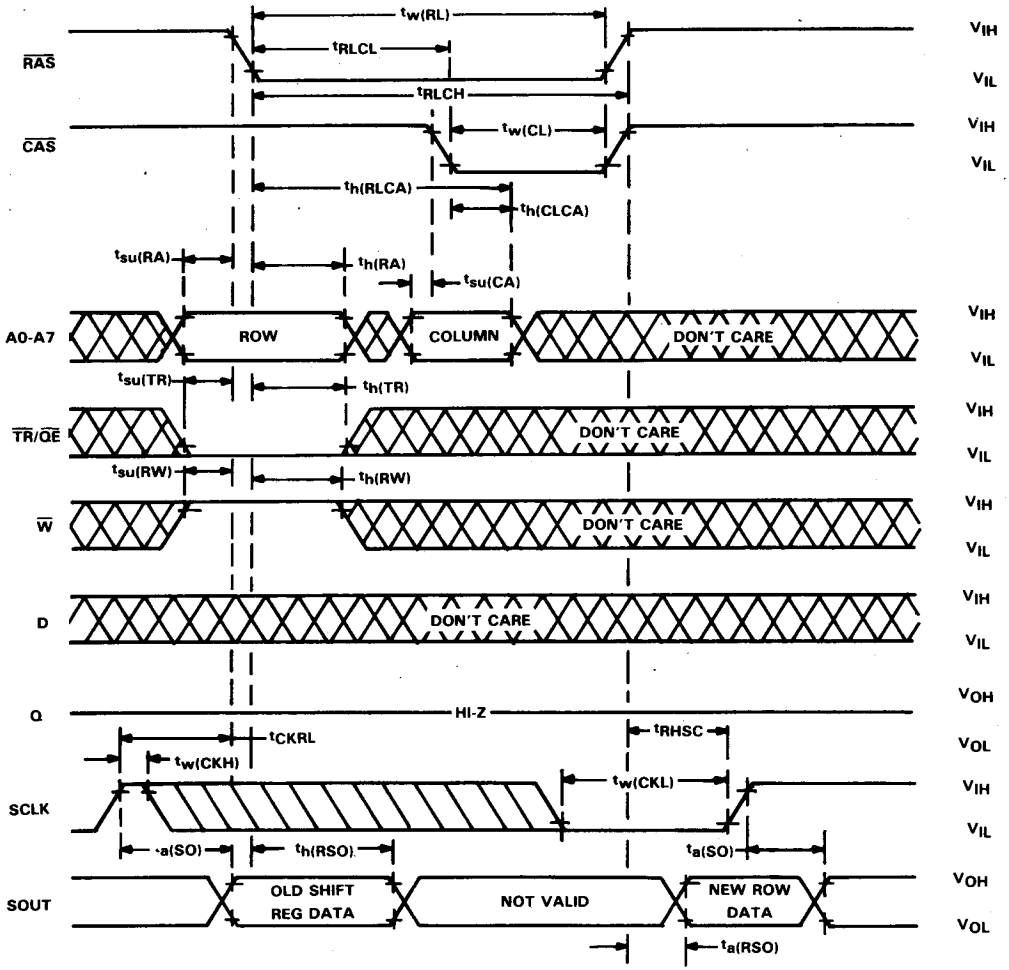
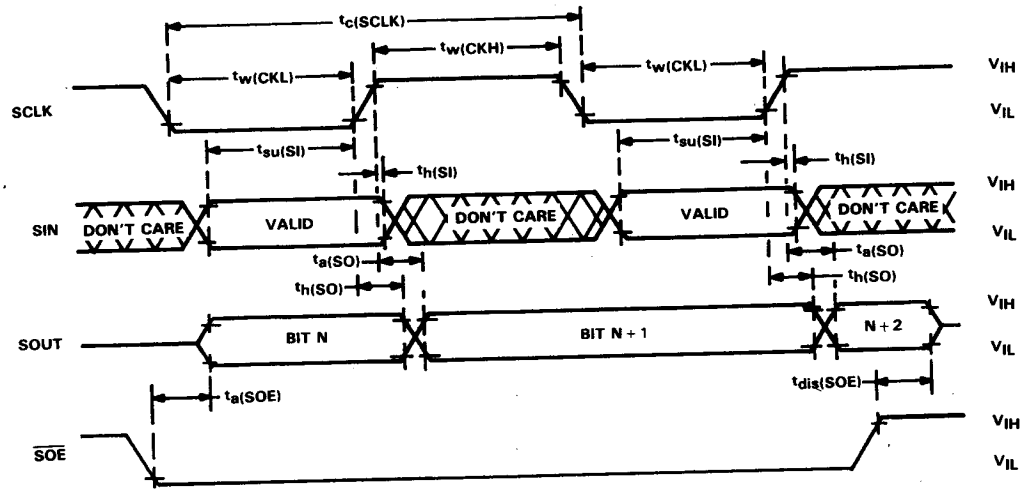
memory to shift register timing



NOTES: 12. $\overline{SOE}$ assumed low.

13. SCLK may be high or low during $t_{w(RL)}$.
14. Multiple transfer write cycles require either a 500-ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$ cycle before initiation of the transfer write cycles and separation between any two consecutive transfer write cycles.
15. The memory to shift register cycle is used to load the shift register in parallel from the memory array. Every one of the 256 locations in the shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift register may be either shifted out or written back into another row.

serial data shift timing



NOTES: 4. $t_{c(SCLK)}$ min is tested by connecting SIN to SOUT and test conditions include $t_{su(SI)}$; see paragraph entitled SIN and SOUT on page 5.

16. While shifting data through the serial shift register, the state of $\overline{TR}/\overline{OE}$ is a don't care as long as $\overline{TR}/\overline{OE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift register.

17. When loading data into the shift register from the serial input in preparation for a shift-register-to-memory transfer operation, the serial clock must be clocked an even number of times.

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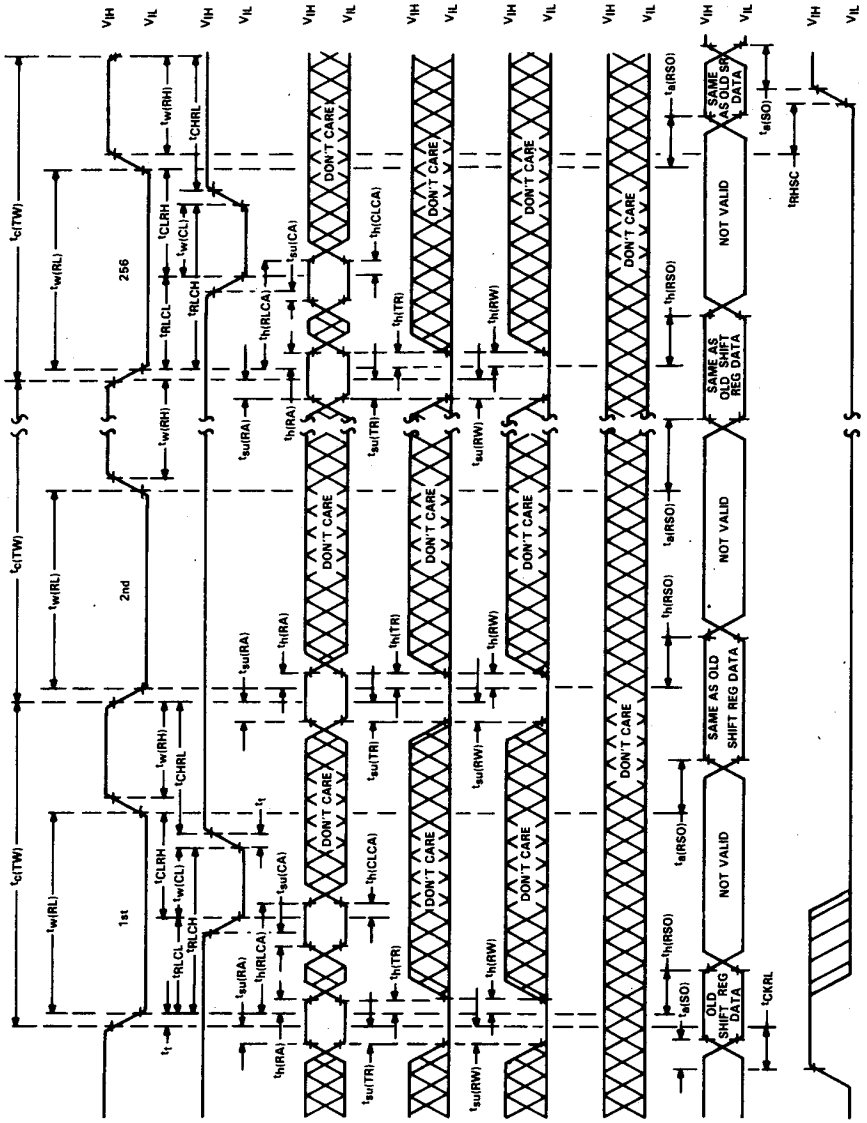
shift register to memory multiple timing



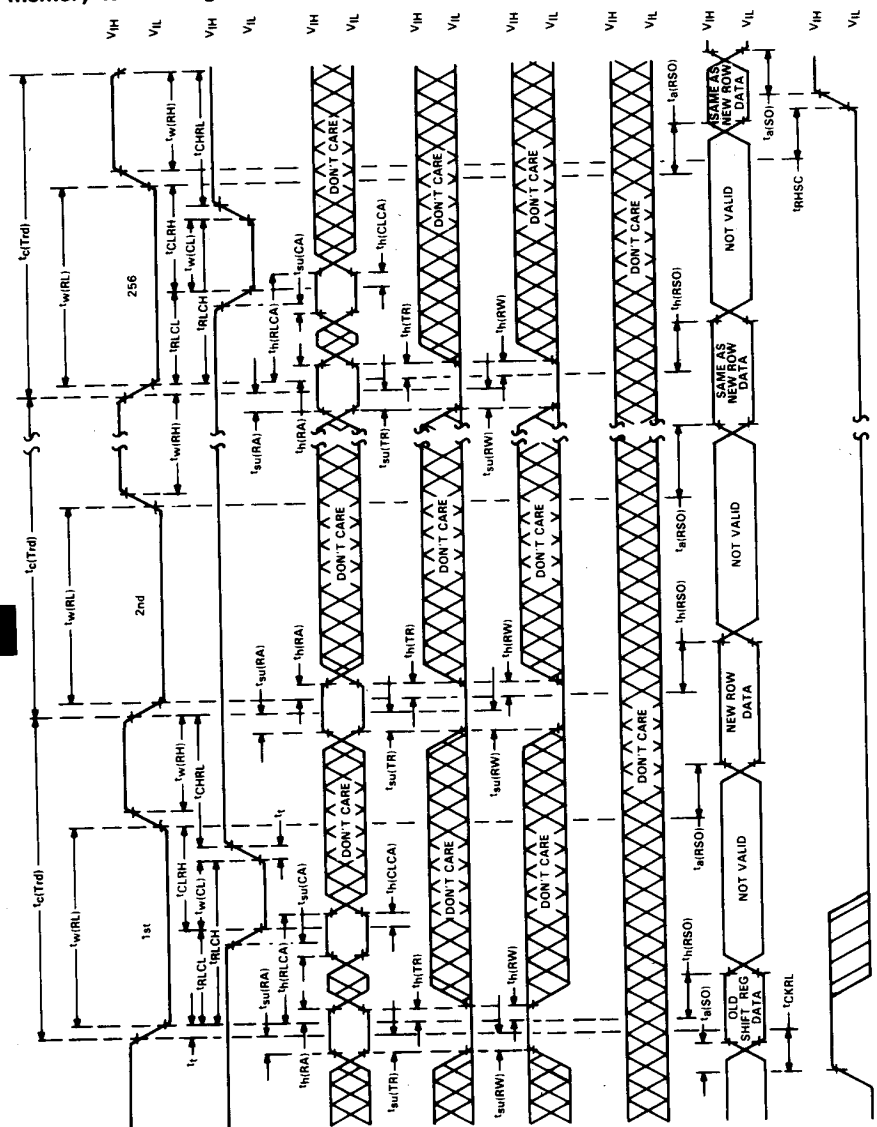
†CAS and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 12. SOE assumed low.

18. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN line would be held at 0 to fill all locations in the shift register with 0s. The shift register would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

19. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to tCKRL prior to RAS falling with TR/OE low.

memory to shift register to memory multiple timing



†$\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change from one register to another.

NOTES: 12. $\overline{SOE}$ assumed low.

19. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR/QE}$ low.
20. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

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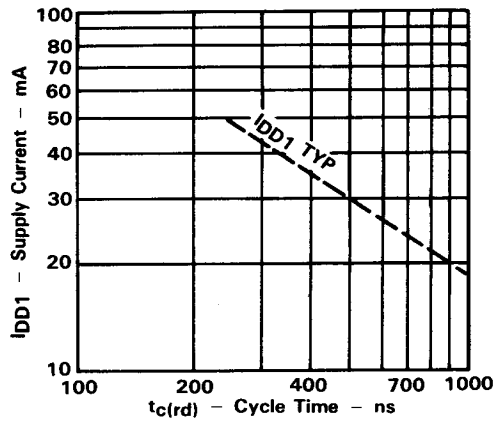
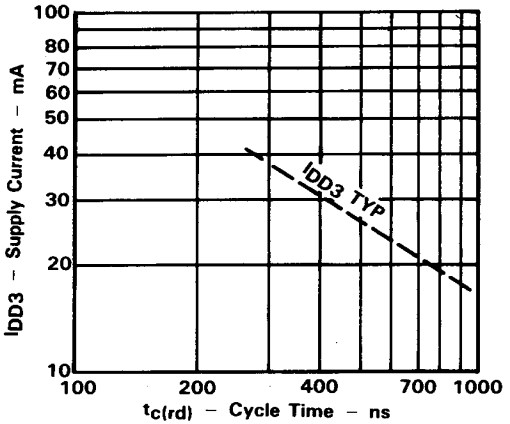
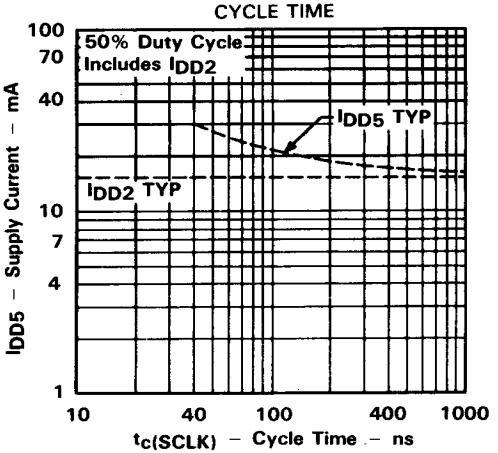
I_{DD1} vs CYCLE TIME



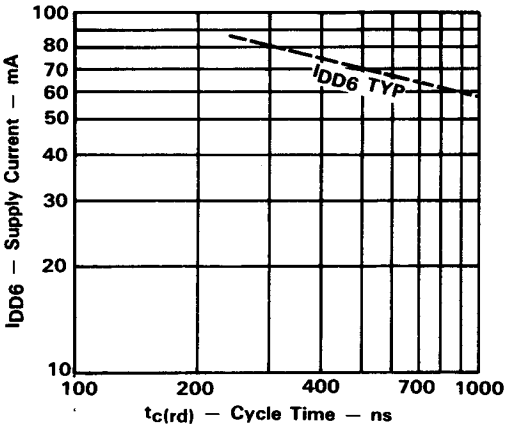
I_{DD3} vs CYCLE TIME



I_{DD5} vs CYCLE TIME



I_{DD6} vs CYCLE TIME



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