REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to test conditions in table I. Change code ident. no. from 14933 to 67268. Editorial changes throughout.	87-11-24	R. P. Evans
B	Add generic part number 1691A. Changes to table I. Editorial changes throughout.	94-10-05	M. A. Frye
C	Update to current requirements. Editorial changes throughout. – drw	03-07-10	Raymond Monnin
D	Sheet 10, correction to figure 3, test circuit. Editorial changes throughout. - drw	05-07-06	Raymond Monnin
E	Correction to the E package descriptive designator paragraph 1.2.2. – drw	06-05-01	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	E	E	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Donald R. Osborne

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
86-12-31

REVISION LEVEL
E

MICROCIRCUIT, LINEAR, RS-422/RS-423 LINE DRIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-86721**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E424-06

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86721	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	26LS30, 1691A	Dual differential RS-422 party line/quad single ended RS-423 line driver

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Supply voltage range (V_{EE})	+0.5 V dc to -7.0 V dc
Input voltage range	-1.5 V dc to +15.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	500 mW
Lead temperature (soldering, 4 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	90°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

EIA RS-422 connection:	
Mode voltage	≤0.76 V
Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Supply voltage (V_{EE})	GND
EIA RS-423 connection:	
Mode voltage	≥2.0 V
Supply voltage range (V_{CC})	+4.75 V dc to +5.5 V dc
Supply voltage range (V_{EE})	-4.75 V dc to -5.5 V dc
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 Vdc
Ambient operating temperature range	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{SA}/I_{SB}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table and logic diagram. The truth table and logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
EIA RS-422 Connection, mode voltage ≤0.76 V 1/ 2/								
Differential output voltage $V_{A, B}$	V_O	R_L = Infinity	V_{IN} = 2.0 V	1, 2, 3	01		6.0	V
	$\overline{V_O}$		V_{IN} = 0.8 V				-6.0	
Differential output voltage $V_{A, B}$	V_T	R_L = 100Ω	V_{IN} = 2.0 V	1, 2, 3	01	2.0		V
	$\overline{V_T}$		V_{IN} = 0.8 V			-2.0		
Common mode offset voltage	V_{OS}, $\overline{V_{OS}}$	R_L = 100Ω		1, 2, 3	01		3.0	V
Differential in diff'l output voltage	$\|\|V_T\|-\|\overline{V_T}\|\|$	R_L = 100Ω		1, 2, 3	01		0.4	V
Differential in common mode offset voltage	$\|\|V_{OS}\|-\|\overline{V_{OS}}\|\|$	R_L = 100Ω		1, 2, 3	01		0.4	V
$\|V_T - \overline{V_T}\|$	V_{SS}	R_L = 100Ω		1, 2, 3	01	4.0		V
Output voltage common mode range	V_{CMR}	$\overline{V}_{ENABLE}$ = 2.4 V 3/		1, 2, 3	01	±10		V
Output leakage current	I_{XA}	V_{CC} = 0 V	V_{CMR} = 10 V	1, 2, 3	01		100	µA
	I_{XB}		V_{CMR} = -10 V				-100	
Off-state output current (high impedance)	I_{OX}	V_{CC} = +5.5 V	V_{CMR} = 10 V	1, 2, 3	01		100	µA
			V_{CMR} = -10 V				-100	
Output short circuit current 4/	I_{SA}, I_{SB}	V_{IN} = 2.4 V, V_{CC} = +5.5 V	V_{OB} = 6.0 V	1, 2, 3	01	10	150	mA
			V_{OA} = 0 V			-10	-150	
		V_{IN} = 2.4 V, V_{CC} = +5.5 V	V_{OB} = 0 V	1, 2, 3	01	-10	-150	
			V_{OA} = 6.0 V			10	150	
Supply current	I_{CC}	V_{IN} = 0.4 V, V_{cc} = +5.5 V		1, 2, 3	01		30	mA
Input high voltage	V_{IH}	5/		1, 2, 3	01	2.0		V
Input low voltage	V_{IL}	5/		1, 2, 3	01		0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input high current	I_{IH}	V_{CC} = +5.5 V	V_{IN} = 2.4 V	1, 2, 3	01		40	µA
			V_{IN} = 15 V				100	
Input low current	I_{IL}	V_{CC} = +5.5 V, V_{IN} = 0.4 V		1, 2, 3	01		-200	µA
Input clamp voltage	V_{IC}	I_{IN} = -12 mA, V_{CC} = +4.5 V		1, 2, 3	01		-1.5	V
Functional tests	FT	See 4.3.1.c		7, 8	01			
Differential output rise and fall time 6/	t_r, t_F	R_L = 100Ω, T_A = +25°C, C_L = 500 pF, V_{CC} = 5.0 V, V_{EE} = GND, See figure 3		9	01		250	ns
Output propagation delay time 6/	t_{PDH}, t_{PDL}	R_L = 100Ω, T_A = +25°C, C_L = 500 pF, V_{CC} = 5.0 V, V_{EE} = GND, See figure 3		9	01		200	ns
Output enable to output time 6/	t_{LZ}, t_{ZH}	R_L = 100Ω, T_A = +25°C, C_L = 500 pF, V_{CC} = 5.0 V, C_C = 0 pF, V_{EE} = GND, See figure 3		9	01		300	ns
	t_{HZ}, t_{ZL}						350	
EIA RS-423 Connection, mode voltage ≥2.0 V								
Output voltage	V_O	R_L = Infinity, $\|V_{CC}\| = \|V_{EE}\|$ = 4.75 V	V_{IN} = 2.0 V	1, 2	01	4.0	6.0	V
				3		3.9	6.0	
	$\overline{V_O}$		V_{IN} = 0.4 V	1, 2	01	-4.0	-6.0	
				3		-3.9	-6.0	
Output voltage 7/	V_T	R_L = 450Ω, $\|V_{CC}\| = \|V_{EE}\|$ = 4.75 V	V_{IN} = 2.4 V	1, 2, 3	01	3.6		V
	$\overline{V_T}$		V_{IN} = 0.4 V			-3.6		
Output unbalance 7/	$\|\|V_T\|-\|\overline{V_T}\|\|$	R_L = 450Ω, $\|V_{CC}\| = \|V_{EE}\|$		1, 2, 3	01		0.4	V
Output leakage power off	I_{X+}	$\|V_{CC}\| = \|V_{EE}\|$ = 0 V	V_{OUT} = 6.0 V	1, 2, 3	01		100	µA
	I_{X-}		V_{OUT} = -6.0 V				-100	
Output short circuit current 4/	I_{S+}	V_{OUT} = 0 V, V_{CC} = 5.5 V V_{EE} = -5.5 V	V_{IN} = 2.4 V	1, 2, 3	01	-20	-150	µA
	I_{S-}		V_{IN} = 0.4 V			20	150	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Positive supply current	I_{CC}	V_{IN} = 0.4 V, R_L = Infinity, $\|V_{CC}\| = \|V_{EE}\|$ = 5.5 V		1, 2, 3	01		30	mA
Negative supply current	I_{EE}	V_{IN} = 0.4 V, R_L = Infinity, $\|V_{CC}\| = \|V_{EE}\|$ = 5.5 V		1, 2, 3	01		-22	mA
Input clamp voltage	V_{IC}	I_{IN} = -12 mA, V_{CC} = +4.75 V, V_{EE} = -5.5 V 8/		1, 2, 3	01		-1.5	V
Input high voltage	V_{IH}	9/		1, 2, 3	01	2.0		V
Input low voltage	V_{IL}	9/		1, 2, 3	01		0.8	V
Input high current	I_{IH}	$\|V_{CC}\| = \|V_{EE}\|$ = 5.5 V, V_{IN} = 2.4 V		1, 2, 3	01		40	µA
		V_{CC} = 5.5 V, V_{EE} = -5.0 V, V_{IN} = 15 V					100	
Input low current	I_{IL}	$\|V_{CC}\| = \|V_{EE}\|$ = 5.5 V, V_{IN} = 0.4 V		1, 2, 3	01		-200	µA
Functional tests	FT	See 4.3.1.c		7, 8	01			
Rise and fall time	t_r, t_f	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF, See figure 3	T_A = +25°C, V_{CC} = 5.0 V, V_{EE} = -5.0 V	9	01		300	ns
			V_{CC} = +4.75 V to +5.5 V, V_{EE} = -4.75 V to -5.5 V	10, 11 6/			375	
Output propagation delay time	t_{PDH}, t_{PDL}	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF, See figure 3	T_A = +25°C, V_{CC} = 5.0 V, V_{EE} = -5.0 V	9	01		300	ns
			V_{CC} = +4.75 V to +5.5 V, V_{EE} = -4.75 V to -5.5 V	10, 11 6/			375	

1/ R_L connected between each output and its complement.
2/ Measurements for ATE loads are for single-ended conditions.
3/ V_{CMR} is guaranteed by tested parameters I_{XA}, I_{XB} and I_{OX}.
4/ Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
5/ Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
6/ This parameter is guaranteed, but not tested.
7/ This parameter is tested by forcing an equivalent current.
8/ The V_{IC} parameter in the RS423 mode is guaranteed by the tested V_{IC} parameter in the RS422 mode.
9/ Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.

Device type	01	
Case outlines	E, F	2
Terminal number	Terminal symbol	
1	V_{CC}	NC
2	INPUT A	V_{CC}
3	INPUT/$\overline{\text{ENABLE}}$ B	INPUT A
4	MODE	INPUT/$\overline{\text{ENABLE}}$ B
5	GND	MODE
6	INPUT/$\overline{\text{ENABLE}}$ C	NC
7	INPUT D	GND
8	V_{EE}	INPUT/$\overline{\text{ENABLE}}$ C
9	SLEW RATE CONTROL D	INPUT D
10	OUTPUT D	V_{EE}
11	OUTPUT C	NC
12	SLEW RATE CONTROL C	SLEW RATE CONTROL D
13	SLEW RATE CONTROL B	OUTPUT D
14	OUTPUT B	OUTPUT C
15	OUTPUT A	SLEW RATE CONTROL C
16	SLEW RATE CONTROL A	NC
17	- - -	SLEW RATE CONTROL B
18	- - -	OUTPUT B
19	- - -	OUTPUT A
20	- - -	SLEW RATE CONTROL A

FIGURE 1. Terminal connections.

Mode	Inputs		Outputs	
	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

0 = low level
1 = high level
Z = high impedance

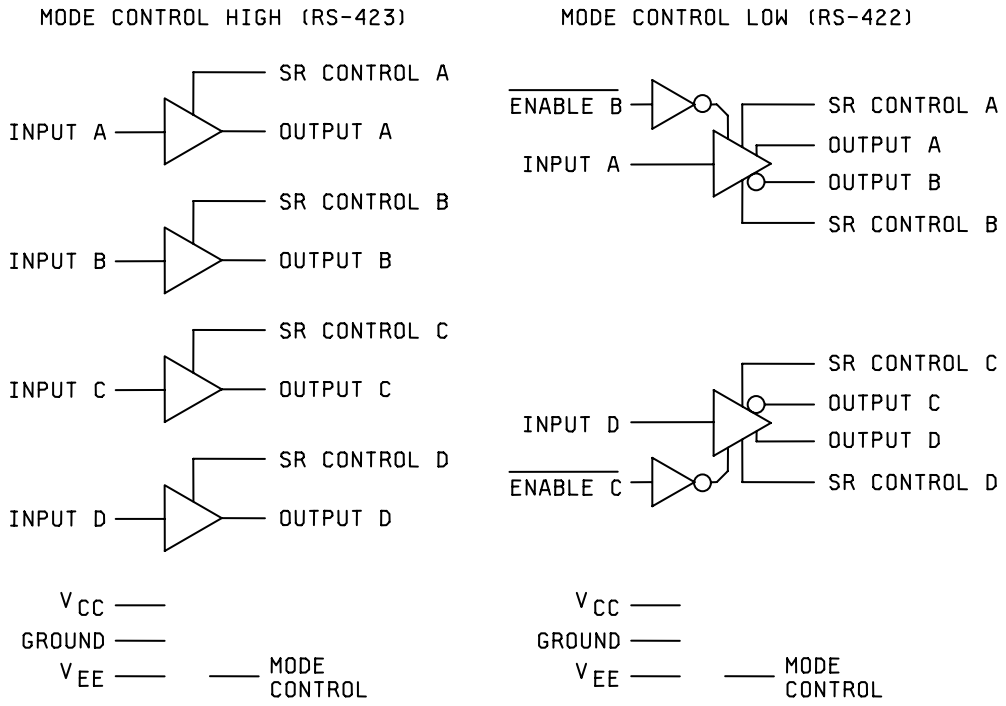
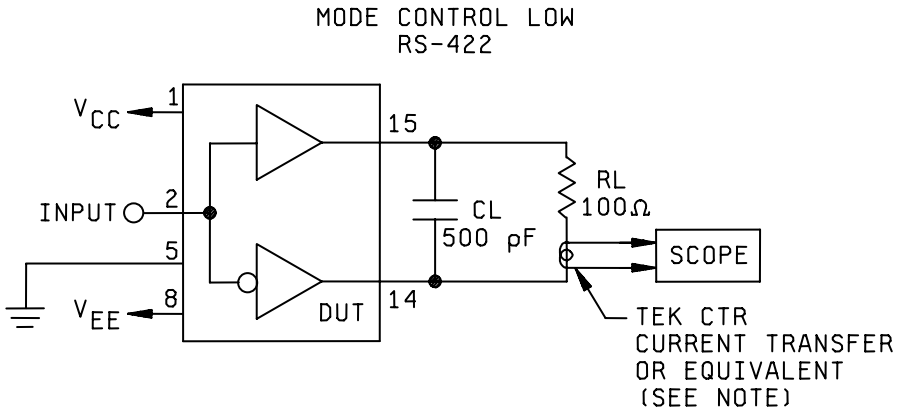
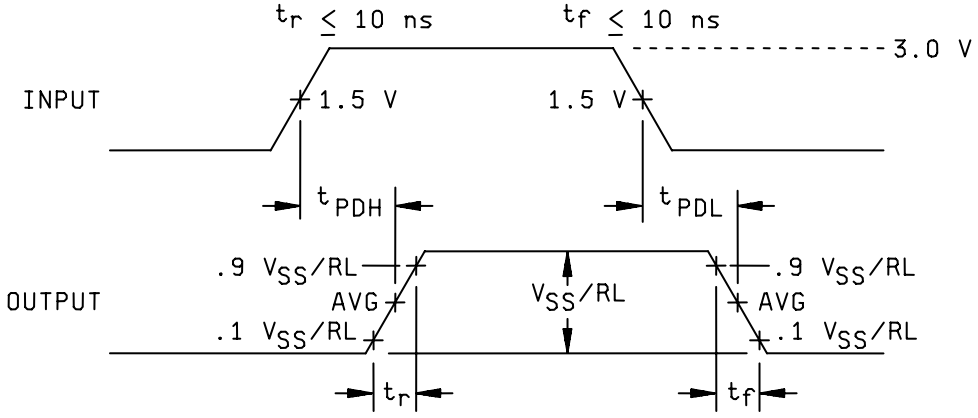


FIGURE 2. Truth table and logic diagram.



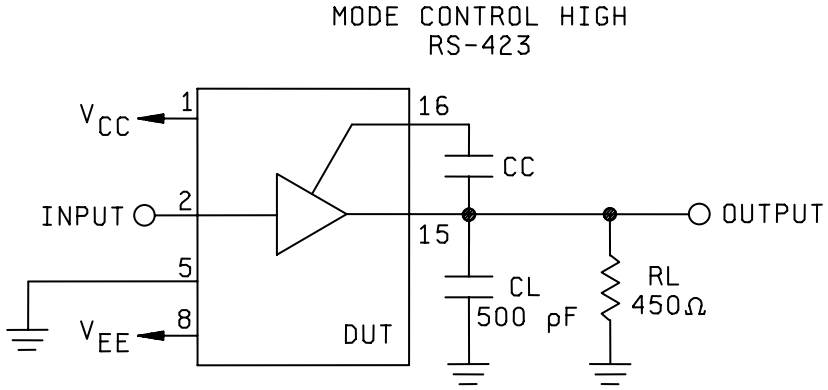
TEST CIRCUIT



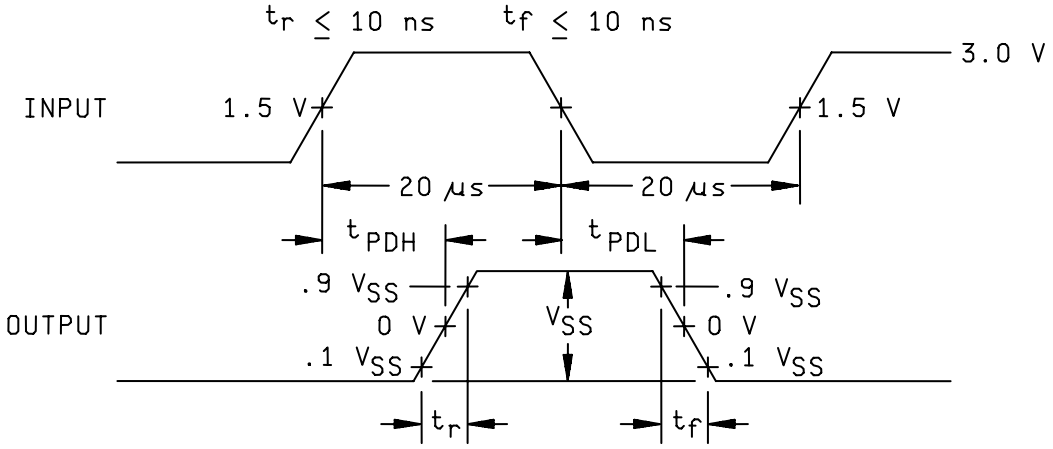
AC WAVEFORM

NOTE: Current probe is the easiest way to display a differential waveform.

FIGURE 3. AC test circuits and waveforms.

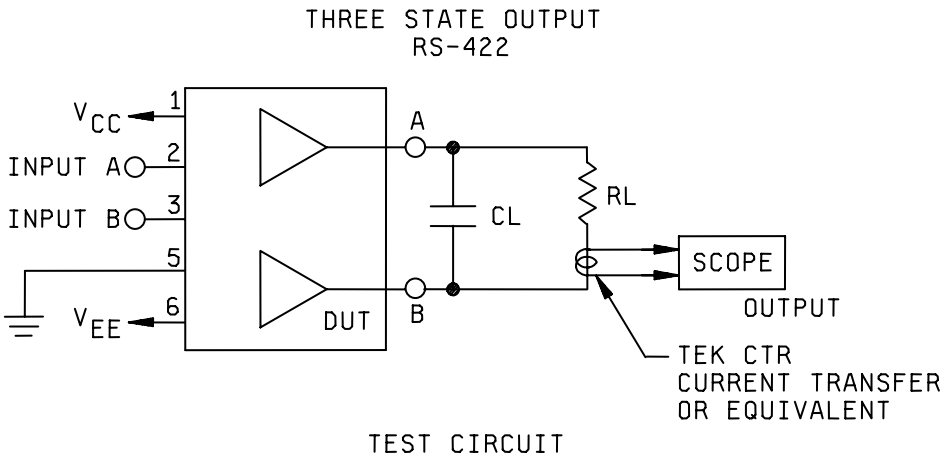


TEST CIRCUIT

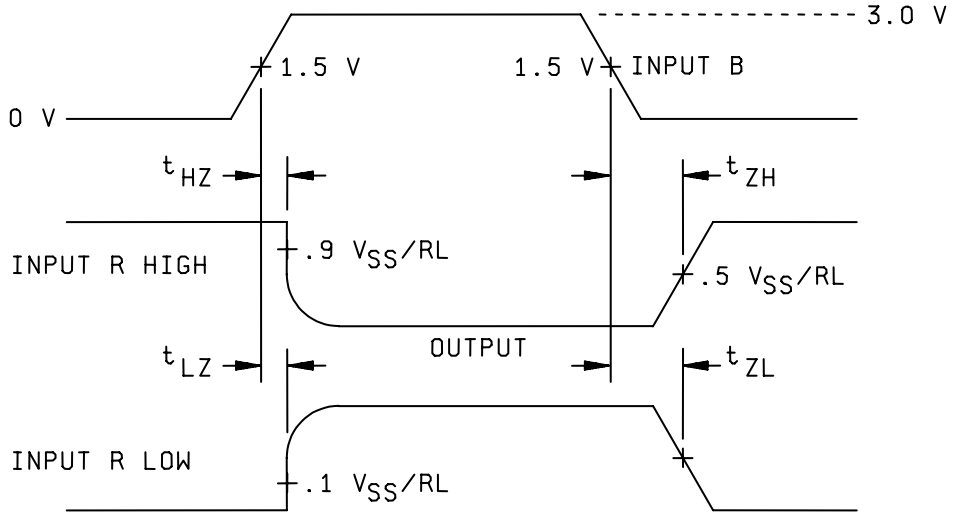


AC WAVEFORM

FIGURE 3. AC test circuits and waveforms - continued.



TEST CIRCUIT



AC WAVEFORM

FIGURE 3. AC test circuits and waveforms - continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-05-01

Approved sources of supply for SMD 5962-86721 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-86721012A	3V146	26LS30/B2A
	3/	AM26LS30/B2A
5962-8672101EA	3V146	26LS30/BEA
	3/	DS1691AJ/883
	3/	AM26LS30/BEA
5962-8672101FA	3V146	26LS30/BFA
	3/	AM26LS30/BFA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 10 Malcolm Hoyt Drive Newburyport, MA 01950