Rochester Electronics®

Datasheet

CY7C1021BV33

64K x 16 Static RAM

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

CY7C1021BV33

64K x 16 Static RAM

Features

- **3.3V operation (3.0V–3.6V)**
- **High speed**
  - **t_{AA} = 10/12/15 ns**
- **CMOS for optimum speed/power**
- **Low Active Power (L version)**
  - **576 mW (max.)**
- **Low CMOS Standby Power (L version)**
  - **1.80 mW (max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II and 400-mil SOJ**
- **Available in a 48-Ball Mini BGA package**

Functional Description[1]

The CY7C1021BV is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

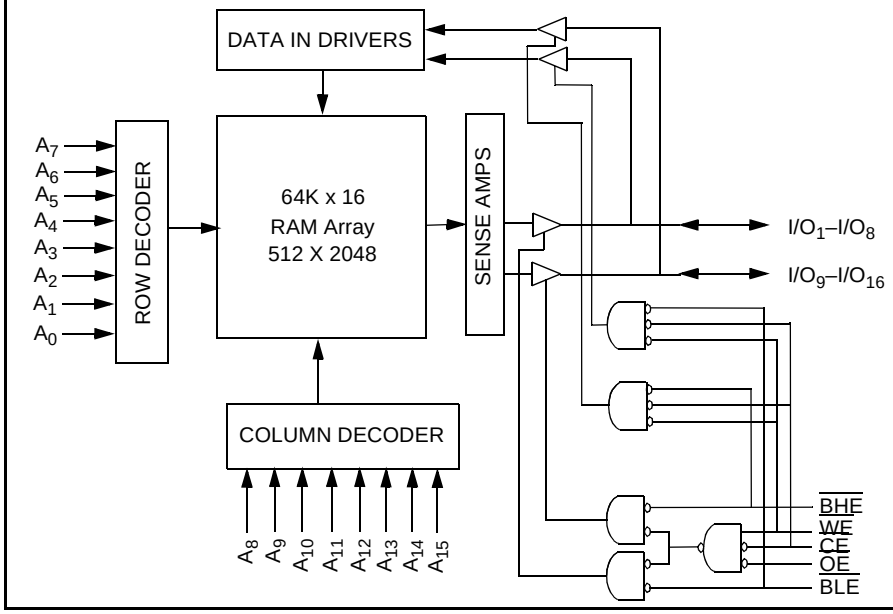
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

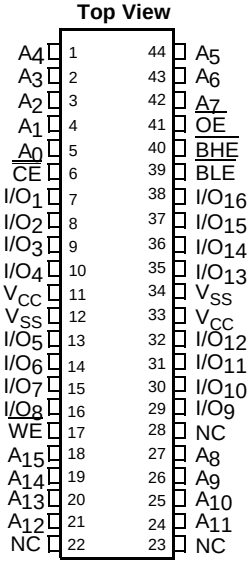
The CY7C1021BV is available in 400-mil-wide SOJ, standard 44-pin TSOP Type II, and 48-ball mini BGA packages.

Logic Block Diagram



Pin Configurations

SOJ / TSOP II
Top View



Selection Guide

			7C1021BV-8	7C1021BV-10	7C1021BV-12	7C1021BV-15
Maximum Access Time (ns)			8	10	12	15
Maximum Operating Current (mA)	Commercial		170	160	150	140
	Industrial		190	180	170	160
Maximum CMOS Standby Current (mA)	Commercial		5	5	5	5
		L	0.500	0.500	0.500	0.500

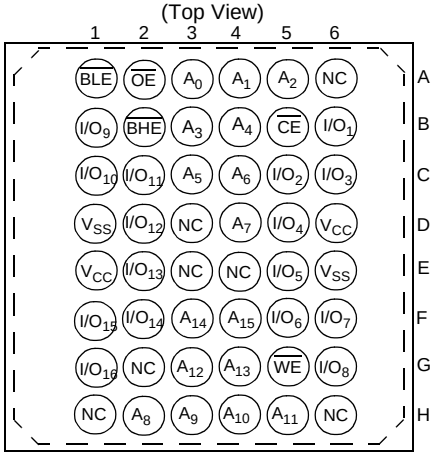
Shaded areas contain advance information.

Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Pin Configurations

Mini BGA
(Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[2] ..... –0.5V to V_{CC}+0.5V

DC Input Voltage[2]..... –0.5V to V_{CC}+0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Note:
2. Mimimum voltage is–2.0V for pulse durations of less than 20 ns.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1021BV-8 Min.	7C1021BV-8 Max.	7C1021BV-10 Min.	7C1021BV-10 Max.	7C1021BV-12 Min.	7C1021BV-12 Max.	7C1021BV-15 Min.	7C1021BV-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+ 0.3V	2.2	V_{CC}+ 0.3V	2.2	V_{CC}+ 0.3V	2.2	V_{CC}+ 0.3V	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com		170		160		150		140	mA
			Ind		190		120		170		160	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0			5		5		5		5	mA
			L		500		500		500		500	µA

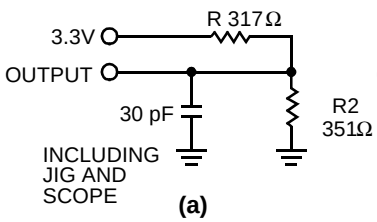
Shaded areas contain advance information.

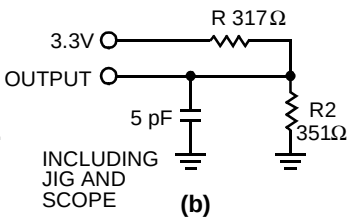
Capacitance[3]

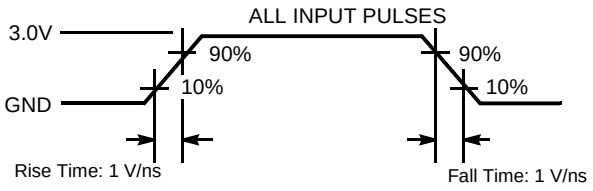
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

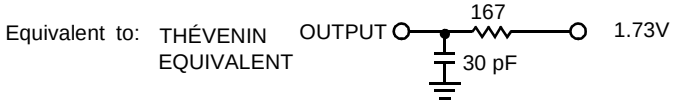
Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms









Switching Characteristics[4] Over the Operating Range

Parameter	Description	7C1021BV-8		7C1021BV-10		7C1021BV-12		7C1021BV-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4		4		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		4		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		12		12		15	ns
t_{DBE}	Byte Enable to Data Valid	4			5		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		0		ns
t_{HZBE}	Byte Disable to High Z		4		5		6		7	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		9		10		ns
t_{AW}	Address Set-Up to Write End	6		7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		8		8		10		ns
t_{SD}	Data Set-Up to Write End	4		6		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		4		5		6		7	ns
t_{BW}	Byte Enable to End of Write	8		8		8		9		ns

Shaded areas contain advance information.

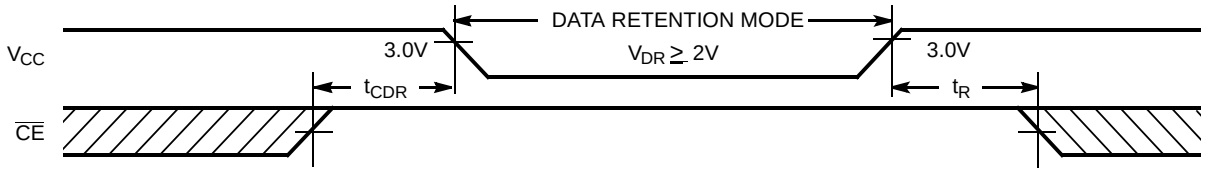
Data Retention Characteristics Over the Operating Range (L version only)

Parameter	Description		Conditions[8]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l	$\underline{V_{CC}} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		100	µA
t_{CDR}[9]	Chip Deselect to Data Retention Time			0		ns
t_R[10]	Operation Recovery Time			t_{RC}		ns

Notes:

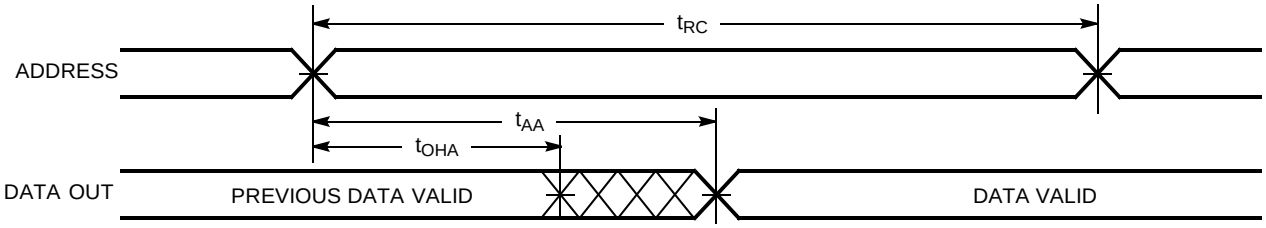
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$ / $\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$ / $\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. No input may exceed V_{CC} + 0.5V.
9. Tested initially and after any design or process changes that may affect these parameters.
10. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.

Data Retention Waveform

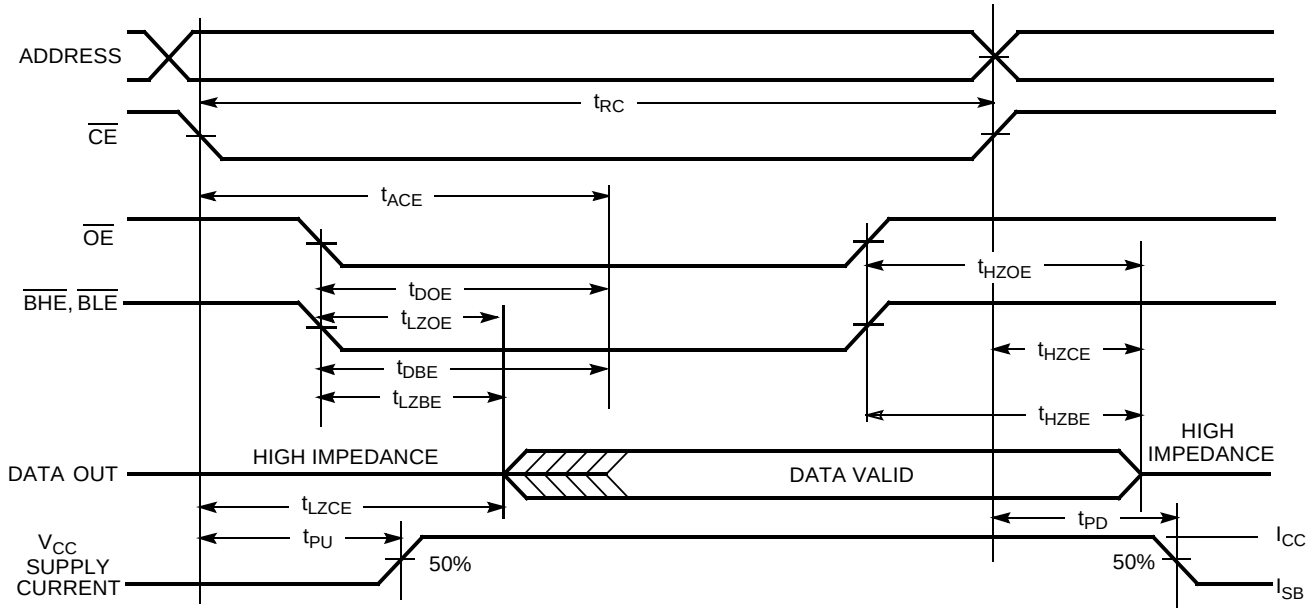


Switching Waveforms

Read Cycle No. 1[11, 12]



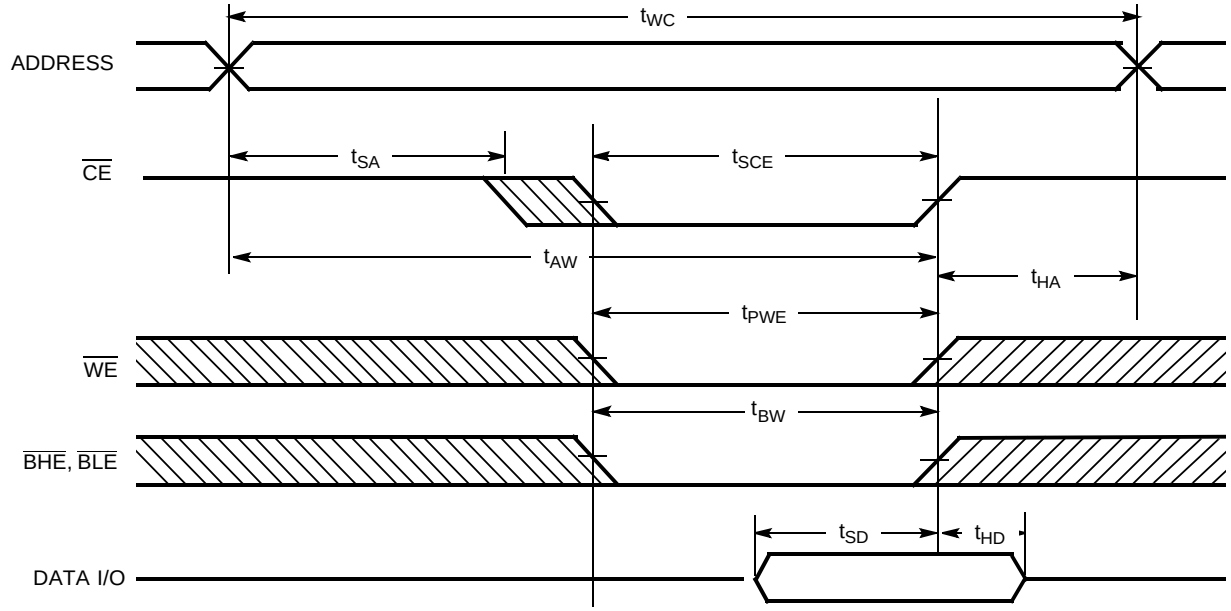
Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



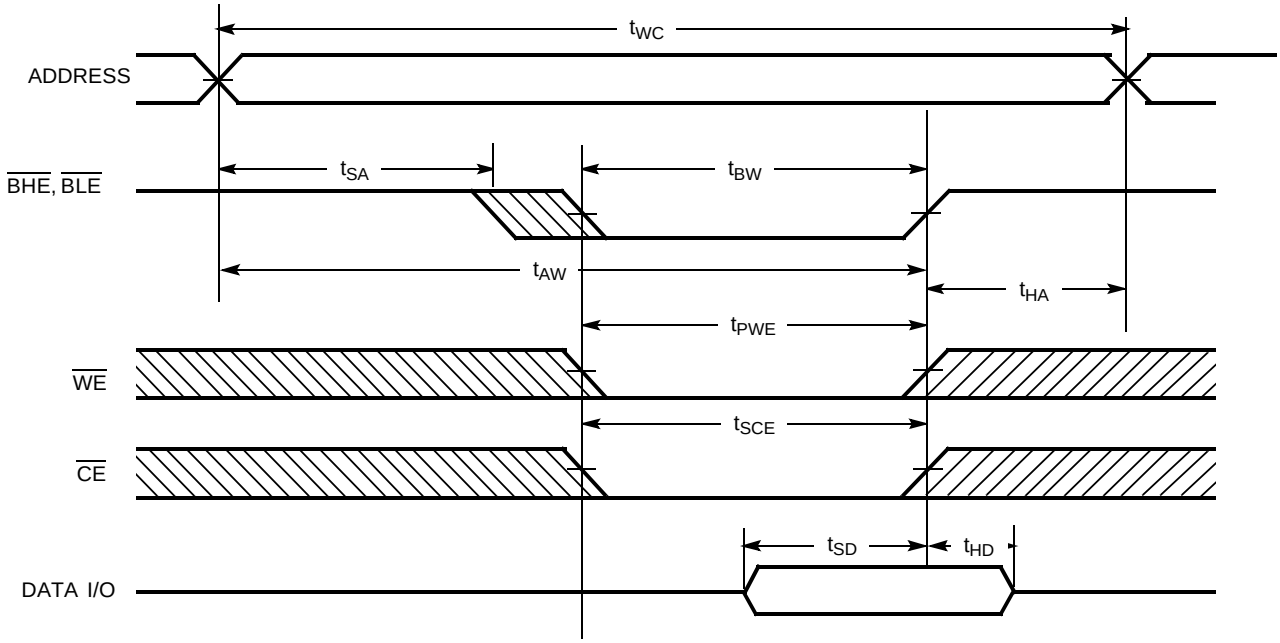
Notes:
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]



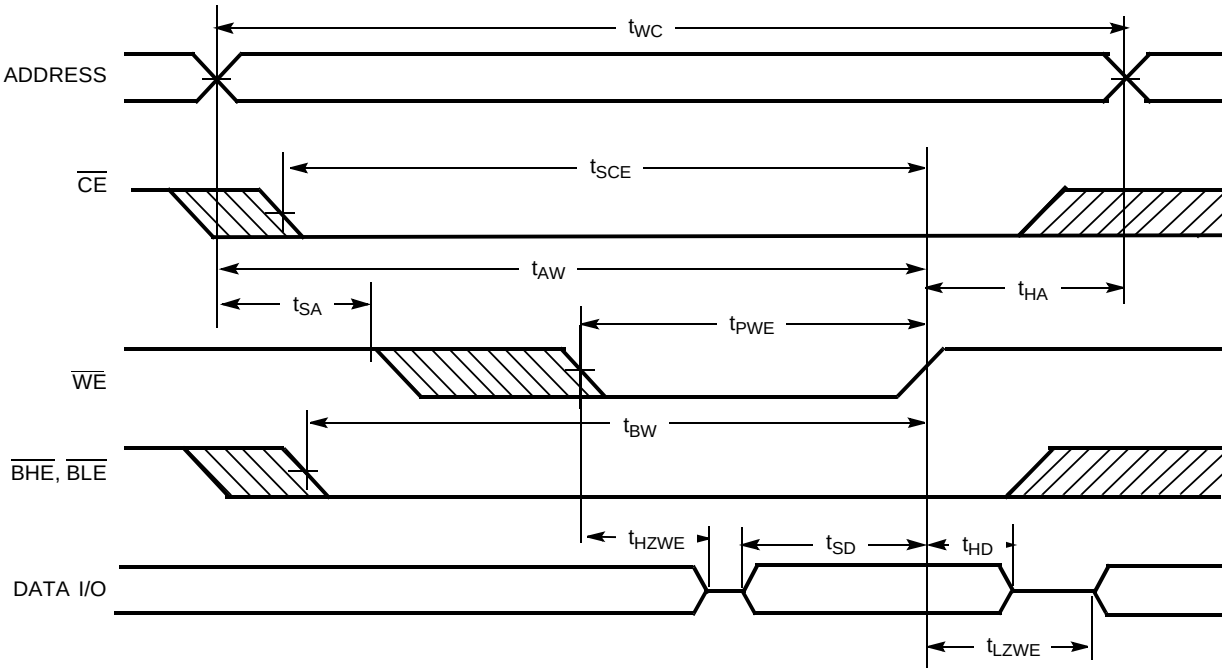
Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes:
14. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_1–I/O_8$	$I/O_9–I/O_{16}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

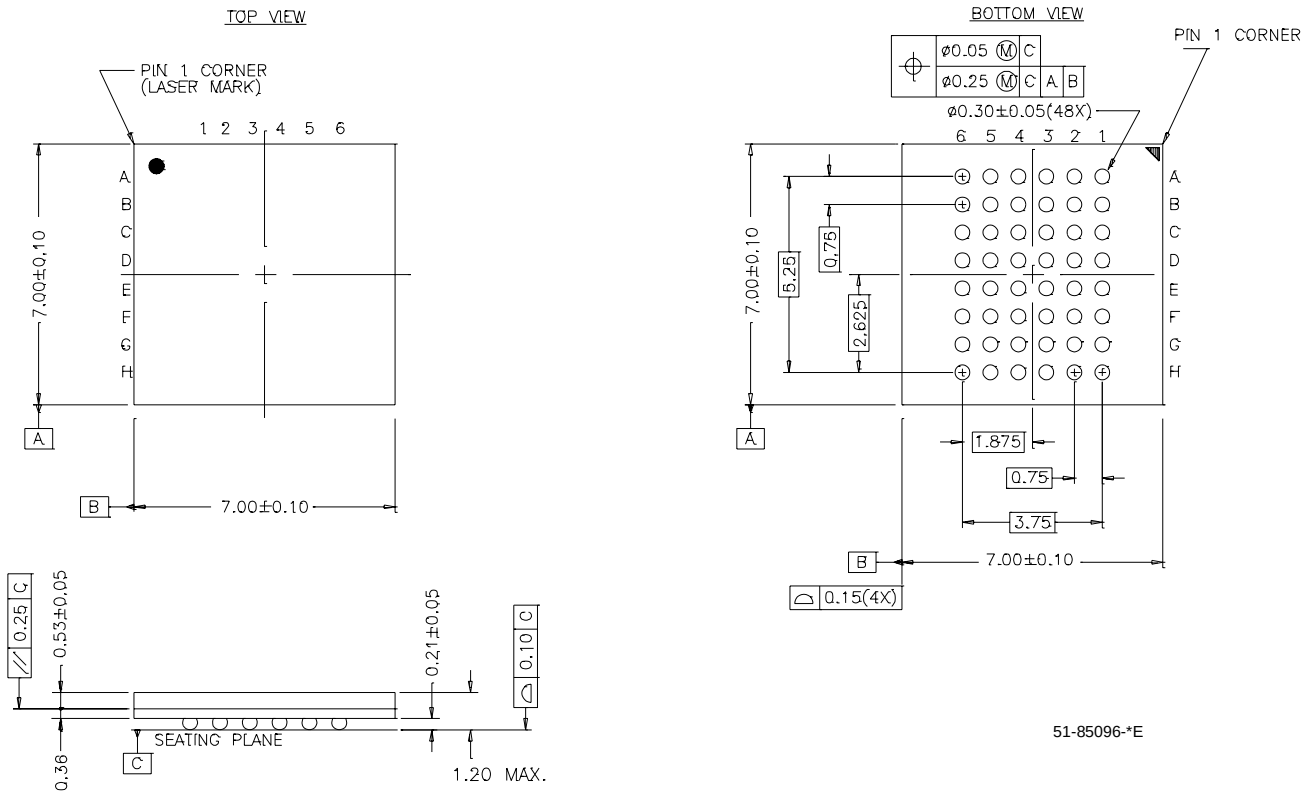
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1021BV33-8BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33-8VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-8VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-8ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-8ZC	Z44	44-Lead TSOP Type II	
10	CY7C1021BV33-10BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33-10VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-10VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-10ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-10ZC	Z44	44-Lead TSOP Type II	
12	CY7C1021BV33-12BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33-12BAI	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
	CY7C1021BV33-12VI	V34	44-Lead (400-Mil) Molded SOJ	
15	CY7C1021BV33-15BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33L-15BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY7C1021BV33-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-15ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-15VC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33-15BAI	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
	CY7C1021BV33L-15BAI	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY7C1021BV33-15VI	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-15ZI	Z44	44-Lead TSOP Type II	

Shaded areas contain advance information.

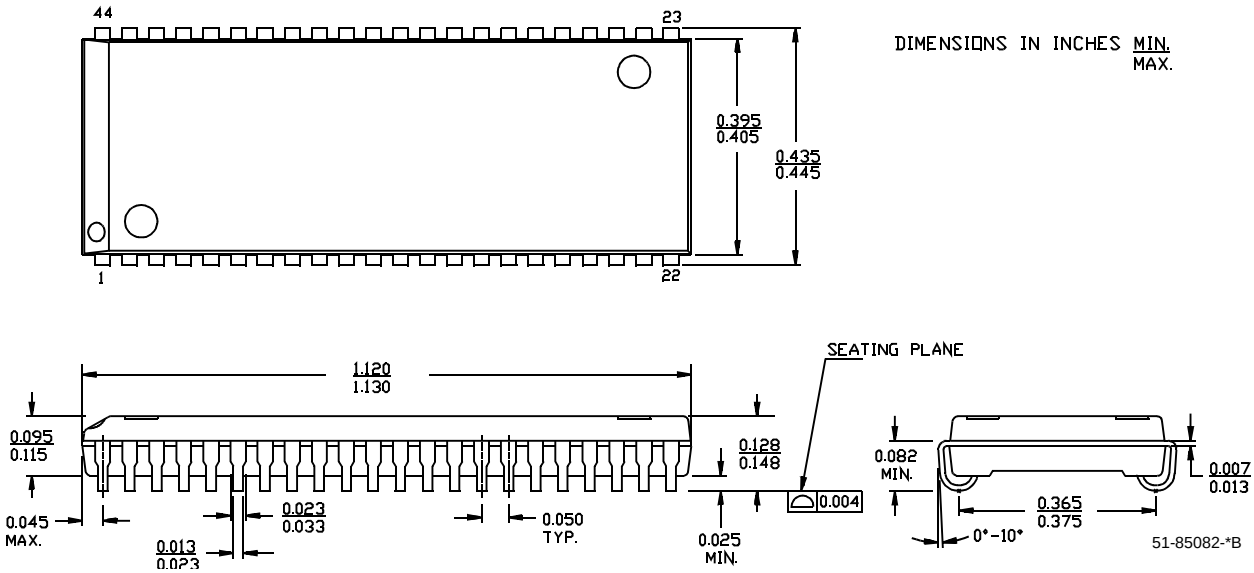
Package Diagrams

48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A

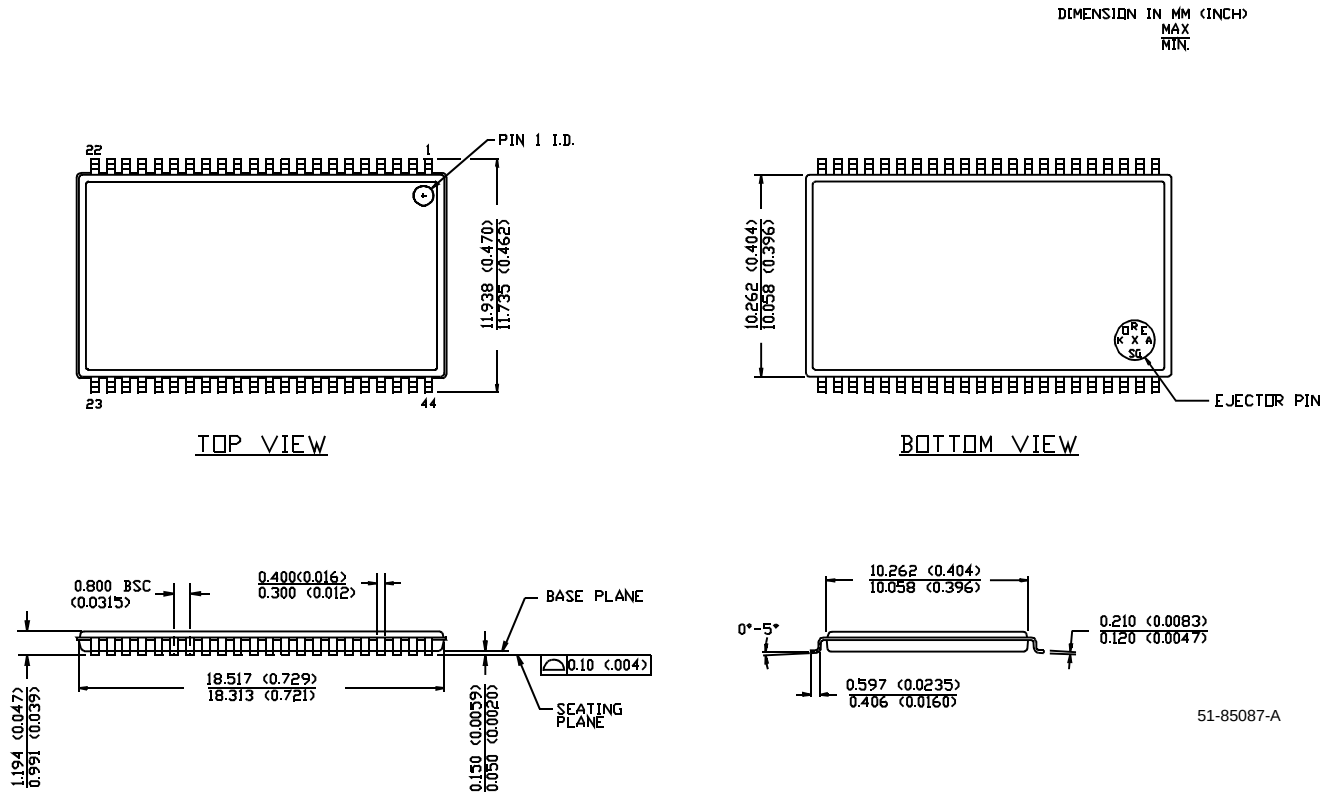


Package Diagrams (continued)

44-Lead (400-Mil) Molded SOJ V34



44-Pin TSOP II Z44



Document History Page

Document Title: CY7C1021BV33 64K x 16 Static RAM Document Number: 38-05148				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109892	09/22/01	SZV	Change from Spec number: 38-00954 to 38-05148
*A	116474	09/16/02	CEA	Add applications foot note to data sheet, page 1.