



## Preliminary 8Mb (256Kx36 & 512x18) and 4Mb (128Kx36 & 256Kx18) SRAM

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### Features

- 256K x 36 or 512K x 18 Organizations
- 128K x 36 or 256K x 18 Organizations
- 0.25 Micron CMOS Technology
- Synchronous Flow Thru Mode of Operation with Self-Timed Late Write
- Differential HSTL Input Clocks (K,  $\bar{K}$ )
- Differential HSTL Output Clocks (C,  $\bar{C}$ )
- +3.3V Power Supply, Ground, 1.6V  $V_{DDQ}$ , and 0.95V  $V_{REF}$
- HSTL Input and Output levels
- Registered Addresses, Write Enables, Synchronous Select, and Data Ins.
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary Scan Order
- Programmable Impedance Output Drivers

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### Description

The 4Mb and 8Mb SRAMs are Synchronous Flowthru Mode, high-performance CMOS Static Random Access Memories that are versatile and wide I/O, and can achieve 3ns cycle times. Differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K clock, all Addresses, Write-Enables, Sync Select, and Data Ins are registered

internally. Differential clocks C and  $\bar{C}$  are used to control the Output Data hold time by allowing output data to change after the rising edge of the C clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with HSTL I/O interface.

### x36 BGA Pinout (Top View)

|   | 1                | 2               | 3                 | 4               | 5                 | 6               | 7                |
|---|------------------|-----------------|-------------------|-----------------|-------------------|-----------------|------------------|
| A | V <sub>DDQ</sub> | SA              | SA                | NC              | SA                | SA              | V <sub>DDQ</sub> |
| B | NC               | NC              | SA                | NC              | SA                | NC,SA(8Mb)      | NC               |
| C | NC               | SA              | SA                | V <sub>DD</sub> | SA                | SA              | NC               |
| D | DQ19             | DQ18            | V <sub>SS</sub>   | ZQ              | V <sub>SS</sub>   | DQ9             | DQ10             |
| E | DQ22             | DQ20            | V <sub>SS</sub>   | $\overline{SS}$ | V <sub>SS</sub>   | DQ11            | DQb13            |
| F | V <sub>DDQ</sub> | DQ21            | V <sub>SS</sub>   | $\overline{G}$  | V <sub>SS</sub>   | DQ12            | V <sub>DDQ</sub> |
| G | DQ24             | DQ23            | $\overline{SBWc}$ | $\overline{C}$  | $\overline{SBWb}$ | DQ14            | DQb15            |
| H | DQ25             | DQ26            | V <sub>SS</sub>   | C               | V <sub>SS</sub>   | DQ17            | DQb16            |
| J | V <sub>DDQ</sub> | V <sub>DD</sub> | V <sub>REF</sub>  | V <sub>DD</sub> | V <sub>REF</sub>  | V <sub>DD</sub> | V <sub>DDQ</sub> |
| K | DQ34             | DQ35            | V <sub>SS</sub>   | K               | V <sub>SS</sub>   | DQ8             | DQ7              |
| L | DQ33             | DQ32            | $\overline{SBWd}$ | $\overline{K}$  | $\overline{SBWa}$ | DQ5             | DQ6              |
| M | V <sub>DDQ</sub> | DQ30            | V <sub>SS</sub>   | $\overline{SW}$ | V <sub>SS</sub>   | DQ3             | V <sub>DDQ</sub> |
| N | DQ31             | DQ29            | V <sub>SS</sub>   | SA              | V <sub>SS</sub>   | DQ2             | DQ4              |
| P | DQ28             | DQ27            | V <sub>SS</sub>   | SA              | V <sub>SS</sub>   | DQ0             | DQ1              |
| R | NC               | SA              | M1*               | V <sub>DD</sub> | M2*               | SA              | NC               |
| T | NC               | NC              | SA                | SA              | SA                | NC              | ZZ               |
| U | V <sub>DDQ</sub> | TMS             | TDI               | TCK             | TDO               | NC              | V <sub>DDQ</sub> |

Note: \* M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V<sub>DD</sub>.

### x18 BGA Pinout (Top View)

|   | 1                | 2               | 3                 | 4               | 5                 | 6               | 7                |
|---|------------------|-----------------|-------------------|-----------------|-------------------|-----------------|------------------|
| A | V <sub>DDQ</sub> | SA              | SA                | NC              | SA                | SA              | V <sub>DDQ</sub> |
| B | NC               | NC              | SA                | NC              | SA                | NC,SA(8Mb)      | NC               |
| C | NC               | SA              | SA                | V <sub>DD</sub> | SA                | SA              | NC               |
| D | DQ14             | NC              | V <sub>SS</sub>   | ZQ              | V <sub>SS</sub>   | DQ0             | NC               |
| E | NC               | DQ15            | V <sub>SS</sub>   | $\overline{SS}$ | V <sub>SS</sub>   | NC              | DQ1              |
| F | V <sub>DDQ</sub> | NC              | V <sub>SS</sub>   | $\overline{G}$  | V <sub>SS</sub>   | DQ2             | V <sub>DDQ</sub> |
| G | NC               | DQ16            | $\overline{SBWb}$ | $\overline{C}$  | NC                | NC              | DQ3              |
| H | DQ17             | NC              | V <sub>SS</sub>   | C               | V <sub>SS</sub>   | DQ4             | NC               |
| J | V <sub>DDQ</sub> | V <sub>DD</sub> | V <sub>REF</sub>  | V <sub>DD</sub> | V <sub>REF</sub>  | V <sub>DD</sub> | V <sub>DDQ</sub> |
| K | NC               | DQ13            | V <sub>SS</sub>   | K               | V <sub>SS</sub>   | NC              | DQ8              |
| L | DQ12             | NC              | NC                | $\overline{K}$  | $\overline{SBWa}$ | DQ7             | NC               |
| M | V <sub>DDQ</sub> | DQ10            | V <sub>SS</sub>   | $\overline{SW}$ | V <sub>SS</sub>   | NC              | V <sub>DDQ</sub> |
| N | DQ11             | NC              | V <sub>SS</sub>   | SA              | V <sub>SS</sub>   | DQ6             | NC               |
| P | NC               | DQ9             | V <sub>SS</sub>   | SA              | V <sub>SS</sub>   | NC              | DQ5              |
| R | NC               | SA              | M1                | V <sub>DD</sub> | M2                | SA              | NC               |
| T | NC               | SA              | SA                | NC              | SA                | SA              | ZZ               |
| U | V <sub>DDQ</sub> | TMS             | TDI               | TCK             | TDO               | NC              | V <sub>DDQ</sub> |

Note: \* M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V<sub>DD</sub>.



## Pin Description

|               |   |              |                                 |
|---------------|---|--------------|---------------------------------|
| SA0-SA18      | Address Input<br>SA0-SA18 for 512Kx18<br>SA0-SA17 for 256Kx36<br>SA0-SA17 for 256Kx18<br>SA0-SA16 for 128Kx36 | $\bar{G}$    | Asynchronous Output Enable      |
| DQ0-DQ35      | Data I/O<br>DQ0-DQ17 for 512Kx18<br>DQ0-DQ35 for 256Kx36  | $\bar{SS}$   | Synchronous Select              |
| K, $\bar{K}$  | Differential Input Register Clocks  | M1, M2       | Clock Mode Inputs.              |
| C, $\bar{C}$  | Differential Output Data Hold Control Clocks  | $V_{REF(2)}$ | HSTL Input Reference Voltage    |
| $\bar{SW}$    | Write Enable, Global  | $V_{DD}$     | Power Supply (+3.3V)            |
| $\bar{SBW}_a$ | Write Enable, Byte a (DQ0-DQ8)  | $V_{SS}$     | Ground                          |
| $\bar{SBW}_b$ | Write Enable, Byte b (DQ9-DQ17)   | $V_{DDQ}$    | Output Power Supply             |
| $\bar{SBW}_c$ | Write Enable, Byte c (DQ18-DQ26)  | ZZ           | Asynchronous Sleep Mode         |
| $\bar{SBW}_d$ | Write Enable, Byte d (DQ27-DQ35)  | ZQ           | Output Driver Impedance Control |
| TMS,TDI,TCK   | IEEE 1149.1 Test Inputs (LVTTTL levels)   | NC           | No Connect                      |
| TDO           | IEEE 1149.1 Test Output (LVTTTL level)  |              |                                 |

## Ordering Information (These are all possible sorts; some may not be qualified.)

| Part Number         | Organization | Speed                      | Leads      |
|---------------------|--------------|----------------------------|------------|
| IBM0418A40QLAB - 3T | 256K x 18    | 4.2ns Access / 3.3ns Cycle | 7 x 17 BGA |
| IBM0418A40QLAB - 3S |              | 4.5ns Access / 3.6ns Cycle |            |
| IBM0418A40QLAB - 3E |              | 5.0ns Access / 3.8ns Cycle |            |
| IBM0418A40QLAB - 4T |              | 5.5ns Access / 4.2ns Cycle |            |
| IBM0436A40QLAB - 3T | 128K x 36    | 4.2ns Access / 3.3ns Cycle |            |
| IBM0436A40QLAB - 3S |              | 4.5ns Access / 3.6ns Cycle |            |
| IBM0436A40QLAB - 3E |              | 5.0ns Access / 3.8ns Cycle |            |
| IBM0436A40QLAB - 4T |              | 5.5ns Access / 4.2ns Cycle |            |
| IBM0418A80QLAB - 3T | 512K x 18    | 4.2ns Access / 3.3ns Cycle |            |
| IBM0418A80QLAB - 3S |              | 4.5ns Access / 3.6ns Cycle |            |
| IBM0418A80QLAB - 3E |              | 5.0ns Access / 3.8ns Cycle |            |
| IBM0418A80QLAB - 4T |              | 5.5ns Access / 4.2ns Cycle |            |
| IBM0436A80QLAB -3T  | 256K x 36    | 4.2ns Access / 3.3ns Cycle |            |
| IBM0436A80QLAB -3S  |              | 4.5ns Access / 3.6ns Cycle |            |
| IBM0436A80QLAB -3E  |              | 5.0ns Access / 3.8ns Cycle |            |
| IBM0436A80QLAB -4T  |              | 5.5ns Access / 4.2ns Cycle |            |



## Revision Log

| Revision | Contents of Modification           |
|----------|------------------------------------|
| 11/98    | Initial release.                   |
| 7/99     | Corrected BGA Dimension on page 28 |

For a complete datasheet, please contact your IBM sale representative.



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