ANALOG DEVICES

14- & 16-Bit, Hybrid Digital-to-Resolver Converter

DRC1765, DRC1766

FEATURES

- Single Rank Transparent LS or CMOS Latched Inputs Registers With High and Low Byte ENABLE
- 14- or 16-Bit Resolution
- ±2 or ±4 Arc-Minutes Accuracy
- Very Low dc Offset Voltage
- 4.3mA Peak Output Will Drive Resistive, Inductive or Capacitive Load
- Low Radius Vector Variation (Transformation Ratio). (0.03%)
- CMOS Version Requires Only ±15V Supplies
- Low Power Dissipation (CMOS Option)
- DC to 2.6kHz Operation
- Single 32 Pin Package
- Protection Against +200% Overload On Analog Input

APPLICATIONS

- Polar to Rectangular Coordinate Conversion
- Missile and Fire Control Systems
- Simulators
- Low Frequency Oscillators
- PPI Displays
- Radar and Navigational Systems
- Axis Rotation
- Avionics

GENERAL DESCRIPTION

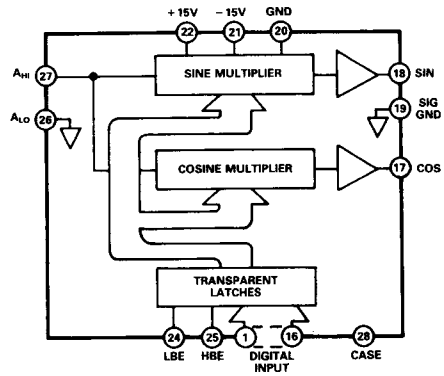
The DRC1765 and DRC1766 are hybrid digital to resolver converters which accept a 14-bit or 16-bit digital input work representing angle and output Sine and Cosine voltages which are multiplied by an analog input reference voltage. The analog input voltage can either be dc or ac voltage of frequency up to 2.6kHz.

The digital input to the converter is latched with a transparent high and low byte ENABLE system to facilitate easy interfacing to microprocessor systems. The input latches can be CMOS or Low Power Schottky.

The units are available in accuracy grades of ±2 and ±4 arc-minutes.

A particular feature of the converters is their low dc output offset voltage (±2mV typ). This compares very favorably

DRC1765, DRC1766 FUNCTIONAL BLOCK DIAGRAM



with similar products on the market where the offset voltage can be as high as ±50mV. This low offset voltage means that external trim adjustments are not required which is particularly important in display applications.

The converters have a closed loop bandwidth of 300kHz and are able to drive into a load which can be inductive, resistive or capacitive to the extent of 15nF.

A further feature of the converters is that the radius vector variation (transformation ratio) is very low at 0.03%. This means that the individual Sine and Cosine outputs are independently accurate which is important in coordinate conversion or display applications.

The power consumption of the DRC1765 and DRC1766 is particularly low in the case of the CMOS latch option which only requires ±15 volts power rails.

The converters are housed in a 32-pin triple DIP hybrid package and hermetically sealed.

MODELS AVAILABLE

The DRC1765 (14-bit resolution) is available with accuracies of ±2 or ±4 arc-minutes. The DRC1766 (16-bit resolution) is available with accuracies of ±2 or ±4 arc-minutes. Both models offer a choice of LS or CMOS logic inputs.

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SPECIFICATIONS (typical @ 25°C, unless otherwise stated)

Models	DRC1765	DRC1766
DIGITAL INPUT RESOLUTION	14 Bits (1.3 arc-minutes)	16 Bits (0.33 arc-minutes)
DIGITAL INPUT FORMAT	Parallel natural binary. TTL compatible. Includes internal pull ups of 27kΩ.	*
RECOMMENDED ANALOG INPUT (V_{REF})	3.4 Volts rms	*
OUTPUT (SINE AND COSINE) WITH RECOMMENDED ANALOG INPUT	6.8 Volts rms ±0.1%	*
OUTPUT TEMPERATURE COEFFICIENT	5ppm/°C of FSR (typ) 25ppm/°C of FSR (max)	* *
ANALOG INPUT FREQUENCY RANGE	dc to 2.6kHz	*
ANALOG INPUT IMPEDANCE	10.2kΩ	*
ANALOG OUTPUT IMPEDANCE	20mΩ (max) 2mΩ (typ)	* *
ANALOG OFFSET VOLTAGE	±2mV (typ) ±12mV (max)	* *
OUTPUT DRIVE CAPABILITY	4.3mA peak @ ±10V peak	*
OUTPUT PROTECTION	Any one output may be grounded indefinitely	*
RESPONSE TO A STEP INPUT	20μs (max) to within accuracy of converter. Any size step input.	*
VECTOR ACCURACY		
Radius Error	0.03%	*
Angular Error	±2, ±4 minutes	*
POWER SUPPLIES		
CMOS Options		
+15 Volts	18mA (typ) 26mA (max)	*
−15 Volts	15mA (typ) 23mA (max)	*
LS Options		
+15 Volts	18mA (typ) 25mA (max)	*
−15 Volts	15mA (typ) 23mA (max)	*
+5 Volts	43mA (typ) 80mA (max)	*
TEMPERATURE RANGE		
Operating	−55°C to +125°C	*
Storage	−65°C to +150°C	*
DIMENSIONS	1.74" × 1.14" × 0.28"	*
PACKAGE TYPE[1]	32-pin triple DIP – HY32C	*
WEIGHT	20 grams (typ)	*

NOTES
[1]See Section 19 for package outline information.
*Specifications same as DRC1765.
Specifications subject to change without notice.

THEORY OF OPERATION

The block diagram below illustrates the operation of the DRC1765 and DRC1766.

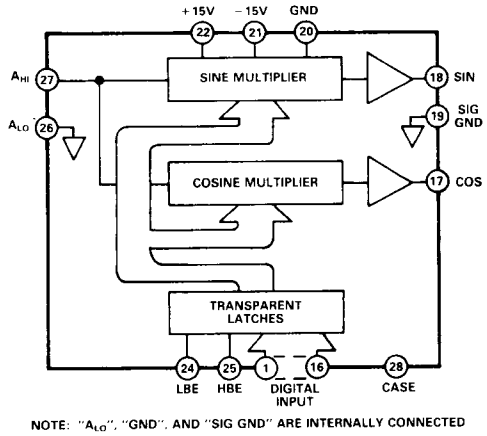


Figure 1. Theory of Operation

An input signal applied between A_{HI} (analog input HI) and A_{LO} (analog input LO) is multiplied by both sineθ and cosineθ where θ is represented by a digital input word.

The resulting outputs at pins Sin and Cos are;

V_O Sin = $2V_i$ Sinθ
V_O Cos = $2V_i$ Cosθ

All the signal inputs and outputs are referred to the SIG GND.

CONNECTING THE CONVERTER

The connections to the DRC1765 and DRC1766 are very straightforward.

The digital inputs should be connected to the converter using pins 1 (MSB) through 14 (LSB) in the case of the DRC1765 and through 16 (LSB) in the case of the DRC1766. The format of the digital angular input is shown under the "Bit Weight Table" section on this page.

The digital input control lines should be connected as described under the "Digital Data Input" section.

A_{LO} and A_{HI} are for the analog input reference voltage (V_{REF}). It should be noted that this is a single ended input where A_{LO} is grounded internally. If it is desired, the V_{REF} input can be externally isolated using the STM1680 transformer. See the section on Reference Transformer.

The "Case" pin is joined to the case which is isolated and should be connected to a convenient zero potential point in the system.

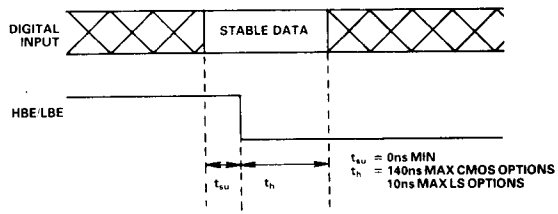
The sine and cosine outputs are taken from the "Sin" and "Cos" pins with "SIG GND" as the common connection.

DIGITAL DATA INPUT

The digital input to the converters is internally buffered by transparent latches. The latches can be CMOS (type 54C373) or low power Schottky (LS) (type 54LS373) depending on the option.

The "HBE" input controls the input of the most significant 8-bit and the "LBE" input controls the input of the least significant bit (6 in the case of the DRC1765 and 8 in the case of the DRC1766).

A logic "Hi" on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital input. When "HBE" and "LBE" are taken to a logic "Lo" state the converter output will be latched at the level of the data present on the input at the low going edge and remains constant until "HBE" and "LBE" are taken to a "Hi" state again. If the latches are not required, "HBE" and "LBE" can be left open circuit. The timing diagram in Figure 2 illustrates the use of "HBE" and "LBE".



NOTE: INTERNAL LATCHES ARE: 54LS373 (LS) 54C373 (CMOS)

Figure 2. Data Transfer Diagram

Internal resistive pull-ups (to +5V using 27k resistors) are employed on all digital inputs. This ensures full TTL compatibility for either latch option even when sourcing 50μA of leakage current in each external digital driver.

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB DRC1765)	0.0220
15	0.0110
16 (LSB DRC1766)	0.0055

VECTOR ERRORS AND EFFECTS

The conversion technique has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the internal components used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays, or metal cutting control where perfect circles have to be generated.

BANDWIDTH

The open loop gain bandwidth product of the DRC1765 and DRC1766 has been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6kHz. This results in a closed loop bandwidth of 300kHz.

DEGLITCHING THE CONVERTERS

The DRC1765 and DRC1766 are fundamentally digital to analog converters and can, therefore, produce glitches on the output at the major transition points of the digital input. For most applications these glitches can be removed by simple smoothing circuits on the outputs. However, in applications where the smoothing is not an acceptable solution, sample and hold amplifiers such as the Analog Devices type AD582 can be used to remove the glitches.

ABSOLUTE MAXIMUM INPUTS

A_{HI} to A_{LO}	$\pm V_{SUPPLY}$
+15V Pin	+17V
−15V Pin	−17V
+5V Pin (LS Option)	−0.4V to +7V
Case to GND	±20V
Any Logical Input	−0.4V to +5.5V

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of voltage.

A resistance of value 3kΩ per extra volt required should be inserted in the A_{HI} line. Care should be taken to ensure that the voltage on the analog input (A_{HI}, A_{LO}) is 3.4 volts rms in order to provide a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and, therefore, the resistor tolerance should be chosen so that the correct voltage appears across the A_{HI}, A_{LO} pins.

REFERENCE INPUT TRANSFORMER

Input Voltage (R_{HI}, R_{LO})	11.8, 26, 115 volts rms depending on option (+10% max voltage)
Output Voltages (A_{HI}, A_{LO})	3.4 volts rms ±0.1%
Frequency Range	360 to 2600 Hz
Input Impedance 11.8V input	5kΩ (min)

ORDERING INFORMATION

The converter part number should be suffixed with an option code as shown below in order to fully specify the device.