
2-Wire Automotive Serial EEPROM
64-Kbit (8,192 x 8)

DATASHEET

Features

- Standard-Voltage Operation
 - 2.7 ($V_{CC} = 2.7V$ to $5.5V$)
- Internally Organized 8,192 x 8 (64K)
- Automotive Temperature Range $-40^{\circ}C$ to $+125^{\circ}C$
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400kHz Clock Rate
- Write Protect Pin for Hardware Data Protection
- 32-byte Page Write Mode (Partial Page Writes Allowed)
- Self-timed Write Cycle (5ms Max)
- High Reliability
 - Endurance: 1,000,000 Write Cycles
 - Data Retention: 100 Years
- Lead-free/Halogen-free Devices Available
- 8-lead JEDEC SOIC and 8-lead TSSOP Packages

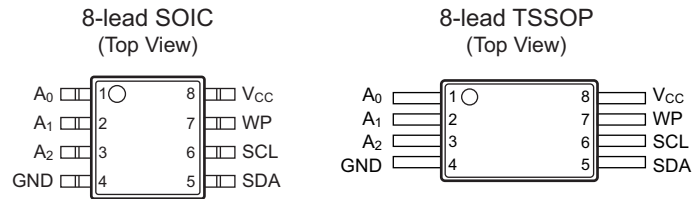
Description

The Atmel® AT24C64B provides 65,536 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 8,192 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many automotive applications where low power and low voltage operation are essential. The AT24C64B is available in space saving 8-lead JEDEC SOIC and 8-lead TSSOP packages and is accessed via a 2-wire serial interface and is available in a 2.7V (2.7V to 5.5V) version.

1. Pin Configurations and Pinouts

Figure 1. Pin Configurations

Pin Name	Function
A ₀ – A ₂	Address Inputs
GND	Ground
V _{CC}	Power Supply
WP	Write Protect
SCL	Serial Clock Input
SDA	Serial Data



Note: Drawings are not to scale.

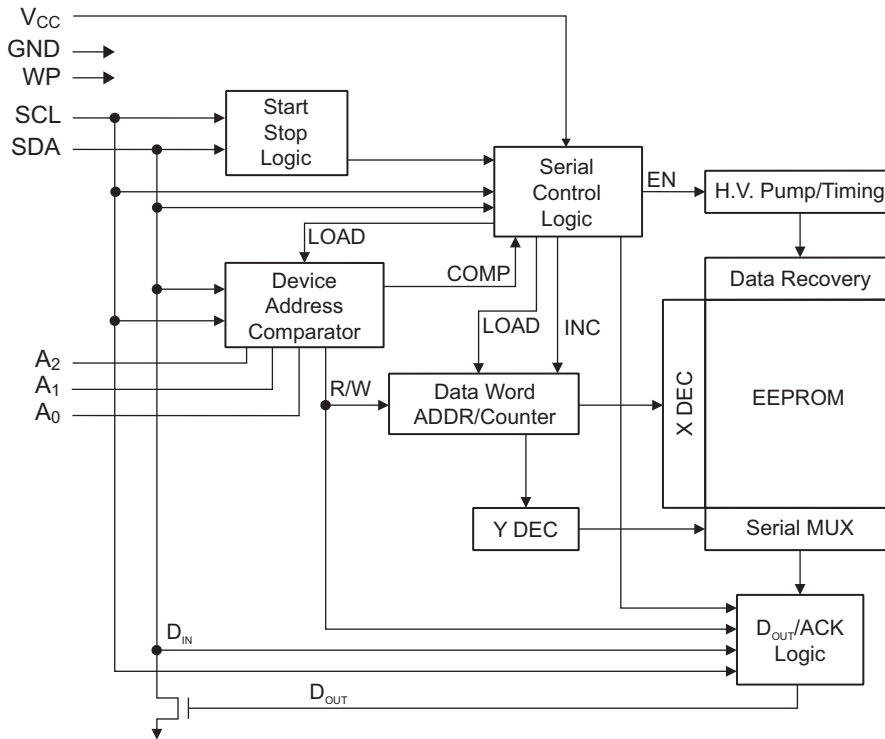
2. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Device Address (A_2 , A_1 , and A_0): The A_2 , A_1 , and A_0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other AT24Cxx devices. When the pins are hardwired, as many as eight 64K devices may be addressed on a single bus system (see Section 7., “Device Addressing”). If the pins are left floating, the A_2 , A_1 , and A_0 pins will internally be pulled down to Ground (GND) if the capacitive coupling to the circuit board V_{CC} plane is less than 3pF. If coupling is greater than 3pF, Atmel recommends connecting the address pins to GND.

Write Protect (WP): The Write Protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{CC} , all write operations to upper quadrant of the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is less than 3pF. If coupling is greater than 3pF, Atmel recommends connecting the pin to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

5. Memory Organization

AT24C64B, 64K Serial EEPROM: The 64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 13-bit data word address.

5.1 Pin Capacitance

Table 5-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = 5.5\text{V}$.

Symbol	Test Condition	Max]	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance ($A_0, A_1, A_2, \text{SCL}$)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

5.2 DC Characteristics

Table 5-2. DC Characteristics

Applicable over recommended operating range from: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC3}	Supply Voltage		2.7		5.5	V
I_{CC1}	Supply Current	$V_{CC} = 5.0\text{V}$ Read at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current	$V_{CC} = 5.0\text{V}$ Write at 400kHz		2.0	3.0	mA
I_{SB}	Standby Current	$V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}	1.0	3.0	μA
		$V_{CC} = 5.0\text{V}$		3.0	5.0	
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
$V_{IL}^{(1)}$	Input Low Level		-0.6		$V_{CC} \times 0.3$	V
$V_{IH}^{(1)}$	Input High Level		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level	$V_{CC} = 3.0\text{V}$ $I_{OL} = 2.1\text{mA}$			0.4	V
V_{OL1}	Output Low Level	$V_{CC} = 1.8\text{V}$ $I_{OL} = 0.15\text{mA}$			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

5.3 AC Characteristics

Table 5-3. AC Characteristics

Applicable over recommended operating range from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$, $CL = 1$ TTL Gate and 100pF (unless otherwise noted).

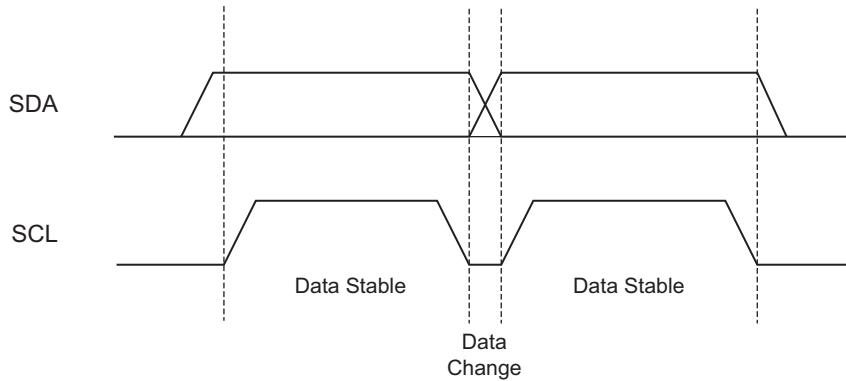
Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		μs
t_{HIGH}	Clock Pulse Width High	0.6		μs
t_I	Noise Suppression Time ⁽¹⁾		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	μs
t_{BUF}	Time the bus must be free before a new transmission can start ⁽¹⁾	1.2		μs
$t_{HD.STA}$	Start Hold Time	0.6		μs
$t_{SU.STA}$	Start Set-up Time	0.6		μs
$t_{HD.DAT}$	Data In Hold Time	0		μs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
$t_R^{(1)}$	Inputs Rise Time		0.3	μs
$t_F^{(1)}$	Inputs Fall Time		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		μs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance ⁽¹⁾	5.0V, 25°C , Page Mode	1,000,000		Write Cycles

Note: 1. This parameter is ensured by characterization only.

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Data Validity timing diagram). Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

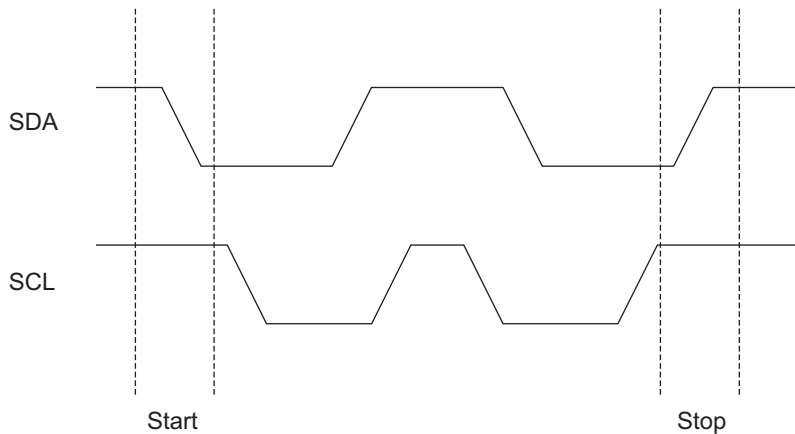
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

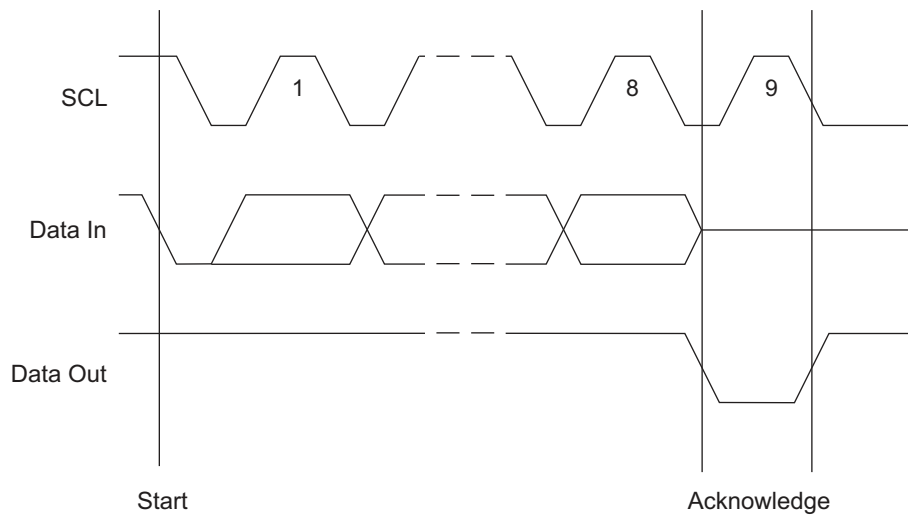
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop condition will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Figure 6-3. Output Acknowledge



Standby Mode: The AT24C64B features a low power standby mode which is enabled:

- Upon power-up.
- After the receipt of the Stop condition and the completion of any internal operations.

Memory Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

- Clock up to nine cycles,
- Look for SDA high in each cycle while SCL is high, and
- Create a Start condition as SDA is high.

The device is ready for the next communication after above steps have been completed.

Figure 6-4. Memory Reset

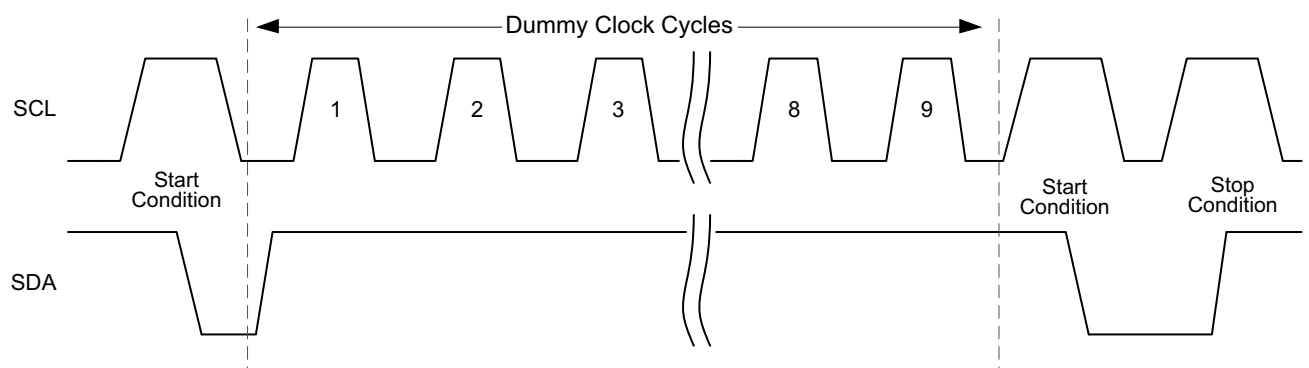


Figure 6-5. Bus Timing — SCL: Serial Clock, SDA: Serial Data I/O

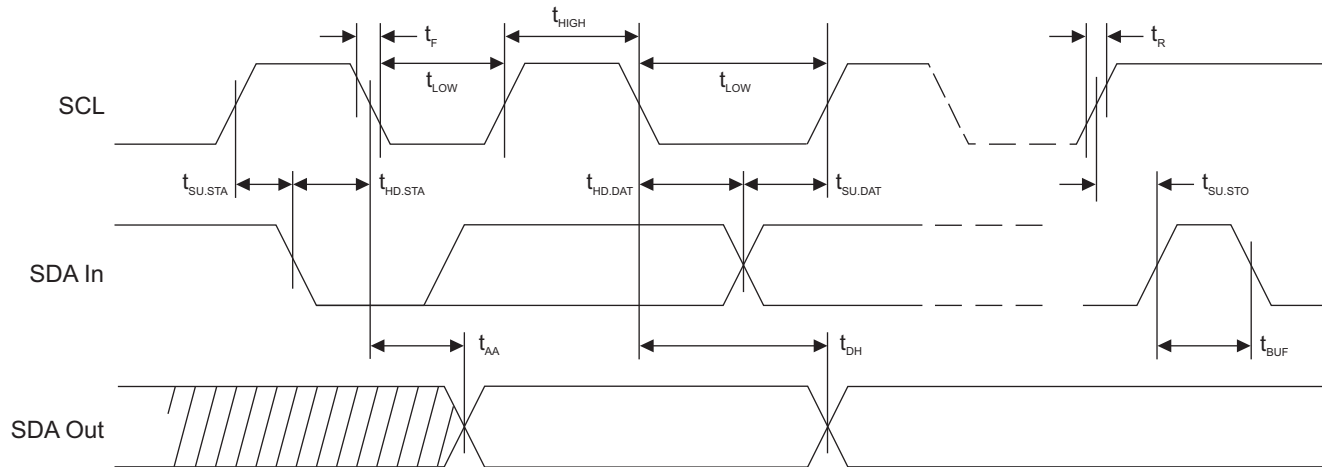
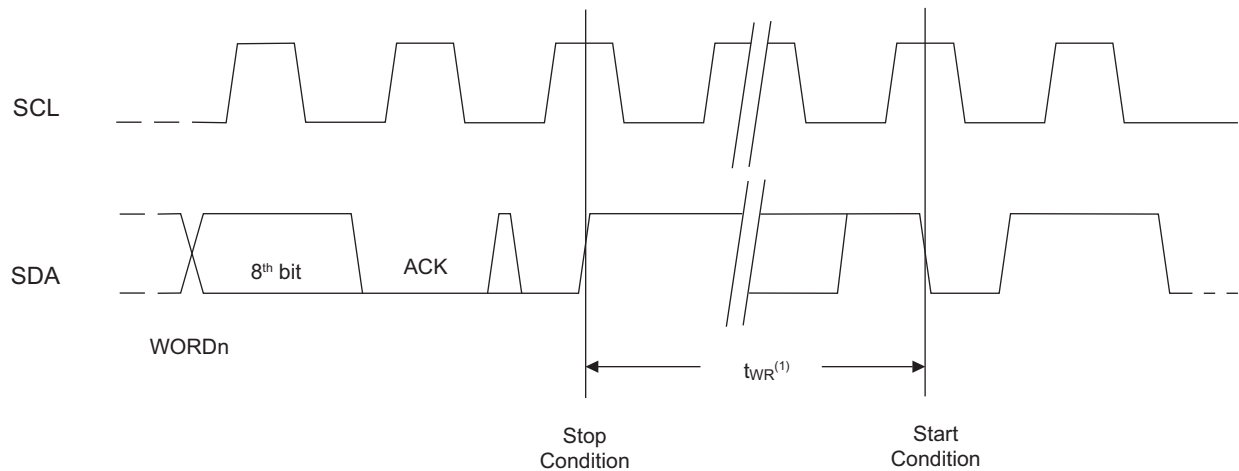


Figure 6-6. Write Cycle Timing — SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

7. Device Addressing

The 64K EEPROM requires an 8-bit device address word following a Start condition to enable the device for a Read or Write operation. The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 64K uses the three device address bits A₂, A₁, and A₀ to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A₂, A₁, and A₀ pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

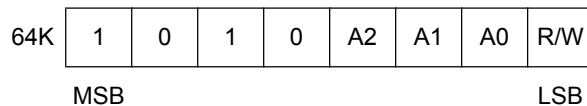
The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is high, and a Write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

Noise Protection: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

Data Security: The AT24C64B has a hardware data protection scheme that allows the user to write protect the upper quadrant of memory when the WP pin is at V_{CC}.

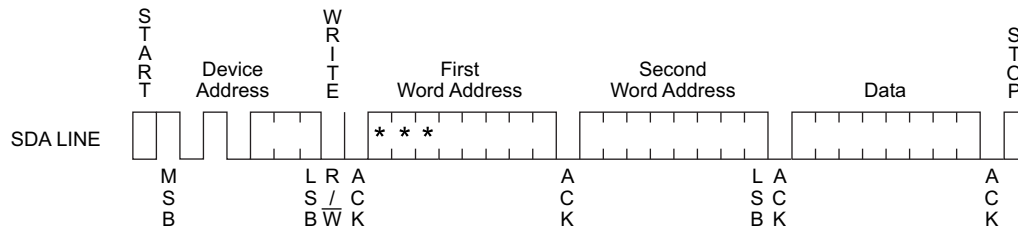
Figure 7-1. Device Address



8. Write Operations

Byte Write: A Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

Figure 8-1. Byte Write



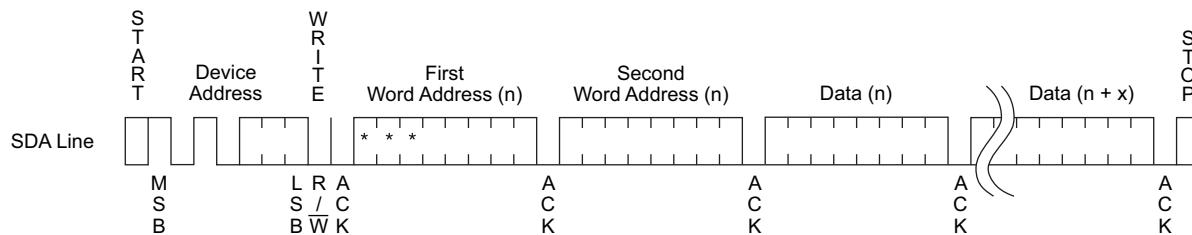
Note: 1. * = Don't care bit.

Page Write: The 64K EEPROM is capable of 32-byte Page Writes.

A Page Write is initiated the same way as a byte write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will roll-over and previous data will be overwritten.

Figure 8-2. Page Write



Note: 1. * = Don't care bit.

Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

9. Read Operations

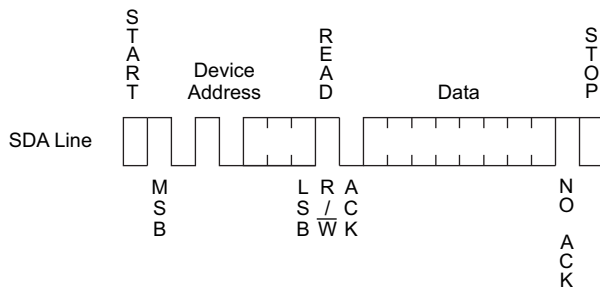
Read operations are initiated the same way as write operations with the exception that the Read/write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as the device power is maintained. The address roll-over during read is from the last byte of the last memory page, to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

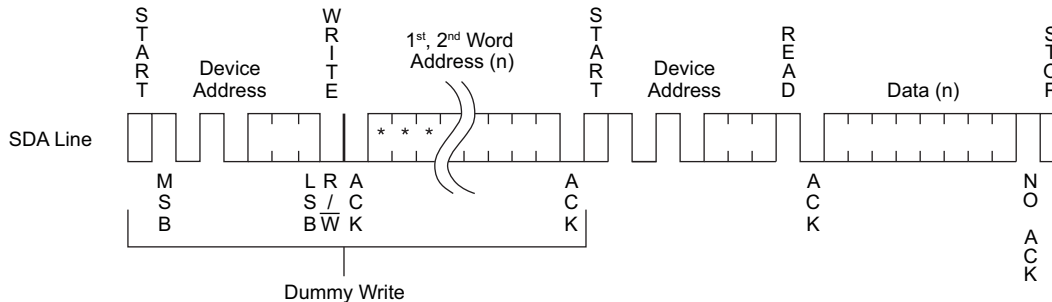
Once the device address with the Read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following Stop condition.

Figure 9-1. Current Address Read



Random Read: A Random Read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a Current Address Read by sending a device address with the Read/Write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following Stop condition.

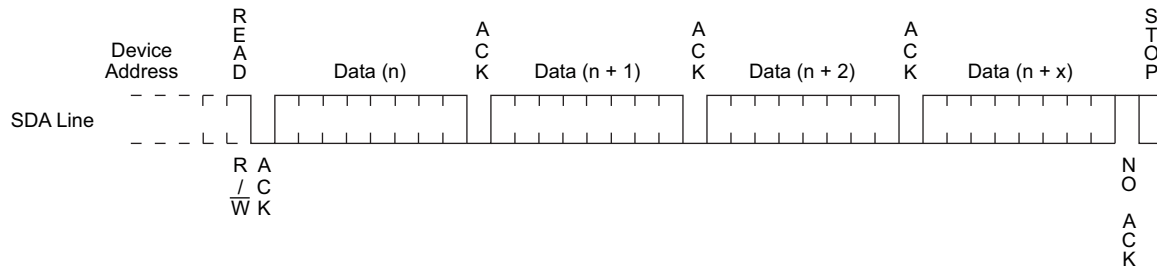
Figure 9-2. Random Read



Note: 1. * = Don't care bit.

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

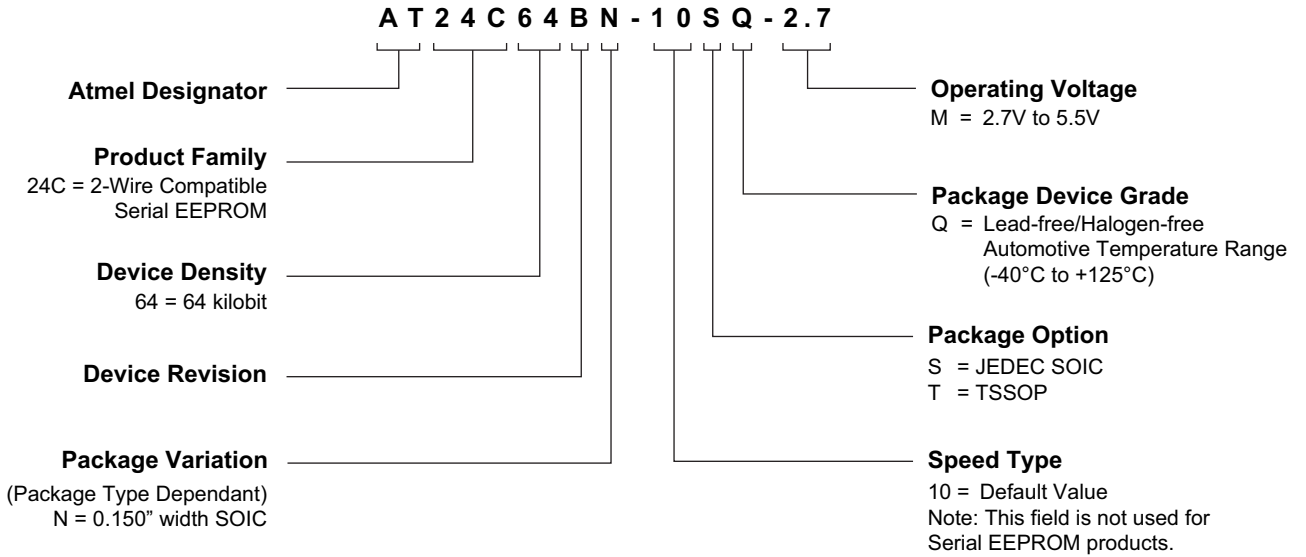
Figure 9-3. Sequential Read



10. Power Recommendation

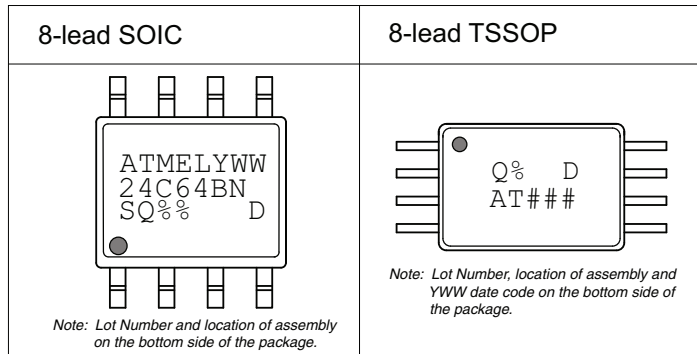
The device internal POR (Power-On Reset) threshold is just below the minimum operating voltage of the device. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100 μ s before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is not recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

11. Ordering Code Detail



12. Product Markings

AT24C64B Automotive Package Marking Information



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT24C64B		Truncation Code ###: 64B	
Date Codes			Voltagages
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014 8: 2018	A: January	02: Week 2	3 or 27: 2.7V min
5: 2015 9: 2019	B: February	04: Week 4	
6: 2016 0: 2020	
7: 2017 1: 2021	L: December	52: Week 52	
Country of Assembly		Lot Number	Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	Q: Automotive /Matte Tin/SnAgCu
Trace Code			Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

6/12/14

<p>Package Mark Contact: DL-CSO-Assy_eng@atmel.com</p>	TITLE 24C64BAM , AT24C64B Automotive Package Marking Information	DRAWING NO.	REV.
		24C64BAM	C

13. Ordering Information⁽¹⁾

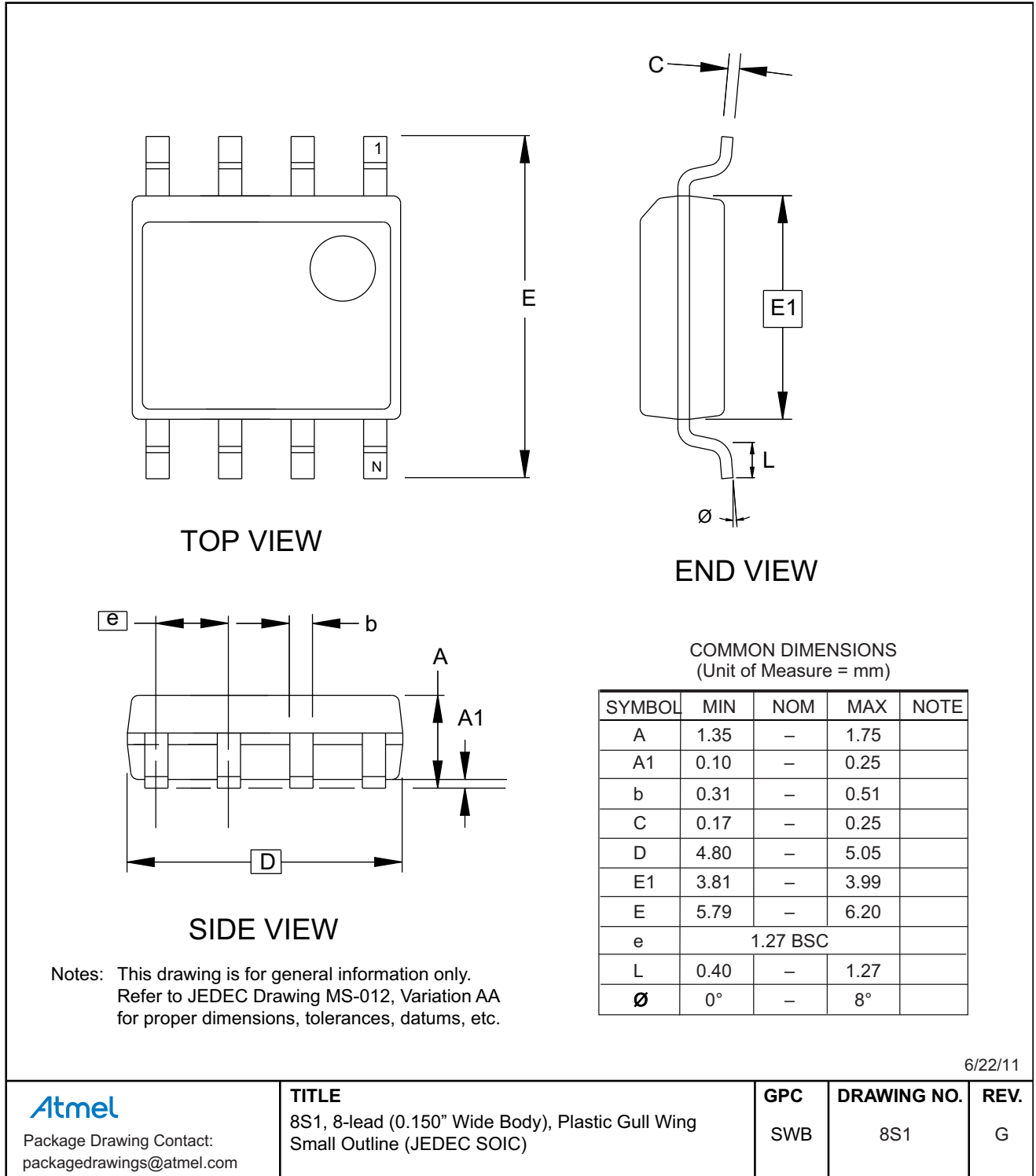
Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT24C64BN-10SQ-2.7 ⁽²⁾	Matte Tin (Lead-free/Halogen-free)	8S1	2.7V to 5.5V	Automotive Temperature (-40°C to +125°C)
AT24C64B-10TQ-2.7 ⁽²⁾		8X		

- Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC characteristics tables.
 2. "Q" designates green package and RoHS compliant.

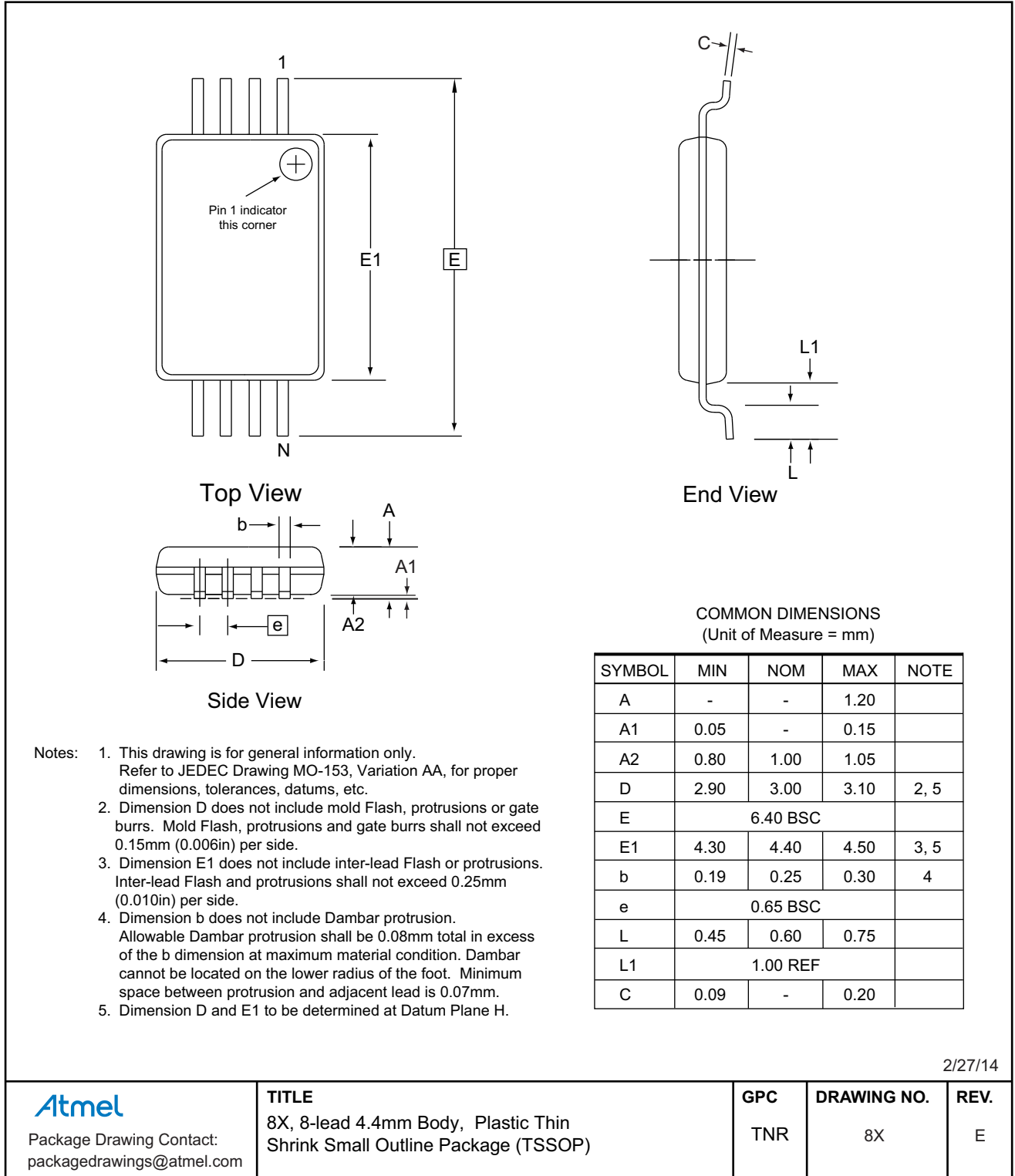
Package Type	
8S1	8-lead, 0.150" wide body, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)

14. Package Drawings

14.1 8S1 — 8-lead JEDEC SOIC



14.2 8X — 8-lead TSSOP



15. Revision History

Revision	Date	Comments
8778B	08/2014	Add the sections, power recommendation and ordering code detail. Updated part markings, template, logos, and disclaimer page. No changes to functional specification.
8778A	09/2011	Initial document release.



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