

Q

# High Speed CMOS Dual Binary 1-of-4 Decoders

QS54/74FCT139T  
QS54/74FCT239T

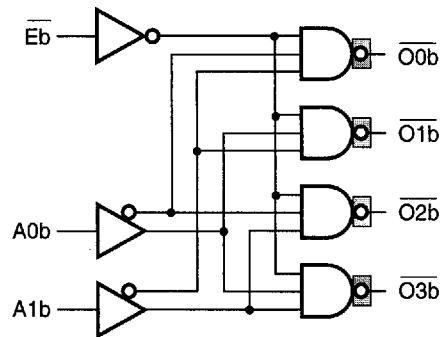
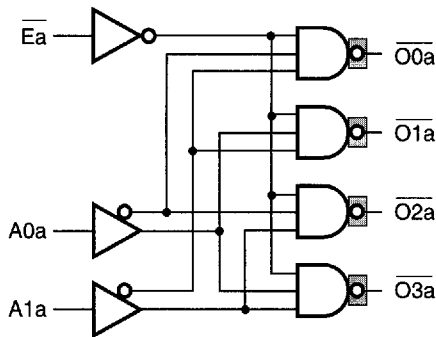
## FEATURES/BENEFITS

- QSFCT139D with 4.0 ns propagation delay
- $I_{OL} = 48 \text{ mA COM}, 32 \text{ mA MIL}$
- TTL-compatible input and output levels
- Mil product compliant with MIL-STD 883, Class B
- QSFCT239T has positive active outputs
- CMOS power levels  $< 7.5 \text{ mW static}$
- Available in DIP, SOIC, QSOP, HQSOP, ZIP
- JEDEC standard pinouts

## DESCRIPTION

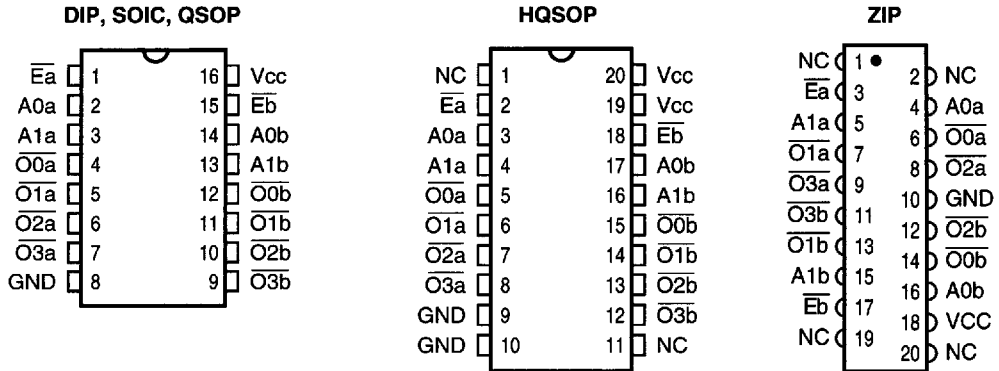
The QSFCT139T and QSFCT239T are high-speed CMOS TTL-compatible high-speed binary decoders. The QSFCT139T has negative active outputs, and the QSFCT239T has positive active outputs. The high output current  $I_{OL}$  and  $I_{OH}$  drive high-capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



Inverting Outputs on 139 Only  
(Non-inverting Outputs on 239)

**PIN CONFIGURATIONS (All Pins Top View)**



**Note:** Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

**PIN DESCRIPTION**

Name	I/O	Description
Ai	I	Select Inputs
$\bar{O}i$	O	Decode Outputs
$\bar{E}i$	I	Enable

**FUNCTION TABLE**

Enable $\bar{E}a, \bar{E}b$	Select		FCT139 Output				FCT239 Output				Note
	A1	A0	$\bar{O}3$	$\bar{O}2$	$\bar{O}1$	$\bar{O}0$	O3	O2	O1	O0	
H	X	X	H	H	H	H	L	L	L	L	Disable Decode
L	L	L	H	H	H	L	L	L	L	H	A1-0 = 0
L	L	H	H	H	L	H	L	L	H	L	A1-0 = 1
L	H	L	H	L	H	H	L	H	L	L	A1-0 = 2
L	H	H	L	H	H	H	H	L	L	L	A1-0 = 3

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-3	4	4	5	7	pF
7, 9-12	6	6	7	9	pF
4-6, 13-15	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18$ mA, $T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12$ mA (MIL) $I_{OH} = -15$ mA (COM)	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 32$ mA (MIL) $I_{OL} = 48$ mA (COM)	— —	— —	0.50 0.50	V

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

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**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = Max., freq = 0 0V ≤ V <sub>IN</sub> ≤ 0.2V or V <sub>cc</sub> -0.2V ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	—	1.5	mA
ΔI <sub>cc</sub>	Supply Current per Input @ TTL HIGH	V <sub>cc</sub> = Max., V <sub>IN</sub> = 3.4V, freq = 0 <sup>(2)</sup>	—	2.0	mA
Q <sub>ccd</sub>	Supply Current per Input per MHz	V <sub>cc</sub> = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V <sub>cc</sub> <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V<sub>IN</sub> = 3.4V).
3. For flip-flops, Q<sub>ccd</sub> is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I<sub>c</sub> can be computed using the above parameters as explained in the Technical Overview section.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial T<sub>A</sub> = 0°C to 70°C, V<sub>cc</sub> = 5.0V ± 5%      Military T<sub>A</sub> = -55°C to 125°C, V<sub>cc</sub> = 5.0V ± 10%  
 C<sub>LOAD</sub> = 50 pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Description <sup>(1)</sup>		139 239		139A 239A		139C 239C		139D 239D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	Com	1.5	9	1.5	5.8	1.5	5.0	1.0	4.0	ns
t <sub>PLH</sub>	A <sub>i</sub> to $\overline{O}_i$	Mil	1.5	12	1.5	7.8	1.5	7.0	—	—	
t <sub>PHLE</sub>	Propagation Delay	Com	1.5	9	1.5	5.9	1.5	5.0	1.0	4.0	ns
t <sub>PLHE</sub>	$\overline{E}_i$ to $\overline{O}_i$	Mil	1.5	12	1.5	8.0	1.5	7.0	—	—	

**Notes:**

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.