Rochester Electronics

Datasheet

PART NUMBER

D2764A-2-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	Change to Military drawing format. Add new vendor CAGE 61394. Add 2 new device types. Editorial changes throughout. Change drawing CAGE to 67268.	31 Aug. 1987	

CURRENT CAGE CODE 67268

REV	D																								
PAGE	24																								

REV STATUS OF PAGES																									
	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
26 May 1982

AMSC N/A

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MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, 65,536 (8KX8), UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	14933	82005

REV D

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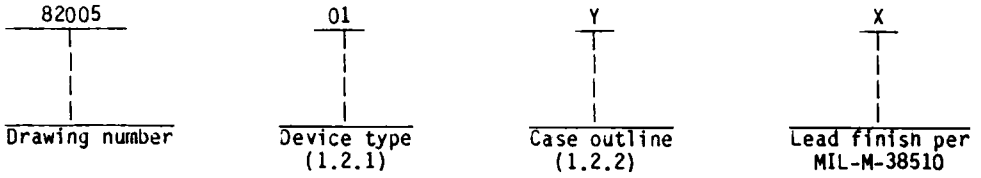
DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access	Program method
01	2764-450	8192 x 8 - Bit UV EPROM	450 ns	A,C
02	2764-250	8192 x 8 - Bit UV EPROM	250 ns	A,C
03	2764A-35	8192 x 8 - Bit UV EPROM	350 ns	B
04	2764A-25	8192 x 8 - Bit UV EPROM	250 ns	B
05	2764A-20	8192 x 8 - Bit UV EPROM	200 ns	B
06	2764-150	8192 x 8 - Bit UV EPROM	150 ns	C
07	2764-200	8192 x 8 - Bit UV EPROM	200 ns	C

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	D-10 (28-pin, 1/2" x 1-3/8"), dual-in-line package 1/
Z	C-12 (32-terminal, .450" x .550"), chip carrier package 1/

1.3 Absolute maximum ratings.

Supply voltage, V_{CC}	-0.3 to 7.0 V 2/
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D	1.0 W
Lead temperature (soldering, 10 seconds)	300°C.
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	
Device types 03 - 05	+150°C
Device types 01, 02, 06, 07	+175°C
All input or output voltages with respect to ground for device types 03 - 05	-0.6 V to 6.25 V
Input voltage range for device types 01, 02, 06, 07	-0.3 V dc to 7.0 V dc
V_{PP} Supply Voltage (methods A and C)	-0.3 V to 22 V
(method B)	-0.6 V to 13 V

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ All voltages referenced to V_{SS}.

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Input low voltage, V_{IL}	-0.1 V to 0.8 V
Input high voltage, V_{IH}	2.0 to V_{CC} +1
Supply voltage, V_{CC}	4.5 V to 5.5 V
High level program input voltage $V_{IN(PR)}$	21.0 V ±.5 V (Program methods A and C)
High level program input voltage $V_{IN(PR)}$	12.5 V ±0.3 V (Program method B)

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \ge 125°C$		Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -400 µA	V_{CC} = 4.5 V	1, 2, 3	01,02 06,07	2.4		V
			V_{CC} = 5.25 V		03-05	2.4		
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	V_{CC} = 5.5 V	1, 2, 3	01,02 06,07		0.4	V
			V_{CC} = 5.25 V		03-05		0.45	
High level output leakage current 2/	I_{OH}	V_{CC} = 5.5 V V_{OUT} = 5.5 V	1/	1, 2, 3	All		10	µA
High level input current 2/	I_{IH}	V_{CC} = 5.25 V V_{IN} = 5.25 V	Outputs deselected	1, 2, 3	All		10	µA
Low level input current 2/	I_{IL}	V_{CC} = 5.25 V V_{IN} = 0.4 V	Output deselected	1, 2, 3	All		-10	µA
V_{PP} supply current read	I_{PP}	V_{PP} = 5.5 V		1, 2, 3	All		5	mA
Supply current (standby)	I_{SB}	Output open $\overline{CE}$ = V_{IH}	V_{CC} = 5.5 V	1, 2, 3	01,02 06,07		60	mA
			V_{CC} = 5.25 V		03-05		40	
Supply current	I_{CC}	Outputs open $\overline{OE}$ = $\overline{CE}$ = V_{IL}	V_{CC} = 5.5 V	1, 2, 3	01,02 06,07		120	mA
			V_{CC} = 5.25 V		03-05		100	
Low level output leakage current	I_{OL}	V_{CC} = 5.5 V V_{OUT} = 0.1 V	1/	1, 2, 3	All		10	µA
High level input leakage current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V		1, 2, 3	01,02 06,07		1	µA
					03,04, 05		10	
Low level input leakage current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.1 V		1, 2, 3	01,02 06,07		1	µA
					03,04, 05		-10	
High level input voltage	V_{IH}	V_{CC} = 4.5 V	3/	1, 2, 3	All	2.0	6.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \ge 125°C$	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Low level input voltage	V_{IL}	V_{CC} = 5.5 V 3/	1, 2, 3	All	-0.1	0.8	V
V_{PP} read voltage	V_{PP}		1, 2, 3	All	V_{CC} -0.7	V_{CC} +1	V
Input capacitance 2/ 4/	C_{IN}	V_{IN} = 0 V, f = 1 MHz T_C = 25°C	4	All		6	pF
Output capacitance 4/	C_O	V_{OUT} = 0 V, f = 1 MHz T_C = 25°C	4	All		12	pF
Address access time	t_{AA}	V_{CC} = 5.25 V 2/ 5/ See figure 5	9, 10, 11	06		150	ns
				05,07		200	
				01		450	
				02,04		250	
				03		350	
Chip enable access time	t_{CE}		9, 10, 11	06		150	ns
				05,07		200	
				01		450	
				02,04		250	
				03		350	
Output enable access time	t_{OE}		9, 10, 11	03	15	130	ns
				01	15	200	
				02,04, 06	10	100	
				05,07	0	150	
$\overline{CE}$ or $\overline{OE}$ to high Z	t_{DF} 6/		9, 10, 11	03	0	115	ns
				01	5	150	
				02	0	90	
				04	0	60	
				05,07	0	150	
				06	0	80	
Output hold from address change	t_{OH} 6/		9, 10, 11	All	0		ns

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OL} and I_{OH} with the output under test connected to V_{OUT}.
2/ Outputs shall be loaded per figure 4.
3/ Tests for all inputs and control pins.
4/ All pins not being tested are to be grounded.
5/ Equivalent ac test conditions (actual load conditions vary by tester):
Output load: 1 TTL gate and C_L = 100 pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.4 V and 2.4 V.
6/ Tested initially and after any design changes.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and 4.6.

3.5.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).
2. Bake, unbiased, for 12 hours at 200°C.
3. Perform a margin test using $V_M = V_{CC} = 6.0$ V at +25°C using loose timing.
4. Erase device, then program 45 percent-50 percent of the bits to a worst case speed pattern.
5. Perform dynamic burn-in (see 4.2a).
6. Perform a margin test using $V_M = V_{CC} = 6.0$ V at +25°C.
7. Perform 100 percent electrical testing at +125°C and -55°C. Perform 100 percent ac and dc electricals at +25°C.
8. Erase device (see 3.5.1), except devices submitted for groups A, B, C, and D.
9. Verify erasure (see 3.5.3).

Margin test method B

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.
2. Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.
3. Perform a margin test using $V_M = +5.9$ V at +25°C using loose timing (i.e., $t_{ACC} = 1$ µs).
4. Perform dynamic burn-in (see 4.2a).
5. Margin at $V_M = +5.9$ V.
6. Perform electrical tests (see 4.2).
7. Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.
8. Verify erasure (see 3.5.3).

Margin test method C

1. Program at 25°C with a greater than 95 percent pattern (ex. diagonal "1's") (see 3.5.2).
2. Unbiased bake for 8 hours at 200°C or 24 hours at 170°C or 72 hours at 150°C.
3. Test at 95°C (see 3.5.3), including a margin test at $V_M = +6$ V and loose timing (i.e. $T_{ACC} = 1$ µs).
4. Erase (see 3.5.1).
5. Program at 25°C with a 50 percent pattern (ex. checkboard bar) (see 3.5.2) (Programmed with checkboard at wafer sort).