DS90LV032AQML 3V LVDS Quad CMOS Differential Line Receiver

Check for Samples: DS90LV032AQML

FEATURES

- **Low chip to chip skew**
- **Low differential skew**
- **High impedance LVDS inputs with power-off**
- **Low power dissipation**
- **Accepts small swing (330 mV) differential signal levels.**
- **Compatible with ANSI/TIA/EIA-644**
- **Operating temperature range (-55°C to +85°C)**
- **Pin compatible with DS90C032A and DS26C32A.**
- **Typical Rise/Fall time is 350pS.**

DESCRIPTION

The DS90LV032A is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates.

The DS90LV032A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs.

The DS90LV032A and companion LVDS line driver (eg. DS90LV031A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

In addition, the DS90LV032A provides power-off high impedance LVDS inputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present.

Connection Diagram
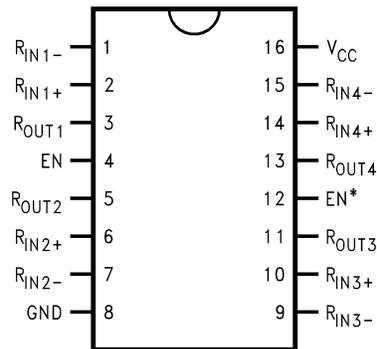
Figure 1. NAD0016A and NAC0016A Packages

Functional Diagram
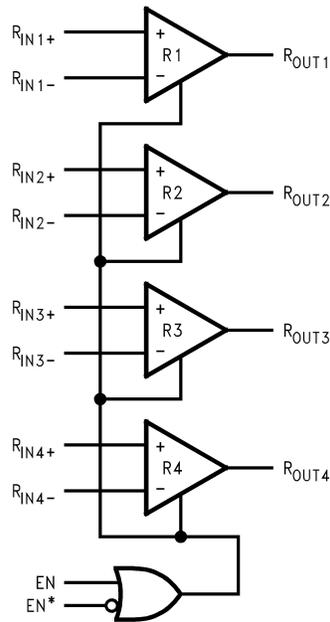
Figure 2.

Truth Table

ENABLES		INPUTS	OUTPUT
En	**En***	$R_{I+} − R_{I−}$	R_O
L	H	X	Z
All other combinations of enable inputs		$V_{ID} ≥ 0.1V$	H
		$V_{ID} ≤ −0.1V$	L
		Full Fail-safe Open/Short or Terminated	H

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Product Folder Links: *DS90LV032AQML*

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (R_I+, R_I-)	−0.3V to +3.9V
Enable Input Voltage (En, En*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_O)	−0.3V to (V_{CC} + 0.3V)
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature Range (Soldering 4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C [2]	
NAD0016A Package	845 mW
NAC0016A Package	845 mW
Thermal Resistance	
θ_{JA}	
NAD0016A Package	148°C/W
NAC0016A Package	148°C/W
θ_{JC}	
NAD0016A Package	21°C/W
NAC0016A Package	21°C/W
Maximum Junction Temperature	+150°C
ESD Rating [3]	4.5 KV

(1)   "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2)   Derate @ 6.8mW/°C
(3)   Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	+3.15	+3.45	V
Receiver Input Voltage	Gnd	+3.0	V
Operating Free Air Temperature (T_A)	−55	+85	°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS90LV032A Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.
Over supply voltage range of 3.15V to 3.45V and operating temperature of −55°C to +85°C.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{TL}	Differential Input Low Threshold	V_{CM} = +1.2V	(1)	-100		mV	1, 2, 3
V_{Th}	Differential Input High Threshold	V_{CM} = +1.2V	(1)		100	mV	1, 2, 3
VCMR	Common Mode Voltage Range	V_{ID} = 200mV peak to peak	(1), (2)	0.1	2.3	V	1, 2, 3
I_I	Input Current	V_{CC} = 3.45V or 0V, V_I = 2.8V or 0V			±10	μA	1, 2, 3
		V_{CC} = 0V, V_I = 3.45V			±20	μA	1, 2, 3
V_{OH}	Output High Voltage	I_{OH} = -0.4 mA, V_{ID} = 200mV		2.7		V	1, 2, 3
		I_{OH} = -0.4 mA, Inputs Open		2.7		V	1, 2, 3
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = -200mV			0.25	V	1, 2, 3
I_{OS}	Output Short Circuit Current	Enabled, V_O = 0V	(3)	-15	-120	mA	1, 2, 3
I_{OZ}	Output TRI-STATE Current	Disabled, V_O = 0V or V_{CC}			±10	μA	1, 2, 3
V_{IH}	Input High Voltage		(4)	2.0	V_{CC}	V	1, 2, 3
V_{IL}	Input Low Voltage		(4)	Gnd	0.8	V	1, 2, 3
I_L	Input Current	V_I = V_{CC} or 0V, Other Input = V_{CC} or Gnd			±10	μA	1, 2, 3
V_{CI}	Input Clamp Voltage	I_{CI} = -18mA			-1.5	V	1, 2, 3
I_{CC}	No Load Supply Current Receivers Enabled	En, En* = V_{CC} or Gnd, Inputs Open			15	mA	1, 2, 3
		En, En* = 2.4 or 0.5, Inputs Open			15	mA	1, 2, 3
I_{CCZ}	No Load Supply Current Receivers Disabled	En = Gnd, En* = V_{CC} , Inputs Open			5.0	mA	1, 2, 3

(1) Tested during V_{OH}/V_{OL} tests by applying appropriate voltage levels to the input pins of the device under test.
(2) The VCMR range is reduced for larger V_{ID}. Example: if V_{ID} = 400mV, the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is valid over a common-mode range of 0V to 2.3V. A V_{ID} up to V_{CC} − 0V may be applied to the R_{IN+}/ R_{I-} inputs with the Common-Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when V_{ID} is increased from 200mV to 400mV. Skew specifications apply for 200mV ≤ V_{ID} ≤ 800mV over the common-mode range .
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature.
(4) Tested during I_{OZ} tests by applying appropriate threshold voltage levels to the En and En* pins.

DS90LV032A Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = 3.15 / 3.3 / 3.45V, C_L = 20pF

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHLD}	Differential Propagation Delay High to Low	V_{ID} = 200mV, Input pulse = 1.1V to 1.3V, V_I = 1.2V (0V differential) to V_O = 1/2 V_{CC}	Figure 3 and Figure 4	0.5	3.5	ns	9, 10, 11
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200mV, Input pulse = 1.1V to 1.3V, V_I = 1.2V (0V differential) to V_O = 1/2 V_{CC}	Figure 3 and Figure 4	0.5	3.5	ns	9, 10, 11
t_{SkD}	Differential Skew |t_{PHLD} - t_{PLHD}|	C_L = 20pF, V_{ID} = 200mV	Figure 3 and Figure 4		1.5	ns	9, 10, 11
t_{Sk1}	Channel to Channel Skew	C_L = 20pF, V_{ID} = 200mV	(1)		1.75	ns	9, 10, 11
t_{Sk2}	Chip to Chip Skew	C_L = 20pF, V_{ID} = 200mV	(2)		3.0	ns	9, 10, 11
t_{PLZ}	Disable Time Low to Z	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = V_{OL}+0.5V, R_L= 1kΩ.	Figure 5 and Figure 6		12	ns	9, 10, 11
t_{PHZ}	Disable Time High to Z	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = V_{OH}-0.5V, R_L = 1kΩ.	Figure 5 and Figure 6		12	ns	9, 10, 11
t_{PZH}	Enable Time Z to High	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = 50%, R_L = 1kΩ.	Figure 5 and Figure 6		20	ns	9, 10, 11
t_{PZL}	Enable Time Z to Low	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = 50%, R_L = 1kΩ.	Figure 5 and Figure 6		20	ns	9, 10, 11

(1)   Channel-to-Channel Skew, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

(2)   Chip to chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

PARAMETER MEASUREMENT INFORMATION
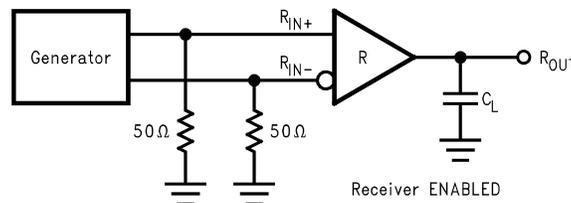
Figure 3. Receiver Propagation Delay and Transition Time Test Circuit
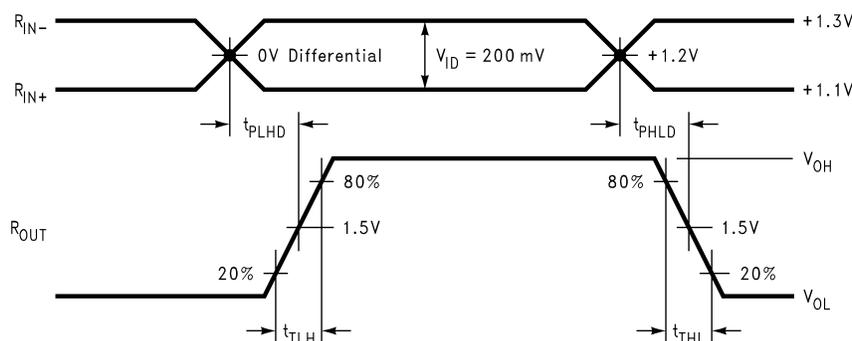
Figure 4. Receiver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)
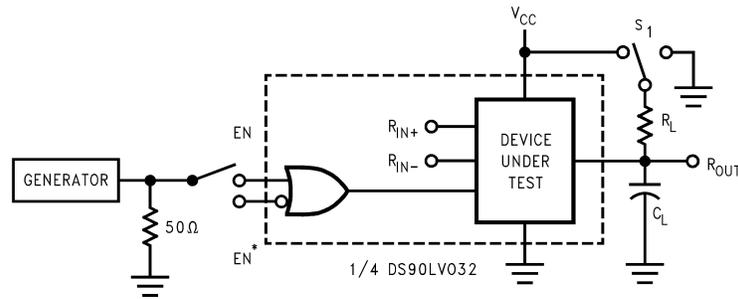
C_L includes load and test jig capacitance.
$S_1 = V_{CC}$ for t_{PZL}, and t_{PLZ} measurements.
$S_1 = $ Gnd for t_{PZH} and t_{PHZ} measurements.

Figure 5. Receiver TRI-STATE Delay Test Circuit
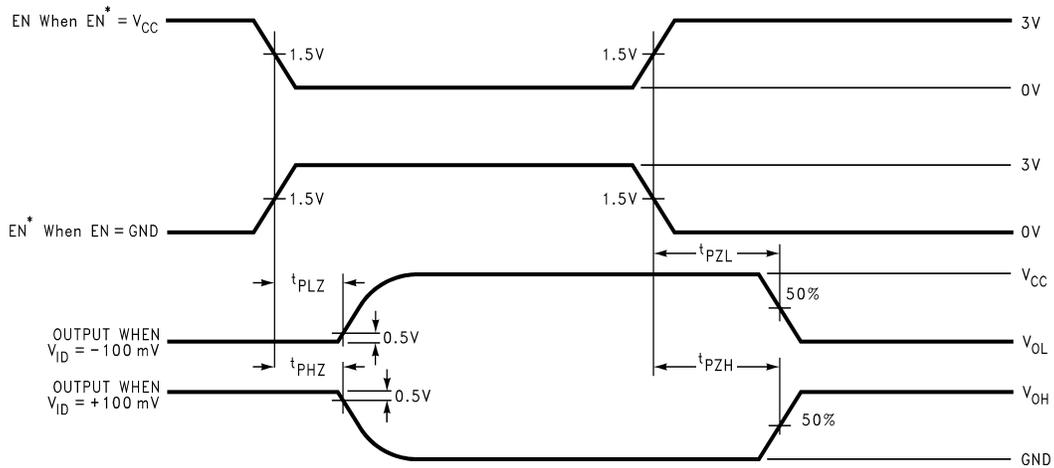
Figure 6. Receiver TRI-STATE Delay Waveforms

Product Folder Links: *DS90LV032AQML*

Typical Performance Characteristics
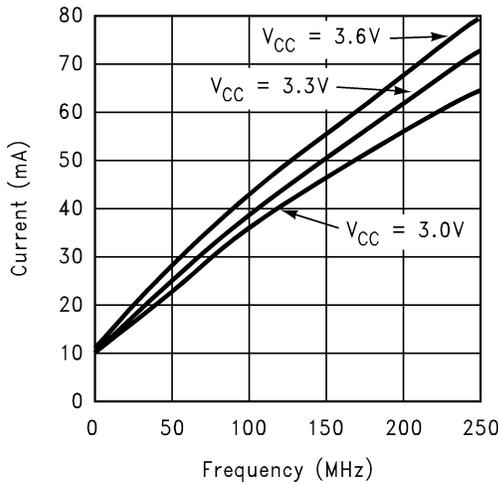
Figure 7. I_{CC} vs Frequency, four channels switching
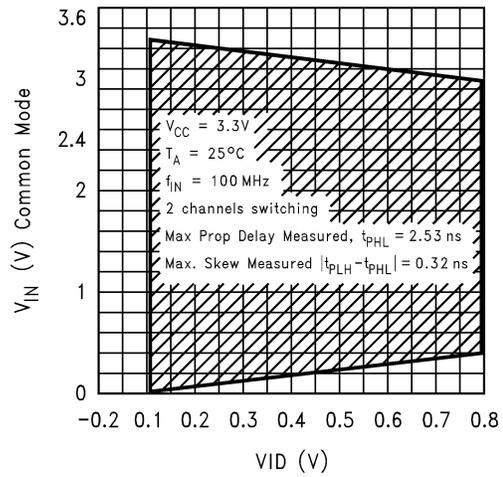
Figure 8. Typical Common-Mode Range variation with respect to amplitude of differential input
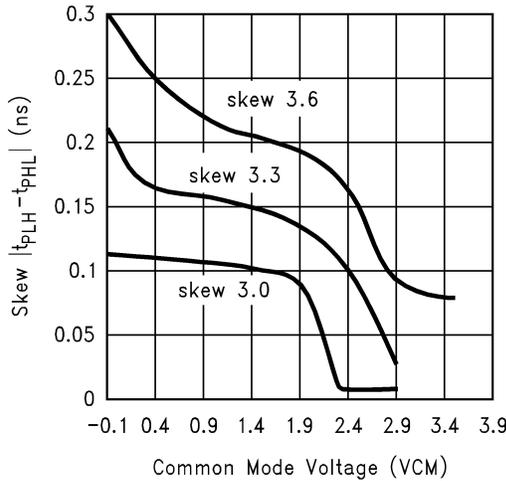
Figure 9. Typical Pulse Skew variation versus common-mode voltage
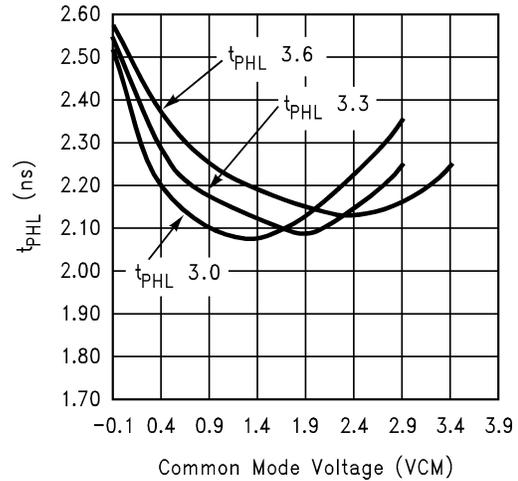
Figure 10. Variation in High to Low Propagation Delay versus V_{CM}
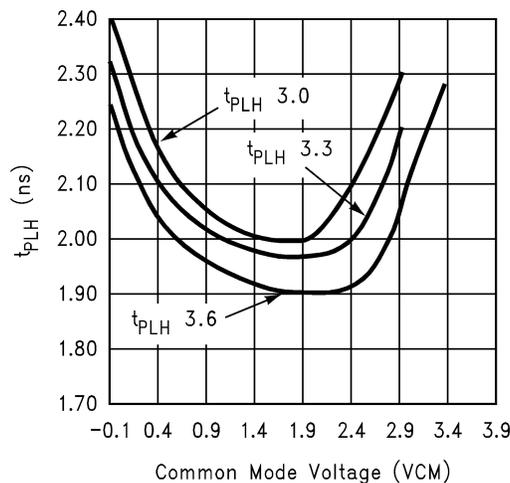
Figure 11. Variation in Low to High Propagation Delay versus V_{CM}

Product Folder Links: DS90LV032AQML

TYPICAL APPLICATION

Balanced System
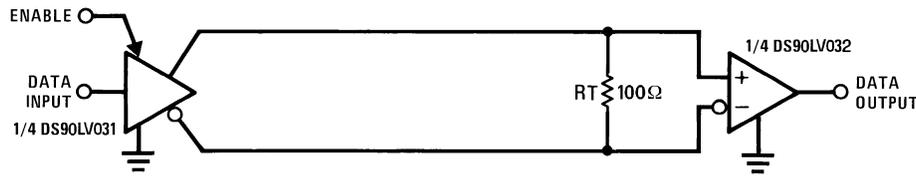
Figure 12. Point-to-Point Application

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the LVDS Owner's Manual at http://www.ti.com/ww/en/analog/interface/lvds.shtml

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 12. This configuration provides a clean signaling environment for the fast edge rates of the drivers . The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV032A differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins have a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1μF in parallel with 0.01μF, in parallel with 0.001μF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes A 10μF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC BOARD CONSIDERATIONS

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Product Folder Links: *DS90LV032AQML*

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a resistor which best matches the differential impedance of your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <10mm (12mm MAX)

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

FAIL-SAFE FEATURE

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV032A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.

2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.

3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

The footprint of the DS90LV032A is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

PIN DESCRIPTIONS

Pin No.	Name	Description
2, 6, 10, 14	R_{I+}	Non-inverting receiver input pin
1, 7, 9, 15	R_{I-}	Inverting receiver input pin
3, 5, 11, 13	R_O	Receiver output pin
4	En	Active high enable pin, OR-ed with En*
12	En*	Active low enable pin, OR-ed with En
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	Gnd	Ground pin

Product Folder Links: *DS90LV032AQML*

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9865201QFA	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 85	(DS90LV031AW ~ DS90LV032AW) -QML Q (5962-98651 ~ 5962-98652) 01QFA ACO 01QFA >T	Samples
DS90LV032AW-MLS	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 85	DS90LV032AW-MLS ACO MLS >T	Samples
DS90LV032AW-QML	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 85	(DS90LV031AW ~ DS90LV032AW) -QML Q (5962-98651 ~ 5962-98652) 01QFA ACO 01QFA >T	Samples
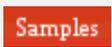
(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DS90LV032AQML, DS90LV032AQML-SP :

● Military: DS90LV032AQML

● Space: DS90LV032AQML-SP

NOTE: Qualified Version Definitions:

   ● Military - QML certified for Military and Defense Applications

   ● Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

NAD0016A

.074 +.006 −.024

.045 .026

.39 MAX

.000 MIN TYP

16   9

8X .32±.01

.3 MAX GLASS

.250 +.025 −.005

PIN #1 ID NOTE 3

8X .32±.01

1   8

.006±.002 TYP NOTE 2

.010±.002

16X .017±.002 NOTE 2

14X .050±.005

DIMENSIONS ARE IN INCHES

W16A (Rev T)

IMPORTANT NOTICE