QUALITY SEMICONDUCTOR, INC.

# High-Performance CMOS Two-by-Two Analog Cross Point Switch

QS4A201Q

## FEATURES

- Low On-resistance: $r_{DS(on)} = 5\Omega$
- Fast transition time: $t_{TRAN} = 6ns$
- Wide bandwidth: 1.3GHz (–3dB point)
- Crosstalk:
  –90dB @ 50KHz, –40dB @ 5MHz,
  –30dB @ 30MHz
- Off-isolation:
  –70dB @ 50KHz, –40dB @ 5MHz,
  –30dB @ 30MHz,
- Single 5V supply
- Can be used as a multiplexer or demultiplexer
- TTL compatible control inputs
- Ultra-low quiescent current: 3μA
- Switch turn on time of 6.5ns

## APPLICATIONS

- High-speed video signal switching/routing
- HDTV-quality video signal routing
- Phase reversal
- Data acquisition
- ATE systems
- Telecomm routing
- Token Ring transceivers
- High-speed networking

## GENERAL DESCRIPTION

The QS4A201Q is a high-performance CMOS. This device provides 2 sets of five high-speed CMOS switches providing "cross point" connection between inputs and outputs. The low on-resistance of the QS4A201Q allows inputs to be connected to outputs with low insertion loss and high bandwidth. TTL-compatible control circuitry with “Break-Before-Make” feature prevents contention.

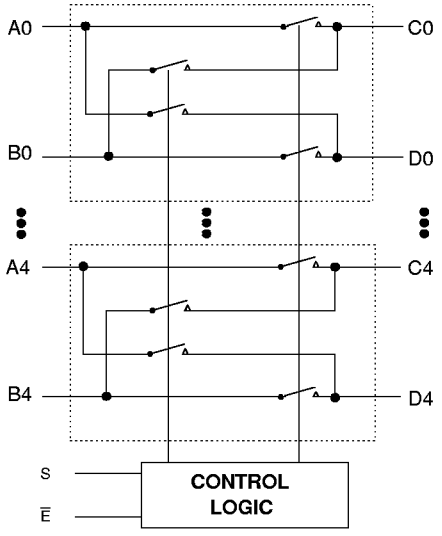
The QS4A201Q with 1.3 GHz bandwidth makes it ideal for high-performance video signal switching, audio signal switching, and telecomm routing applications. High performance and low power dissipation makes this device ideal for battery operated and remote instrumentation applications.

The QS4A201Q is offered in the QSOP package and has several advantages over conventional packages such as PDIP and SOIC including:

- Reduced signal delays due to denser component packaging on circuit boards
- Reduced system noise due to less pin inductance



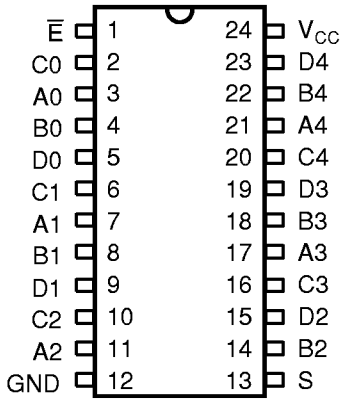
## Figure 1. Functional Block Diagram



## Figure 2. Pin Configuration

(All Pins Top View)

QSOP




## Table 1. Definitions

| Name | I/O | Function |
|---|---|---|
| $A_N$, $B_N$ | I/O | Ports A, B |
| $C_N$, $D_N$ | I/O | Ports C, D |
| $\overline{E}$ | I | Bus Switch Enable |
| S | I | Bus Exchange |

## Table 2. Function Table

| $\overline{E}$ | S | $A_N$ | $B_N$ | Function |
|---|---|---|---|---|
| H | X | Hi-Z | Hi-Z | Disable |
| L | L | $C_N$ | $D_N$ | Enable |
| L | H | $D_N$ | $C_N$ | Exchange |



## Table 3. Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage to Ground | –0.5V to +7.0V |
| DC Switch Voltage $V_S$ | –0.5V to +7.0V |
| Analog Input Voltage | –0.5V to +7.0V |
| DC Input Voltage $V_{IN}$ | –0.5V to +7.0V |
| AC Input Voltage (for a pulse width ≤ 20ns) | –3.0V |
| DC Output Current Max. Sink Current/Pin | 120mA |
| Maximum Power Dissipation | 0.7 watts |
| $T_{STG}$ Storage Temperature | –65° to +150°C |

**Note:** ABSOLUTE MAXIMUM RATINGS are those conditions beyond which damage to the device may occur. Exposure to these conditions or beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rating conditions is not implied.

## Table 4. Power Supply Characteristics

| Symbol | Parameter | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | 3 | µA |

## Table 5. Electrical Characteristics Over Operating Range

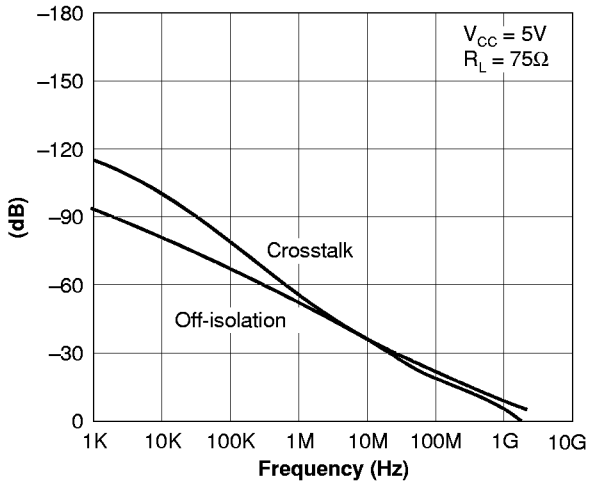
Commercial: $T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ± 5%

| Symbol | Parameter | Test Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| ***Analog Switch*** | | | | | | |
| $V_{IN}$ | Analog Signal Range(2) | | –0.5 | 1.0 | $V_{CC}$–1 | V |
| $r_{DS(on)}$ | Drain-source On-resistance(2,3) | $V_{CC}$ = Min., $V_{IN}$ = 0.0V, $I_{ON}$ = 30mA | — | 5 | 7 | Ω |
| | | $V_{CC}$ = Min., $V_{IN}$ = 1.5V, $I_{ON}$ = 15mA | — | 5.5 | 8 | Ω |
| $\Delta r_{DS(on)}$ | $r_{DS(on)}$ Matching Between Channels(2,3,4) | $V_{CC}$ = Min., $V_{IN}$ = 0.0V, $I_{ON}$ = 30mA | — | 1 | — | Ω |
| | | $V_{CC}$ = Min., $V_{IN}$ = 1.5V, $I_{ON}$ = 15mA | — | 1 | — | Ω |
| $I_{C(OFF)}$ | Channel Off Leakage Current | $A_N$, $B_N$ = $V_{CC}$ or 0V, $C_N$, $D_N$ = 0V or $V_{CC}$, $\overline{E}$ = $V_{CC}$ | — | 1 | — | nA |
| $I_{C(ON)}$ | Channel On Leakage Current | $A_N$ = $B_N$ = $C_N$ = $D_N$ = 0V, Each Channel is Turned On Sequentially | — | 1 | — | nA |
| ***Digital Control*** | | | | | | |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH for Control Pins | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW for Control Pins | — | — | 0.8 | V |
| ***Dynamic Characteristics*** | | | | | | |
| $t_{TRANS}$ | Exchange Switching Time S to $C_N$, $D_N$ | $R_L$ = 1KΩ, $C_L$ = 100pF (See Figure 9) | 0.5 | — | 6.6 | ns |
| $t_{ON(\overline{E})}$ | Enable Turn-on Time $\overline{E}$ to $C_N$, $D_N$ | $R_L$ = 1KΩ, $C_L$ = 100pF (See Figure 10) | 0.5 | — | 6.5 | ns |
| $t_{OFF(\overline{E})}$ | Enable Turn-off Time $\overline{E}$ to $C_N$, $D_N$ | $R_L$ = 1KΩ, $C_L$ = 100pF (See Figure 10) | 0.5 | — | 6.0 | ns |
| $t_{PD}$ | Group Delay(2,5) | $R_L$ = 1KΩ, CL = 100pF | — | — | 250 | ps |
| $f_{3dB}$ | –3dB Bandwidth | $V_{IN}$ = 0 to 1V, 1Vp–p, $R_L$ = 75Ω | — | 1.3 | — | GHz |
| | Off-isolation | $V_{IN}$ = 0 to 1V, 1Vp–p, $R_L$ = 75Ω, f = 5MHz | — | –40 | — | dB |
| $X_{TALK}$ | Crosstalk | $V_{IN}$ = 0 to 1V, 1Vp–p, $R_L$ = 75Ω, f = 5MHz | — | –40 | — | dB |
| $C_{(OFF)}$ | Switch Off Capacitance | $\overline{E}$ = $V_{CC}$, $V_{IN}$ = $V_{OUT}$ = 0V | — | 5 | — | pF |
| $C_{(ON))}$ | Switch On Capacitance | $\overline{E}$ = 0V, $V_{IN}$ = $V_{OUT}$ = 0V | — | 10 | — | pF |
| $Q_{CI}$ | Charge Injection | | — | 1.5 | — | pC |

**Notes**:
1. Typical values indicate $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Guaranteed by design, not subject to production test.
3. Measured by voltage drop between A and C pins or B and D pins at indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A,B or C,D) pins.
4. $\Delta r_{DS(on)}$ compares On-resistance at the specified $V_{IN}$ Values.
5. The bus switch contributes no group delay other than the RC delay of the on-resistance of the switch and load capacitance. Group delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

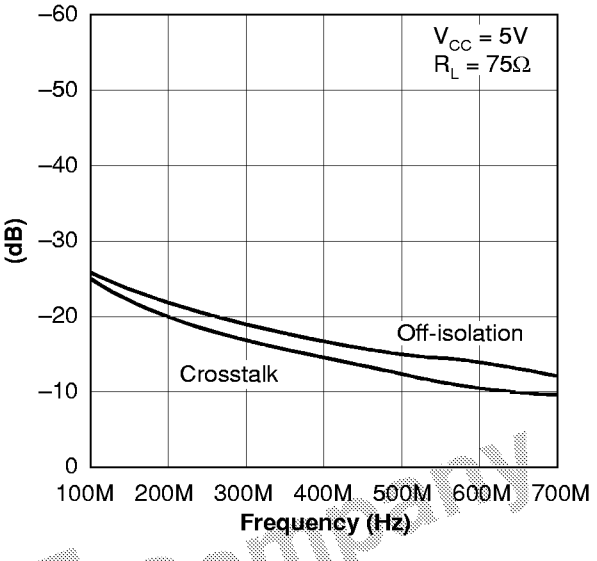
## TYPICAL CHARACTERISTICS

### Figure 3. Off-isolation and Crosstalk vs. Frequency




**Note:** 1. Crosstalk = 20 log | $V_O/V_S$|
2. Off-isolation = 20 log | $V_O/V_S$|

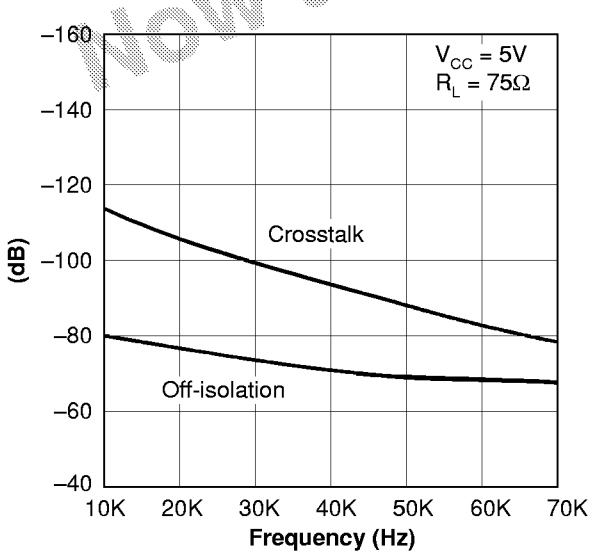
### Figure 4. Off-isolation and Crosstalk vs. Frequency




**Note:** 1. Crosstalk = 20 log | $V_O/V_S$|
2. Off-isolation = 20 log | $V_O/V_S$|

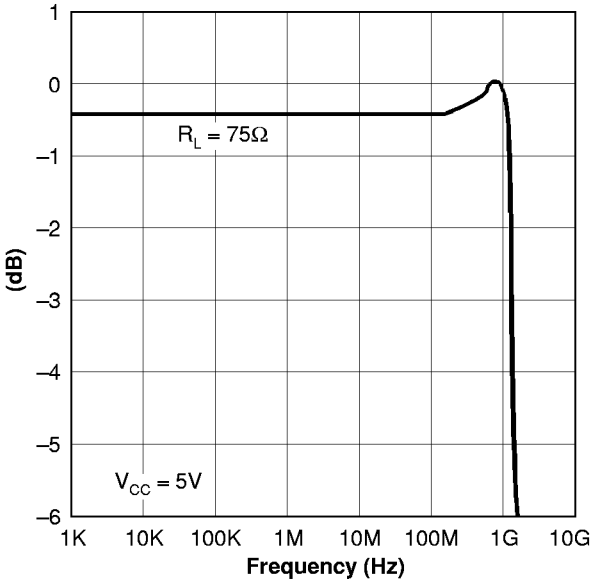


### Figure 5. Off-isolation and Crosstalk vs. Frequency




**Note:** 1. Crosstalk = 20 log | $V_O/V_S$|
2. Off-isolation = 20 log | $V_O/V_S$|

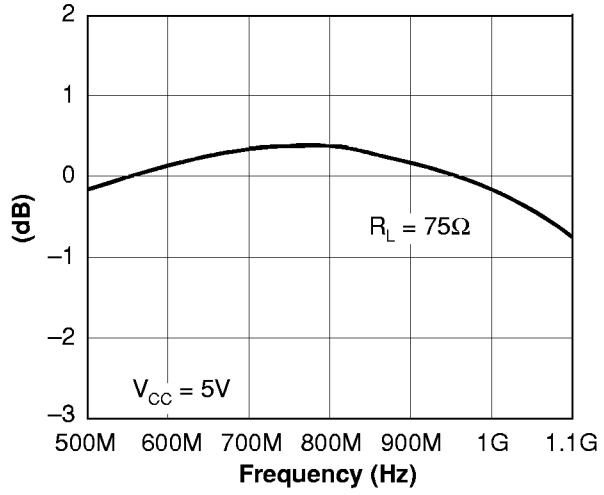
### Figure 6. Insertion Loss vs. Frequency




**Note:** 1. Insertion Loss = 20 log | $V_O/V_S$|

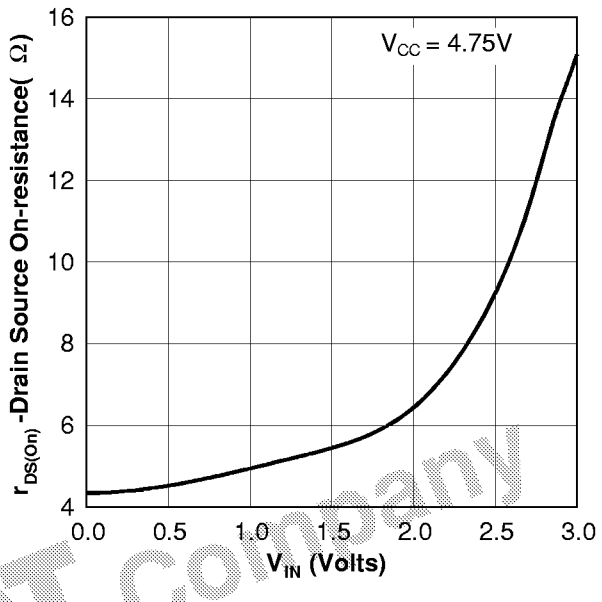
## TYPICAL CHARACTERISTICS (continued)

### Figure 7. Insertion Loss vs. Frequency



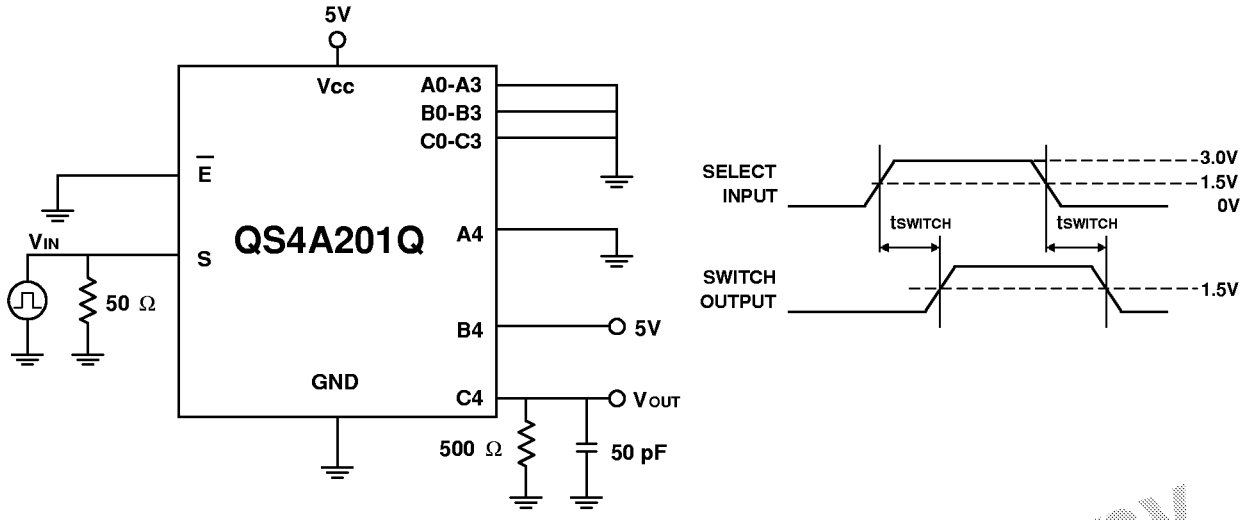

**Note:** 1. Insertion Loss = 20 log |VO/VS|

### Figure 8. ON-Resistance vs. $V_{IN}$



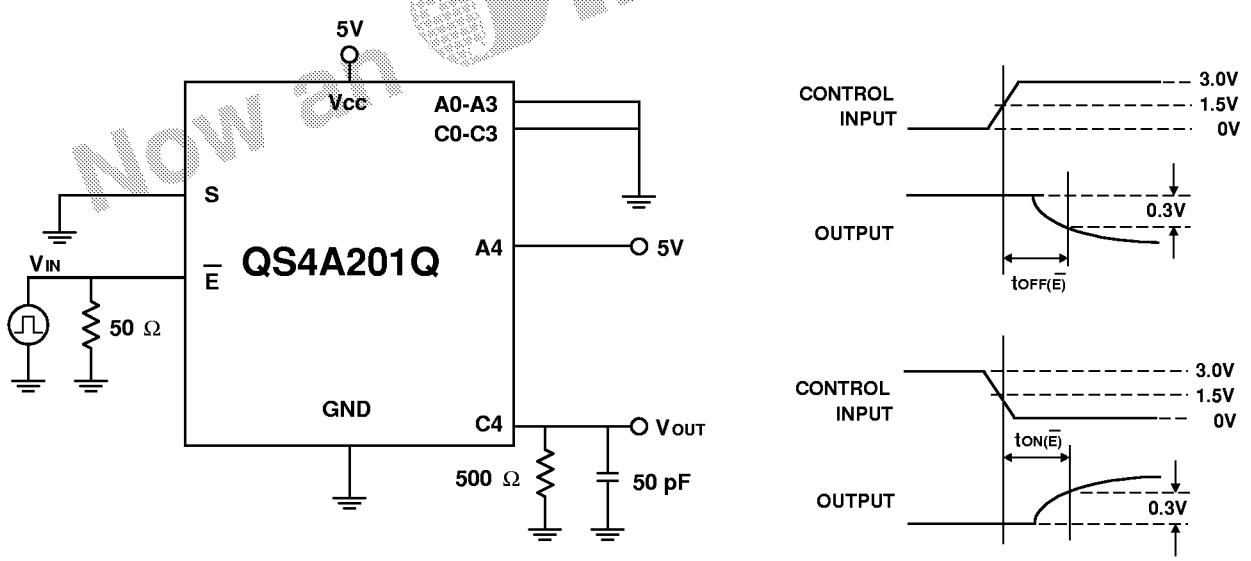
## TEST CIRCUITS

### Figure 9. Transition Time



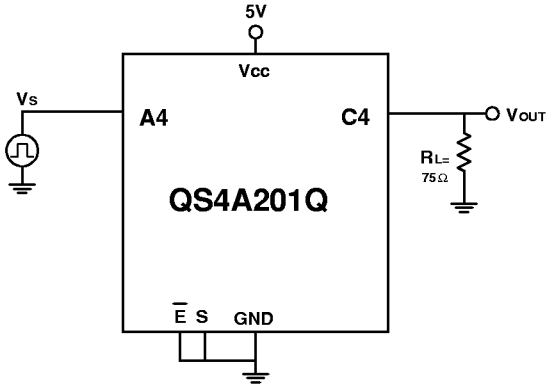



### Figure 10. Switching Time



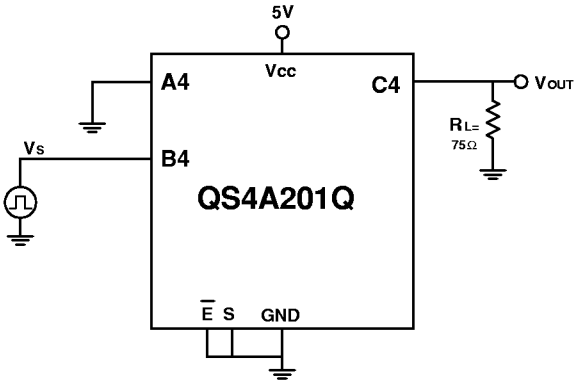
## TEST CIRCUITS (continued)

### Figure 10. Insertion Loss




**Note:** 1. Insertion Loss = 20 log | $V_O/V_S$ |
2. All unused pins are grounded.

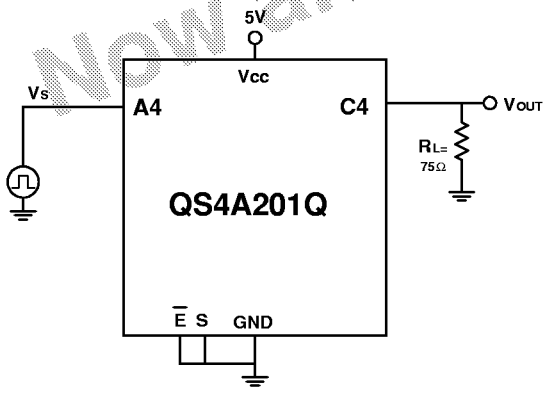
### Figure 11. Crosstalk




**Note:** 1. Crosstalk = 20 log | $V_O/V_S$ |
2. All unused pins are grounded.



### Figure 12. OFF-Isolation




**Note:** 1. Off-isolation = 20 log | $V_O/V_S$ |
2. All unused pins are grounded.