SPWS042B – DECEMBER 1997 – REVISED JUNE 1998

- **Single-Chip With Eight Physical-Layer (PHY) Interfaces for Internetworking Applications**
- **Each PHY Is Full-Duplex Capable for Simultaneous Transmit and Receive**
- **Compliant With IEEE Std 802.3 10BASE-T Specification**
- **Integrated Filters on Both Receive and Transmit Circuits**
  - **No External Filters Are Required**
  - **Meets IEEE Std 802.3 (Section 14.3) Electrical Requirements**
- **Implements IEEE Std 802.3 Autonegotiation to Establish the Highest Common Protocol**
- **Electrostatic Discharge (ESD) Human Body Model (HBM) Protection 1.5 kV Per JEDEC JESD22-A114A**
- **Digital Signal Processor (DSP)-Based Digital Phase-Locked Loop (PLL)**
- **Loopback Mode for Test Operations**
- **Integrated Manchester Encoding/Decoding**
- **Receive-Clock Regeneration for All Input Channels Using Digital PLL**
- **FIFOs Accommodate 8x IEEE Limit on Per-Channel-Pair Frequency Mismatch Across All Eight Channels (IEEE Std 802.3, Sec 7.3.2)**
- **Intelligent Squelch With Selectable Threshold**
- **Link-Pulse Detection and Autonegotiation**
- **Intelligent Rejection of MLT-3 Encoded Data**
- **Transmit Pulse Shaping Reduces Electromagnetic Interference (EMI)**
- **Clock Synchronization Between Channels**
- **Collision Detection**
- **Built-In Jabber Detection**
- **Automatic Reversed-Polarity Detection and Correction**
- **Sufficient Current Drive to Directly Connect LED Status Indicators**
- **CMOS Technology Enables Low Power Consumption**
- **3.3-V Operation**
- **IEEE Std 1149.1 (JTAG)† Test-Access Port (TAP)**
- **Direct Drive to Network Coupling Magnetics**
- **Packaged in 120-Pin Plastic Quad Flatpack (PQFP)**

description

The TNETE2008 OctalPHY is a physical-layer (PHY) interface device for up to eight 10BASE-T networks using a multiplexed medium access controller (MAC) interface compatible with TNETX3110, TNETX3151, TNETX3190, or TNETX3270 switch devices, or equivalent. A digital-signal-processor (DSP)-based phase-locked loop (PLL) is used on each channel to recover data. Integrated wave shaping of the output eliminates the need for filters to meet electromagnetic interference (EMI) testing. DSP-based wave-shaping techniques used internally reduce the required number of external components to a coupling transformer, four resistors, and a capacitor per channel. The multiplexed host interface reduces the number of terminals required to connect eight networks to eight MAC engines, allowing the use of a single package.

The TNETE2008 operation is fully automatic. It can be taken from reset to full operation without parameter downloads or interaction with a host central processing unit (CPU). Some mode terminals affect all of the ports, such as looping back transmit data to the receive path, powering down the PHY, and setting the receiver threshold. There are no management interfaces or internal registers on this device. A directly driven LED matrix provides Ethernet™ status indicators, i.e., link, activity, collision, and duplex. The TNETE2008 produces and receives IEEE Std 802.3-compliant waveforms when coupled to the network with a suitable transformer. The TNETE2008 also incorporates a JTAG-compliant test port.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Std 1149.1-1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture

Ethernet is a trademark of Xerox Corporation.

description (continued)

The TNETE2008 provides PHY interface functions for up to eight 10BASE-T network ports as shown in Figure 1.

A typical application with external components is shown in Figure 2.

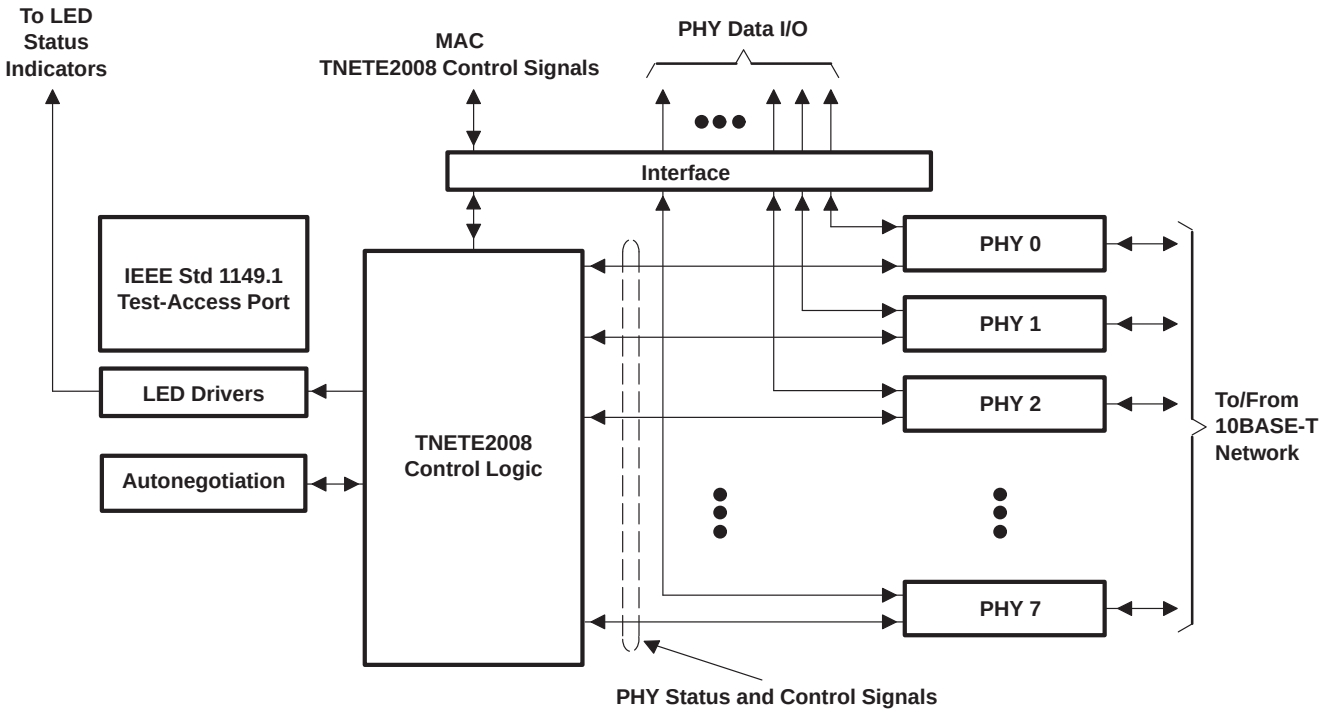


Figure 1. OctalPHY Architecture

1.

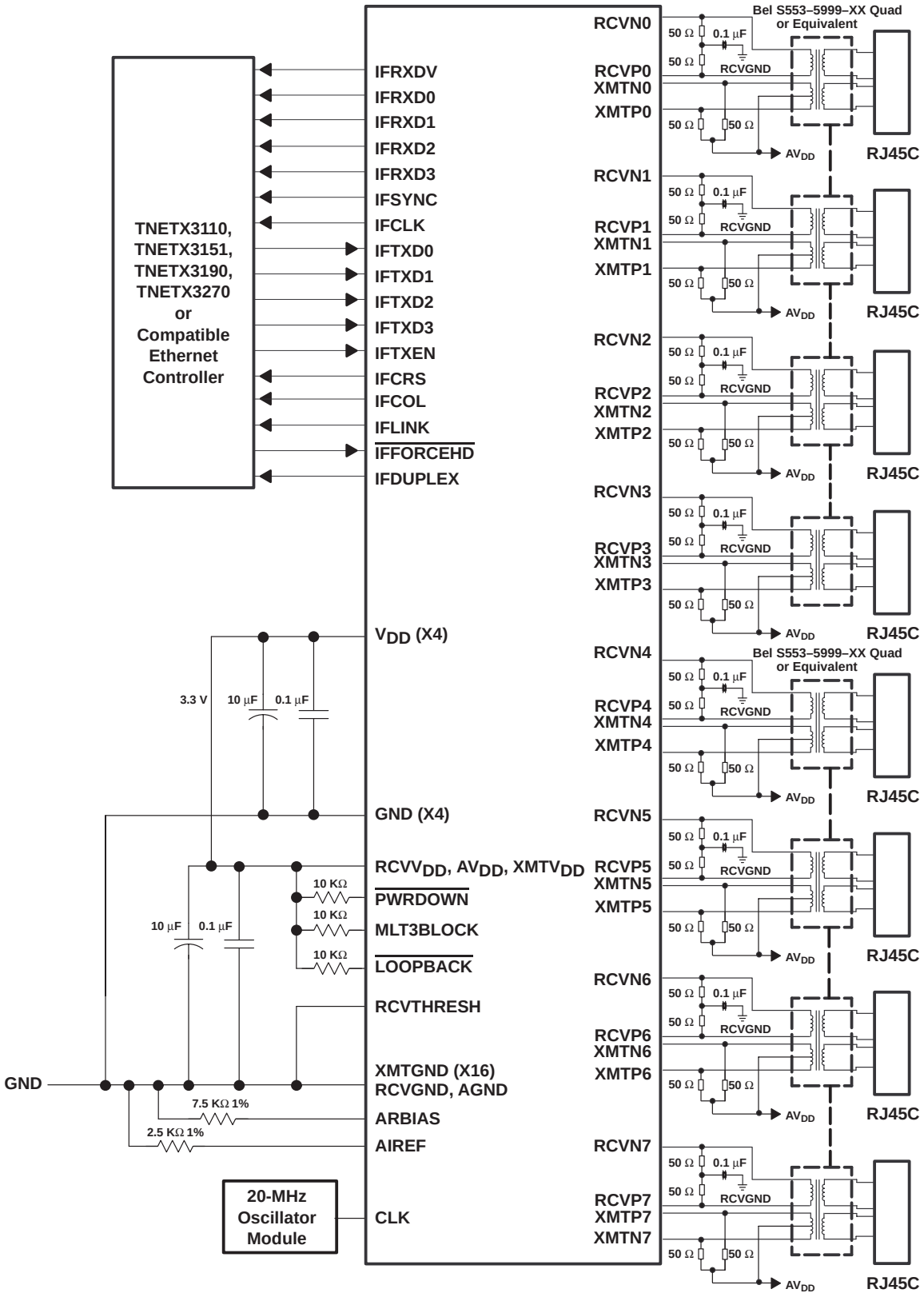
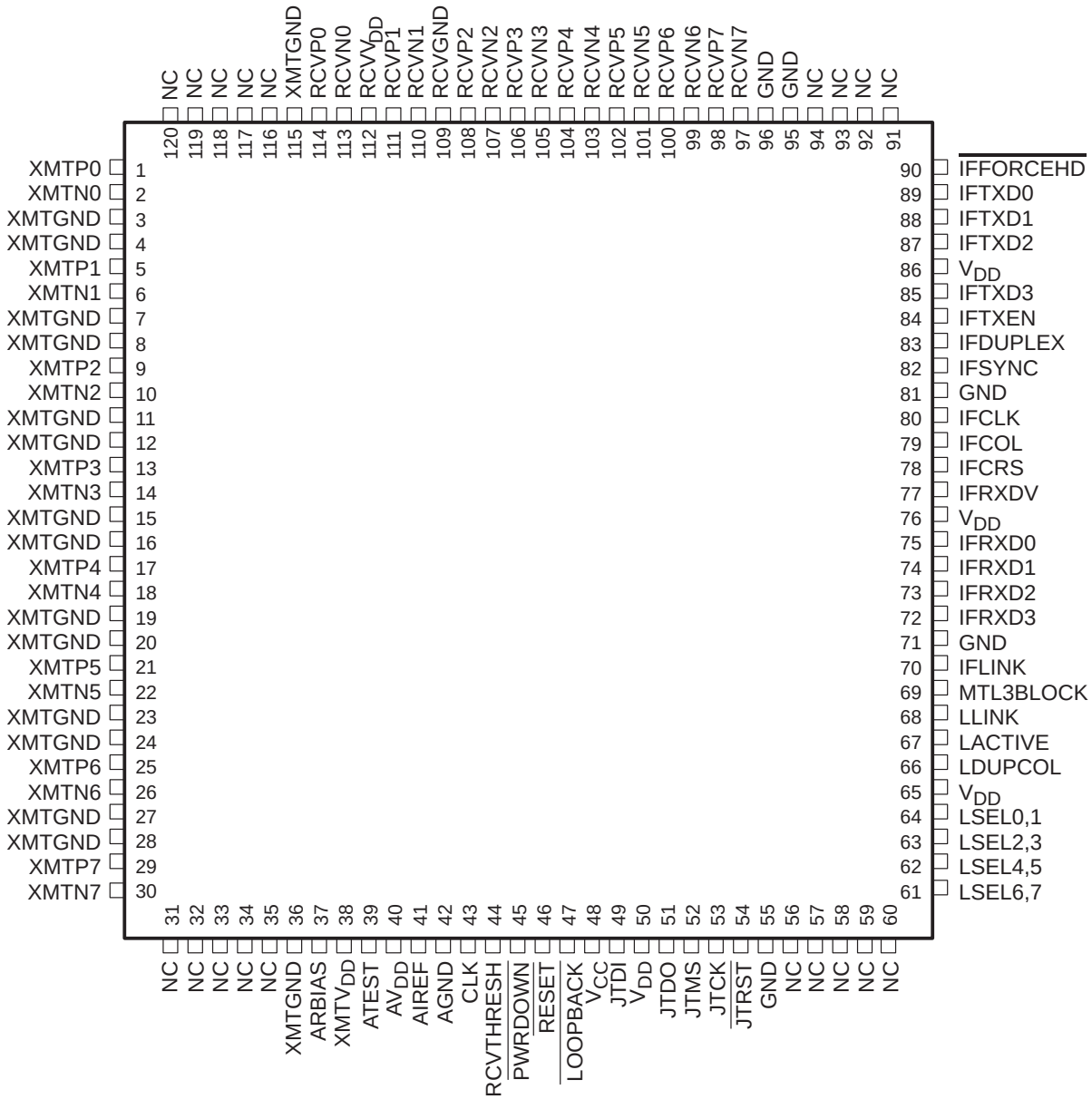


Figure 2. External Components

terminal assignments

TNETE2008 signal terminals are identified according to the section of the device. All 3.3-V power is labeled V_{DD} and GND for ground. V_{CC} power on terminal 48, JTAG power, is subject to JTAG system requirements. Each terminal has prefix letters indicating the circuit of the device it supplies. RCV is receiver circuits, XMT is transmitter circuits, A is analog circuits, J is JTAG circuits, and IF is interface circuits; NC terminals are not connected to anything inside the device.

PBE PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

controller interface – this block of signals is defined for each channel during its time slot (see Figure 6)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
IFCLK	80	O	Interface clock. All ports handled by the interface use the same clock. The clock frequency is 20 MHz.
IFCOL	79	O	Collision. When asserted, IFCOL indicates a network collision on the current port.
IFCRS	78	O	Carrier sense. IFCRS indicates a frame carrier signal is being received on the current port. It asserts for transmissions in half-duplex mode.
IFDUPLEX	83	O	Duplex mode. If IFDUPLEX is low, then the current port is in half duplex, otherwise it is full duplex. If the $\overline{\text{IFFORCEHD}}$ signal is low, then IFDUPLEX also is low.
$\overline{\text{IFFORCEHD}}$	90	I	Force half duplex. This terminal has two functions: The first function concerns the values advertised during autonegotiation of link. If $\overline{\text{IFFORCEHD}}$ is low when a channel latches in the control information about which modes it can advertise during autonegotiation (see Figure 9), this channel is forced to half duplex. Values delivered on IFTXD0–IFTXD3 are overridden. If this terminal is high at latch time, the modes are set by the values passed on IFTXD0–IFTXD3 during the period before commencement of fast link pulse (FLP) exchange for this channel. The second function is the ability of the terminal to drive link invalid for this channel during its time slot and restart link validation. Link is driven invalid and reestablishing link starts when $\overline{\text{IFFORCEHD}}$ transitions from one to zero or from zero to one; that is, any edge on $\overline{\text{IFFORCEHD}}$ drives link invalid and starts the process of reestablishing link. Multiple edges in this signal before link is established force multiple restarts of the linking process shown in Figure 9.
IFLINK	70	O	Interface link. IFLINK indicates the presence of port connection on the current port. Low is no link and high is link made.
IFRXD3†	72	O	Receive data. Receive data bits 3–0 from current port when IFRXDV is asserted. Receive data is clocked out on falling edge of IFCLK.
IFRXD2	73		
IFRXD1	74		
IFRXD0	75		
IFSYNC	82	O	Interface sync. When IFSYNC is 1, the current port for MAC to TNETE2008 transfers is port 0. This signal has a period of 400 ns and a duty cycle of 1:8. The port number for TNETE2008 → MAC data is always two slots ahead and is port 2 when IFSYNC is high. IFSYNC is sampled by the MAC on the falling edge of IFCLK.
IFTXD3†	85	I	Transmit data bit. Transmit data bits 3–0 for the current port when IFTXEN is asserted. Data should change on the rising edge of IFCLK to be clocked into the TNETE2008 on the following rising edge of IFCLK.
IFTXD2	87		
IFTXD1	88		
IFTXD0	89		
IFTXEN	84	I	Transmit enable. IFTXEN indicates that valid transmit data is on IFTXD0–IFTXD3.
IFRXDV	77	O	Receive data valid. This signal indicates the IFXRD0–IFXRD3 contain valid data.

† Most significant bit

Terminal Functions (Continued)

JTAG interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
JTCK	53	I	Test clock. JTCK is used to clock state information and test data into and out of the device during operation of the TAP. This terminal should be pulled up to terminal 48 if the JTAG interface is not used.
JTDI	49	I	Test data input. JTDI is used to serially shift test data and test instructions into the device during operation of the TAP. This terminal should be pulled up to terminal 48 if the JTAG interface is not used.
JTDO	51	O	Test data output. JTDO is used to serially shift test data and test instructions out of the device during operation of the TAP.
JTMS	52	I	Test mode select. JTMS controls the operating state of JTAG. This terminal should be pulled up to terminal 48 if the JTAG interface is not used.
$\overline{\text{JTRST}}$	54	I	Test reset. $\overline{\text{JTRST}}$ is used for asynchronous reset of the JTAG controller. This terminal should be tied to GND if not used.

LED interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LACTIVE	67	O	LED activity indicator. LACTIVE indicates that the selected PHY is transmitting or receiving data. This signal is low for even-numbered (0, 2, 4, 6) ports and high for odd-numbered (1, 3, 5, 7) ports.
LDUPCOL	66	O	LED duplex/collision indicator. This LED status terminal has different meaning when in full- or half-duplex mode. In full-duplex mode, LDUPCOL is continuously driven active. In half-duplex mode, it is driven active for 20 ms after a collision. LDUPCOL indicates full-duplex mode and collisions for the currently selected PHY. This signal is active low for even (0, 2, 4, 6) ports and active high for odd (1, 3, 5, 7) ports.
LLINK	68	O	LED link indicator. LLINK indicates that the selected PHY has established a network link. This signal is low for even (0, 2, 4, 6) ports and high for odd (1, 3, 5, 7) ports.
LSEL0, 1	64	O	LED select PHY 0, 1. LED select indicator for PHY0 or PHY1, depends on polarity. This signal is high for PHY0 and low for PHY1.
LSEL2, 3	63	O	LED select PHY 2,3. LED select indicator for PHY2 or PHY3, depends on polarity. This signal is high for PHY2 and low for PHY3.
LSEL4, 5	62	O	LED select PHY 4,5. LED select indicator for PHY4 or PHY5, depends on polarity. This signal is high for PHY4 and low for PHY5.
LSEL6, 7	61	O	LED select PHY 6,7. LED select indicator for PHY6 or PHY7, depends on polarity. This signal is high for PHY6 and low for PHY7.

Terminal Functions (Continued)

miscellaneous interface

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
AIREF	41	A	Current reference. Used to set a current reference for the analog circuitry. AIREF must be connected to GND by a 2.5-kΩ 1% resistor.
ARBIAS	37	A	Bias resistor for the analog circuitry. Connect 7.5-kΩ 1% resistor between this pin and GND.
ATEST	39	A	Manufacturing test terminal. Leave unconnected.
CLK	43	I	Clock input. CLK connects a 20-MHz clock source to this terminal. The device enters a reset state on loss of CLK.
$\overline{\text{LOOPBACK}}$	47	I	Loopback. When low, $\overline{\text{LOOPBACK}}$ enables internal loopback in all eight PHYs. When asserted, data is internally wrapped within each PHY and does not appear on the network. While in the looped-back state, all network lines are placed in a noncontentious state.
MLT3BLOCK	69	I	MLT-3 block. Pulling MLT3 BLOCK terminal high enables the MLT-3 detector circuit and prevents the TNETE2008 from asserting link or carrier sense in the presence of 100BASE-T data. Setting MLT3BLOCK terminal low disables the MLT-3 detectors on all eight ports for applications that require this.
$\overline{\text{RESET}}$	46	I	Global reset. $\overline{\text{RESET}}$ is used to reset all eight PHY sections.
RCVTHRESH	44	I	Receive threshold. RCVTHRESH selects the threshold level of the receiver squelch circuit. For normal IEEE Std 802.3 operation, this pin should be tied low. Setting RCVTHRESH high slightly lowers the threshold level, allowing the PHY to receive data over extended lengths of cable for all eight PHYs.
$\overline{\text{PWRDOWN}}$	45	I	Power down. When asserted, $\overline{\text{PWRDOWN}}$ places all eight PHYs in a low power state. Transmitting and receiving are inhibited in this state.

† A = analog, I = input

not connected

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
NC	31, 32, 33, 34, 35, 56, 57, 58, 59, 60, 91, 92, 93, 94, 116, 117, 118, 119, 120	No connection. No internal connection for these terminals.

power interface

TERMINAL NAME	TERMINAL NO.	TYPE‡	DESCRIPTION
AGND	42	GND	Ground terminal for analog circuitry
AV_{DD}	40	PWR	V_{DD} terminal for analog circuitry. Connect to 3.3 V.
GND	55, 71, 81, 95, 96	GND	Logic ground terminals
RCVGND	109	GND	Ground terminal for receiver circuitry
$RCVV_{DD}$	112	PWR	V_{DD} terminals for receiver circuitry. Connect to 3.3 V.
XMTGND	3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 36, 115	GND	Ground terminals for transmit circuitry
$XMTV_{DD}$	38	PWR	V_{DD} terminal for transmit circuitry. Connect to 3.3 V.
V_{CC}	48	PWR	Power. Supply for JTAG port interface. Can be 5 V or 3.3 V, depending on test system interface requirements.
V_{DD}	50, 65, 76, 86	PWR	Logic V_{DD} terminals. Connect these to 3.3 V.

‡ GND = ground, PWR = power

Terminal Functions (Continued)

10BASE-T interface

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
RCVP0	114	A	Half of the receive pair to PHY0-PHY7. Differential line-receiver inputs connect to receive pair through transformer isolation.
RCVP1	111		
RCVP2	108		
RCVP3	106		
RCVP4	104		
RCVP5	102		
RCVP6	100		
RCVP7	98		
RCVN0	113	A	Half of the receive pair to PHY0-PHY7. Differential line-receiver inputs connect to receive pair through transformer isolation.
RCVN1	110		
RCVN2	107		
RCVN3	105		
RCVN4	103		
RCVN5	101		
RCVN6	99		
RCVN7	97		
XMTN0	2	A	Half of the transmit pair. Differential line-transmitter outputs from PHY0–PHY7.
XMTN1	6		
XMTN2	10		
XMTN3	14		
XMTN4	18		
XMTN5	22		
XMTN6	26		
XMTN7	30		
XMTP0	1	A	Half of the transmit pair. Differential line-transmitter outputs from PHY0–PHY7.
XMTP1	5		
XMTP2	9		
XMTP3	13		
XMTP4	17		
XMTP5	21		
XMTP6	25		
XMTP7	29		

† A = analog

functional description

Figure 3 is a simplified diagram of one of the eight TNETE2008 PHY interfaces. The diagram indicates the functionality of each PHY but is not a complete representation of the PHY structure or operation.

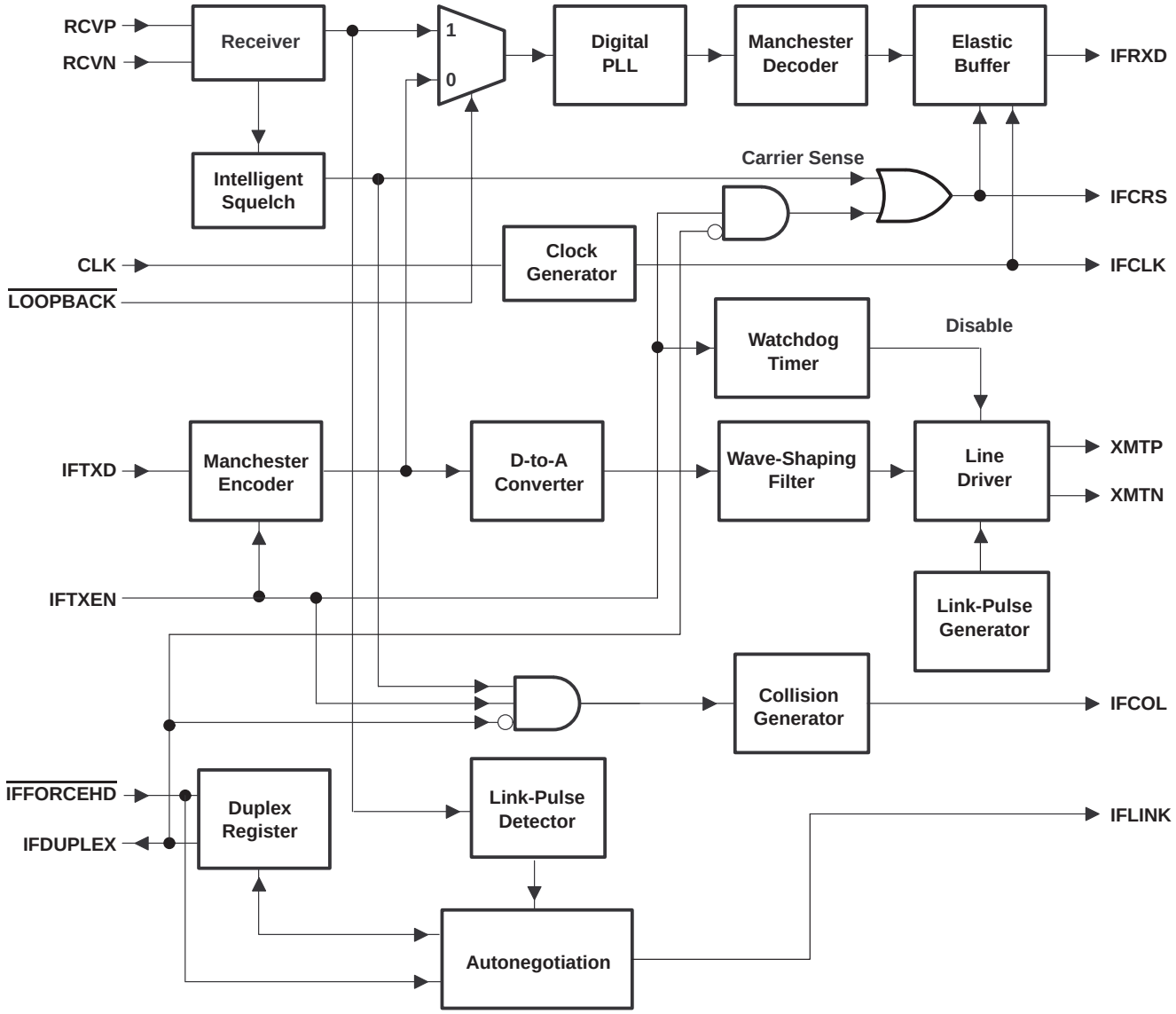


Figure 3. Block Diagram (x8)

10BASE-T differential line-transmitter function

Each TNETE2008 differential line driver drives a balanced, properly terminated twisted-pair transmission line with a nominal characteristic impedance of 100 Ω. In the idle state, the driver maintains a minimum differential output voltage while staying within the required common-mode voltage range.

The driver incorporates an on-chip wave-shaping and high-frequency filtering stage so the outputs can be connected directly to isolation transformers through series-termination resistors. No external filters are required.

After transmission has ceased on a PHY, and for a minimum of 250 ns, the driver maintains full differential outputs, which thereafter begin to decay to the minimum differential level.

Each PHY also transmits regular link pulses in compliance with IEEE Std 802.3.

In half-duplex mode, interface carrier sense (IFCRS) asserts during transmits.

10BASE-T differential line-receiver function

The line-receiver terminals of each PHY must be connected to a properly terminated transmission line via an external isolation transformer. The receiver establishes its own common-mode input-bias voltage. Data received from the network is output on the IFRXD terminals of the interface.

The receiver incorporates an intelligent squelch function that allows incoming data to pass only if the input amplitude is greater than a minimum signal threshold and a specific pulse sequence is received. This protects against impulse line noise being mistaken for signal or line activity. The squelch circuits quickly deactivate if received pulses fall outside the specifications. Over-long pulses are not mistaken as link pulses.

There are two choices for signal thresholds via the RCVTHRESH terminal. Selecting the lower squelch value (selected by pulling RCVTHRESH high) may operate over longer cables but does not meet IEEE minimum squelch levels. For this reason, it is recommended that this terminal be tied low. Each channel's squelch circuit contains an MLT-3 (100BASE-T data format) detector, which, when enabled via MLT3BLOCK pulled high, prevents the receiver from opening the squelch when MLT-3 data is present.

IFCRS is asserted while the squelch function is active to indicate that the circuit is allowing data to pass from the twisted pair. IFCRS is deasserted when the squelch circuit is disabling data flow, although the receive elastic buffer still may be outputting data.

jabber detection

Each PHY monitors the length of the packet being transmitted. If a single packet exceeds 24 ms, then a jabber condition is flagged. The output is disabled, the IFCOL (collision) signal is asserted, and the IFCRS signal is deasserted. To clear the jabber function, it is necessary to cease transmission for a minimum of 400 ms.

link test

When not in autonegotiation mode, each PHY transmits link pulses on the XMTP/XMTN outputs, separated by an interval of 19 ms.

The receiver looks for valid link pulses on the input pair. If a link pulse is not received within a given time interval, ≅ 100 ms, then the PHY enters a link-fail state. In this state, link pulses continue to be generated, and the receiver constantly looks for the link-pulse pattern. The PHY remains in this state until a valid receive packet or multiple legal link test pulses are received. When link pulses are not detected, the IFLINK signal is deasserted and transmission of data is inhibited. Also, an activated enabled MLT-3 decoder inhibits the receive function for MLT-3 encoded data and can, therefore, prevent assertion of IFLINK or, if already asserted, cause deassertion of IFLINK if the MLT-3 encoded data persists for longer than 100 ms.

polarity reversal

The TNETE2008 can detect reversed polarity of its receiver inputs (e.g., due to incorrect cable wiring). If at any time, seven consecutive inverted link pulses are detected, then, reversed polarity is assumed, and the octal swaps the RCVP and RCVN inputs of the affected PHY. Once a single, correct link pulse is received, good polarity is assumed.

autonegotiation

The TNETE2008 supports IEEE Std 802.3 autonegotiation to full duplex where allowed by a link partner. Each PHY on the device is capable of independent autonegotiation. When enabled, this feature allows a PHY to negotiate with the other PHY on its link segment, to establish their highest common protocol. Until a PHY has completed its negotiation, it does not assert IFLINK.

When autonegotiation is disabled for a PHY, via the extended multiplexed MAC interface, link is indicated on receipt of valid data or link pulses.

loopback test mode

By asserting the $\overline{\text{LOOPBACK}}$ terminal on the device, the transmit circuit of each PHY is looped to the corresponding receive circuit; therefore, transmit drivers do not forward any further packet data to the network but continue to send link pulses.

Since there is only one $\overline{\text{LOOPBACK}}$ terminal on the package, all eight PHYs simultaneously are placed into loopback mode.

While in loopback mode, all network receive activity, other than the link pulses, is ignored. However, squelch information is still processed, allowing the link status to be maintained under momentary loopback self-test.

During loopback, IFLINK is driven high for all channels, regardless of the state of the links on all channels. When $\overline{\text{LOOPBACK}}$ goes high, the true state of link on each channel is reported.

Although the TNETE2008 places no restrictions on the format of transmitted data, looped-back data should begin with a preamble and a start-of-frame delimiter to avoid spurious behavior of the receive-data recovery circuitry.

LED status indication

The TNETE2008 has 7 pins that drive 24 LEDs in a multiplexed format, as shown in Figure 4.

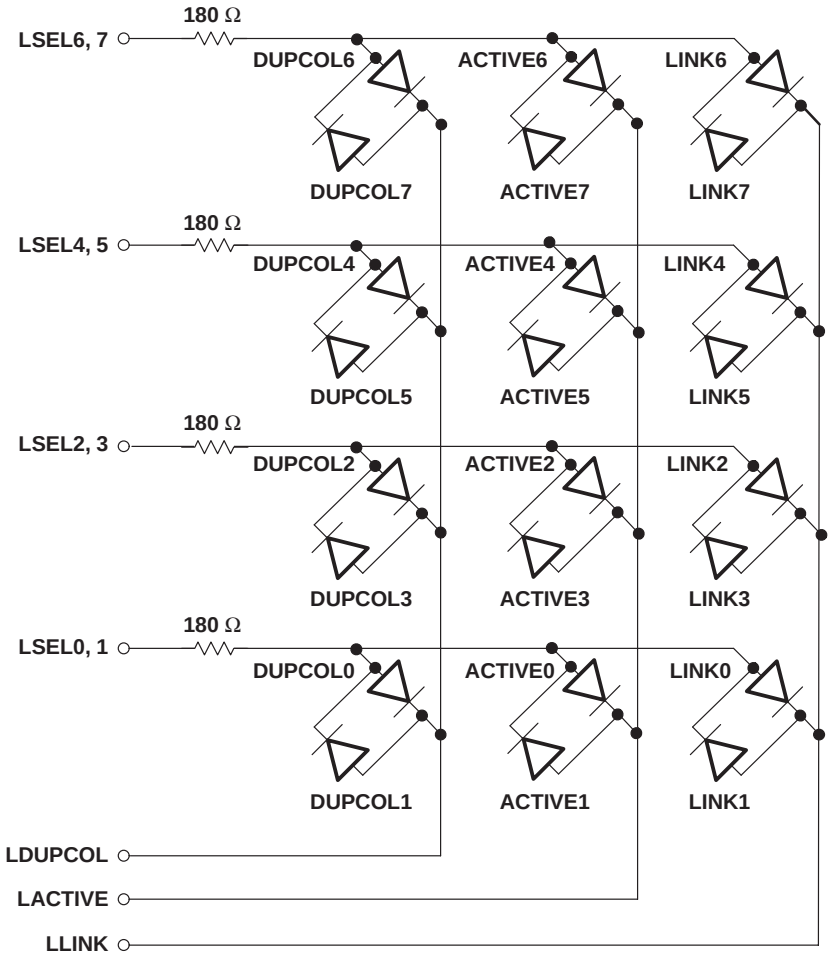


Figure 4. LED External Connection

status LED states

LINK LED	Illuminates when its PHY has established a valid link. The LED flashes at 2 Hz during autonegotiation.
ACTIVE LED	Illuminates when its PHY is transmitting or receiving data. The LED flashes at 19 Hz during continuous activity.
DUPCOL LED	Illuminates continuously when its PHY is in full-duplex mode and illuminates for a minimum duration of 20 ms when collisions occur in half-duplex mode. In the event of continuous or frequent collisions, this LED flashes at 19 Hz. In jabber mode it flashes at 1 Hz.

LED control signals

LACTVE, LLINK, and LDUPCOL	Outputs are each capable of sourcing and sinking up to 40 mA; active low for even, active high for odd-numbered channels.
LSEL0–LSEL7	Outputs each source/sink 10 mA; active low for odd, active high for even-numbered channels.

When $\overline{\text{RESET}}$ is active (low), all LEDs are illuminated during their time slot as a lamp test feature, regardless of the state of the corresponding status signal. CLK input must be driven with a valid clock for this to occur.

JTAG test access port

Compliant with IEEE Std 1149.1, the TAP is composed of five terminals. These terminals interface serially with the device and the board on which it is installed for boundary-scan testing. The TNETE2008 implements the following JTAG instructions:

INSTRUCTION TYPE	NAME	JTAG OPCODE	ACTION
Mandatory	EXTEST	0000	External boundary-scan test
Mandatory	SAMPLE/PRELOAD	0001	Initialization for boundary-scan test
Optional	IDCODE	0100	Scans out TNETE2008 identification code
Optional	HIGHZ	0011	Sets all digital output pins on TNETE2008 to high impedance
Mandatory	BYPASS	1111	Connects 1-bit bypass register between TDI and TDO

The IDCODE for the TNETE2008 is:

CODE	VARIANT	PART NUMBER	MANUFACTURER	LEAST SIGNIFICANT BYTE
Binary	0000b	0000000001010000	000 0001 0111b	1b

The JTAG terminals do not have internal pullup resistors, so, to comply fully with IEEE Std 1149.11, external resistors must be connected to JTMS, JTCLK, JTDI, and $\overline{\text{JTRST}}$. All other JTAG opcodes are reserved for manufacturing test and should not be used.

global reset logic

At initial power up, the TNETE2008 performs an internal reset. No external reset circuitry is required. However, operation of the TNETE2008 is not specified for 50 ms after power up.

During operation, a full reset of the device can be performed by taking $\overline{\text{RESET}}$ low for not less than 50 μs. Operation of the device is not ensured for 5 ms after reset ends.

The device resets itself if CLK is lost for any reason. CLK loss is detected in 200 μs.

Data is not valid on the multiplexed MAC interface until normal operation resumes, after any reset, and then after two complete IFSYNC cycles have passed.

All signals in the multiplexed MAC interface are driven to 0 during reset, except for IFSYNC, which is driven to 1 during reset.

synchronous PHY interface

To ease the pin-count burden on switching-application devices, Texas Instruments developed a multiplexed interface, which allows multi-PHY devices to be connected to switching cores without using many terminals. To achieve the reduction in terminal count, the interface takes advantage of the fact that modern silicon is able to operate at frequencies much higher than the 10-MHz data rate of the standard interface.

The receive and transmit data are transferred over a nibble-wide bus, (see Figure 5). Table 1 describes the signals on the interface. Any given port only transfers data at 2.5 MHz (2.5 MHz $\times$ 4 bits = 10 Mbit/s). The remaining control and status signals are sampled at the reduced rate of 2.5 MHz.

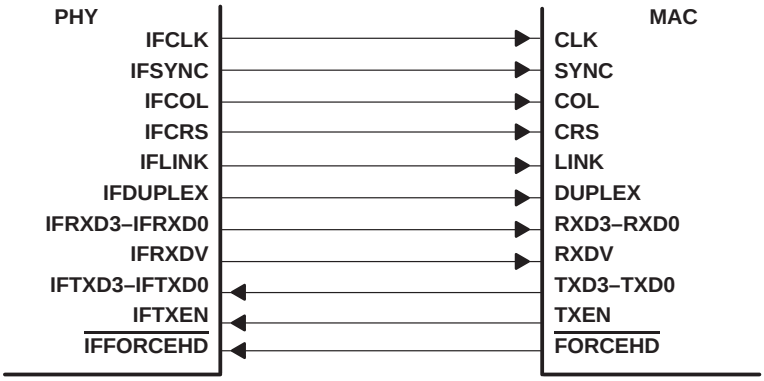


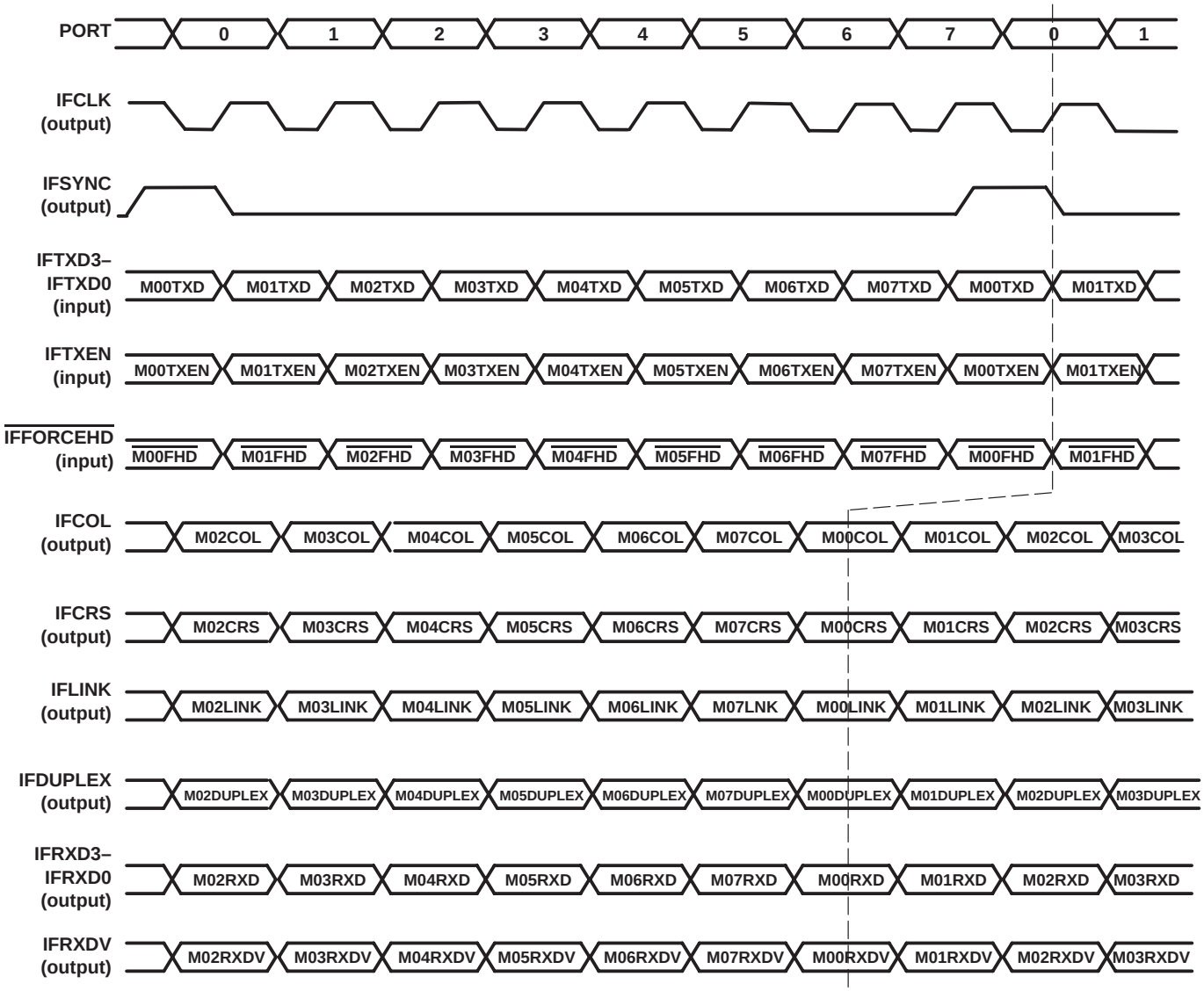
Figure 5. Multiplexed 17-Pin Interface for Eight Ports

The interface runs synchronously to a TNETE2008 generated clock. The information (MAC $\rightarrow$ TNETE2008) for the first port (port 0) is presented on the interface when IFSYNC is high; the next clock cycle the interface carries the information for the second port. This process continues with each port using the interface for one cycle. When all ports have been processed in this manner, the sequence resumes with the first port and again IFSYNC is asserted. To improve latency-related issues, the data from the TNETE2008 to the MAC is skewed by two slots as shown by the dashed line in Figure 6. This allows the MAC to respond to input signals from the TNETE2008 in the same 400-ns cycle, rather than waiting for the next 400-ns cycle, which would be the case if the signals were not skewed.

If the mode to be advertised during autonegotiation arrives on IFTXD3–IFTXD0 during link-invalid, $\overline{\text{IFFORCEHD}}$ can be tied high or used to restart autonegotiation.

timing diagram

The basic signals on the multiplexed interface and their alignment to IFCLK and IFSYNC are shown in Figure 6. All input signals change on the rising edge of IFCLK and are sampled by the TNETE2008 on the rising edge of IFCLK. All output signals, except IFSYNC, change on the falling edge of IFCLK and should be sampled by the MAC on the rising edge of IFCLK. The IFSYNC output changes on the rising edge of IFCLK and should be sampled by the MAC on the falling edge of IFCLK.



Note: Dashed line shows data from TNETE2008 to MAC is skewed by two slots.

Figure 6. MAC Interface

bit ordering within nibbles

Normally, network packet data is transferred from the TNETE2008 to the MAC for a particular PHY when, during its time slot, IFRXDV and IFLINK are both high. There is an opportunity to send other information to the MAC when either of these two signals is not high. Similarly, the MAC transfers packet information to a particular PHY in the TNETE2008 when IFLINK and IFTXEN are both high during that PHY's time slot. There is an opportunity to send other information to TNETE2008 when either of these two signals is not high.

Currently, the only extended data used in this interface is sending allowed autonegotiating modes to the PHY channels when IFTXEN and IFLINK are both low, and reporting mode, when autonegotiation is successfully completed, and when IFLINK and IFRXDV both are low.

Table 1 shows the possible classes of data based on IFLINK and IFTXEN for data to the TNETE2008 from the MAC, and based on IFLINK and IFRXDV for data from the TNETE2008 to the MAC.

Table 1. Transmit and Receive Data Nibbles

IFLINK	IFTXEN	IFTXD3–IFTXD0	COMMENT
0	0	0000–1111	Extension-specific information
0	1	Reserved	Reserved for future extension
1	0	0000	Normal interframe
1	0	0001–1111	Reserved
1	1	0000–1111	Normal data transmission

IFLINK	IFRXDV	IFRXD3–IFRXD0	COMMENT
0	0	0000–1111	Extension-specific information
0	1	Reserved	Reserved for future extension
1	0	0000	Normal interframe
1	0	0001–1111	Reserved
1	1	0000–1111	Normal data transmission

Figure 7 defines the bits-to-nibble-to-byte ordering and translation used in the multiplexed interface.

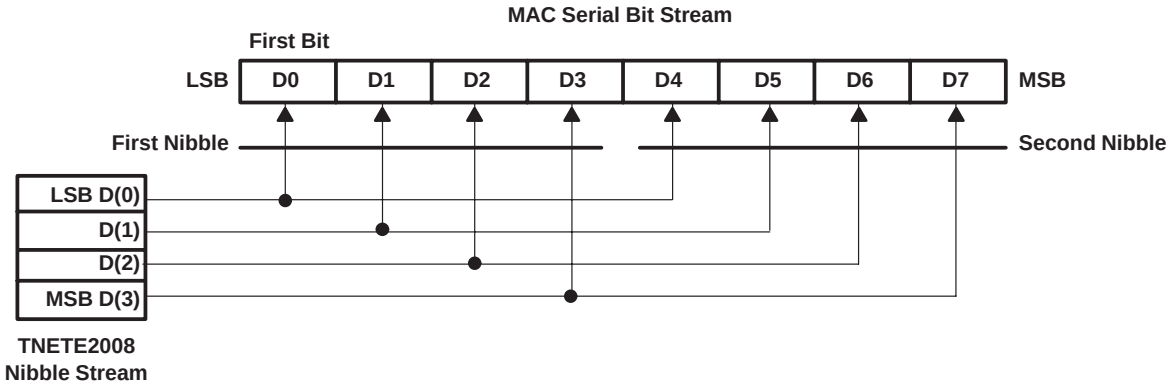


Figure 7. Data Stream

non-data MAC-to-PHY and PHY-to-MAC control exchanges

Autonegotiation parameters can be sent to the TNETE2008 by the MAC and the results of the link negotiation reported to the MAC using the multiplexed data pins during non-network data time (IFLINK = 0). This signaling system also allows the MAC to force the configuration of the TNETE2008 duplex and pause modes to those it requested.

When IFLINK and IFTXEN are deasserted, duplex, pause, speed, and force configuration information is transferred from MAC to TNETE2008 on terminals IFTXD0, IFTXD1, IFTXD2, and IFTXD3, respectively.

When IFLINK and IFRXDV are deasserted, duplex, pause, and speed information is transferred from TNETE2008 to MAC on terminals IFRXD0, IFRXD1, and IFRXD2, respectively.

Figure 8 shows the control information exchange for the case where the MAC is not forcing the configuration of the link. In this case, the link configuration is determined by autonegotiation. The TNETE2008 latches the final requested values just before FLP exchange commences. The diagrams show only one channel; for clarity, time slices from other PHYs are not shown interspersed with the sample channel.

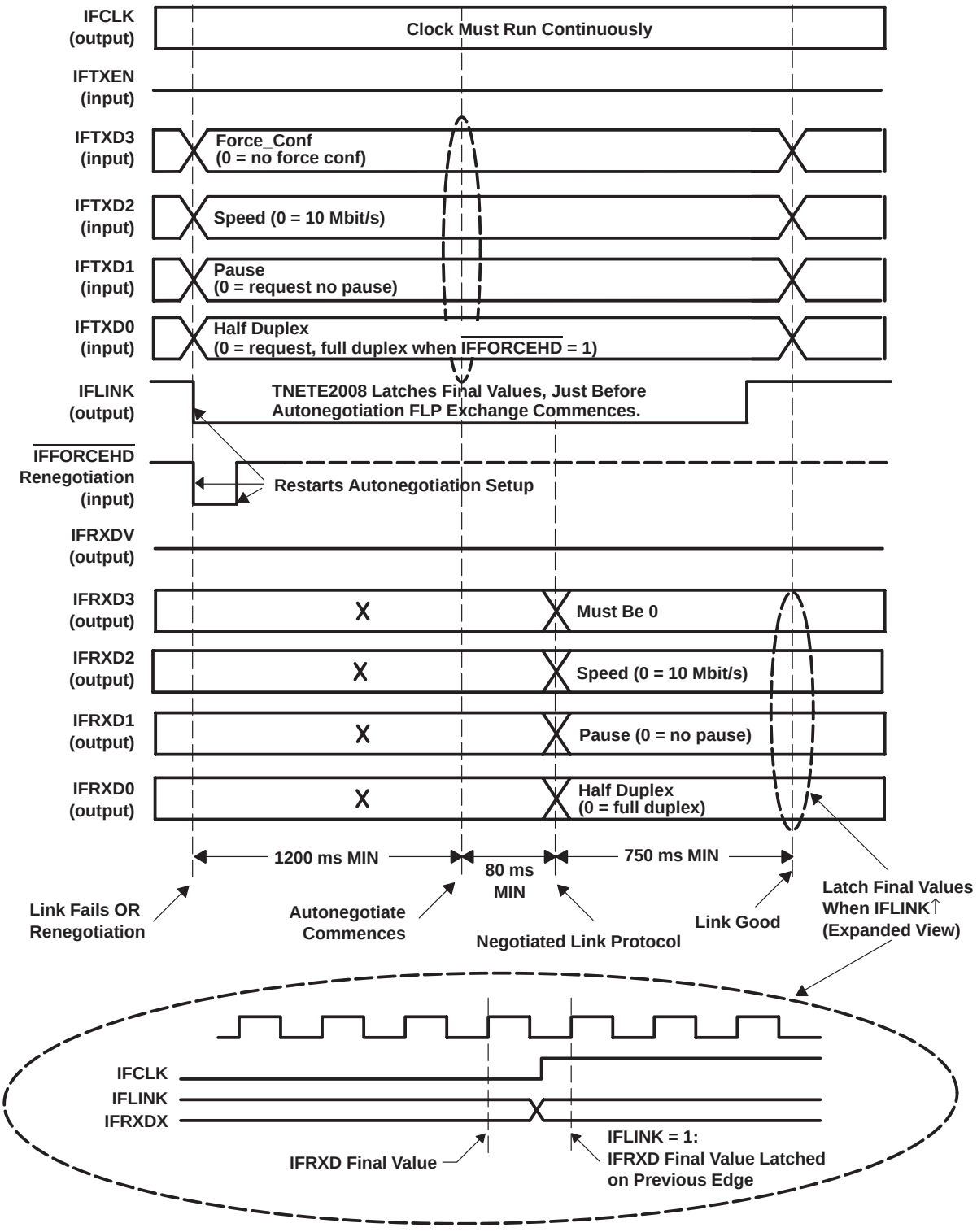


Figure 8. MAC-to-PHY, PHY-to-MAC Control Exchanges for Not Force Configuration Mode

non-data MAC-to-PHY and PHY-to-MAC control exchanges

Figure 9 shows the control information exchange for the case where the MAC is forcing the configuration of the link. In this case the link is established by link pulse detection and is configured as specified by the MAC. The TNETE2008 latches the final values just before IFLINK asserts. The force configuration mode should be used only when the abilities of the link partner are known or set to be the same as those forced. Failure to do this could result in an incompatibly configured link, e.g., TNETE2008 full duplex and link partner half duplex.

IFLINK going low or any transition on $\overline{\text{IFFORCEHD}}$ can trigger renegotiation. If a new trigger occurs before a negotiation completes, the process starts over at the beginning of an enforced 1.2-s wait. At the end of an undisturbed 1.2-s wait, the state of $\overline{\text{IFFORCEHD}}$ and IFTXD3–IFTXD0 determines the modes advertised to the link partner. $\overline{\text{IFFORCEHD}}$ low commands half duplex; only $\overline{\text{IFFORCEHD}}$ high allows the value clocked from IFTXD0 to determine duplex mode. In the force configuration mode, IFTXD0 alone determines the duplex mode for the next time link is established.

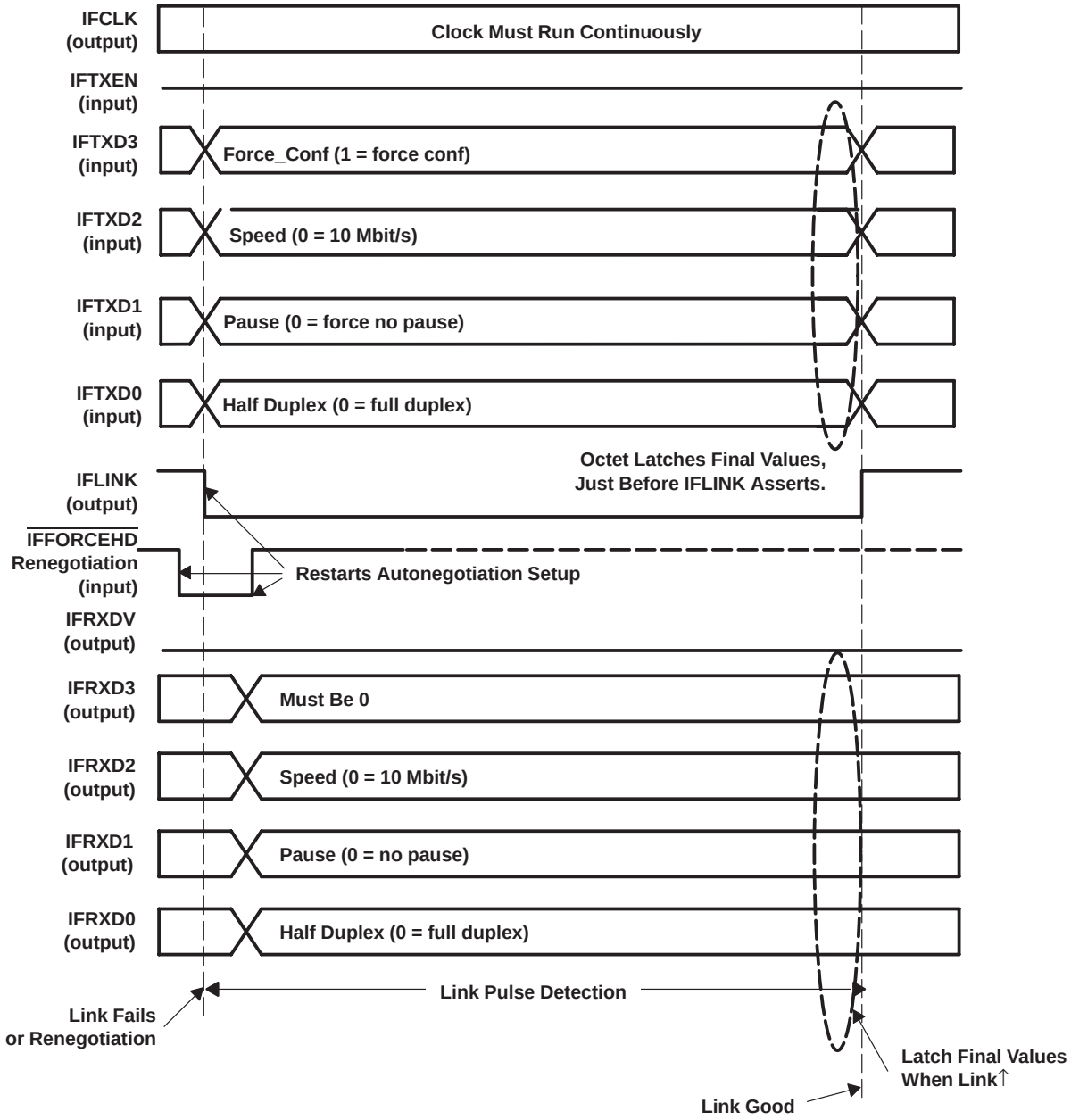


Figure 9. MAC-to-PHY, PHY-to-MAC Control Exchanges for Force Configuration Mode

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Normal power-supply voltage . . . . . 3.3 V ± 5%
DC voltage range applied to logic outputs . . . . . –0.05 V to V_{DD}MAX
DC voltage applied to logic input . . . . . 3.6 V
DC differential voltage at receiver pins . . . . . ±5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 5.25 V
Operating case temperature range, T_C . . . . . 0°C to 95°C
Thermal resistance, junction to ambient, $R_{\theta JA}$ . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND, and all GND terminals should be routed to minimize inductance to system ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.15	3.3	3.45	V
V_{CC}	JTAG supply voltage (see Note 2)		5		V
V_{CC}	JTAG supply voltage (see Note 2)		3.3		V
V_{IH}	High-level input voltage	2		V_{DD}+0.5	V
V_{IL}	Low-level input voltage (see Note 3)	–0.5		0.8	V
I_{OH}	High-level output current			–4	mA
I_{OL}	Low-level output current			4	mA
I_{OH}	High-level output current LED function terminals			–40	mA
I_{OL}	Low-level output current LED function terminals			40	mA
I_{OH}	High-level output current LED group select terminals			–10	mA
I_{OL}	Low-level output current LED group select terminals			10	mA

NOTES: 2. V_{CC} is selected by JTAG test system interface requirements.
3. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = MAX				0.5	V
I_{OZ}	High-impedance current					±10	µA
I_{IH}	High-level output current	V_{IN} = MAX				±10	µA
I_{IL}	Low-level output current	V_{IN} = GND				±10	µA
I_{DD}	Supply current	V_{DD} = MAX	See Note 4		110	125	mA
			See Note 5		220	280	
C_{din}	Digital inputs				1.5		pF
C_{dout}	Digital outputs				1		pF
C_{lsel}	LED select outputs (LSELxx)				3.5		pF
C_{lstat}	LED status outputs				10		pF
C_{jin}	JTAG inputs				2.5		pF
C_{jout}	JTAG outputs				3		pF

NOTES: 4. Full-duplex mode, while transmitting and receiving maximum data packet size with correct line termination and minimum interframe gaps. This is a per-port value.
5. Full-duplex mode, valid link on all PHYs, and no data activity. This is total device value.

oscillator requirements

	MIN	NOM	MAX	UNIT
CLK frequency		20		MHz
CLK frequency error	–100		100	ppm
CLK duty cycle	40		60	%
V_{OH}	2		V_{DD}	V
T_{rise}, T_{fall} (see Note 6)			6	ns

NOTE 6: Measured at 10%–90% transistion low-to-high or high-to-low points

operating characteristics over recommended operating conditions

clock sync delay (see Figure 10)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(IFSYNC)}$	Delay time from IFCLK↑ to IFSYNC state change	–2	10	ns

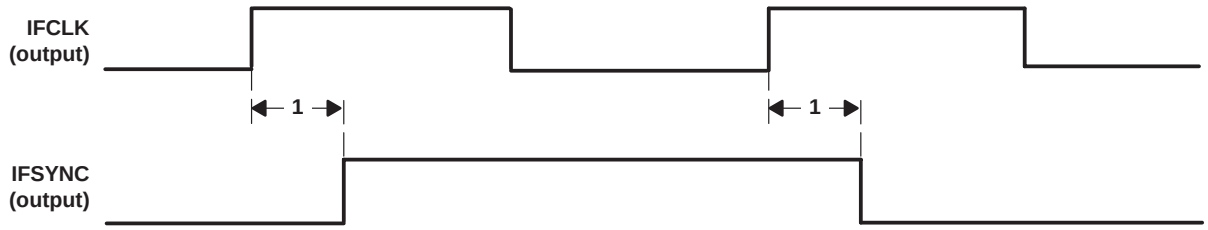


Figure 10. Clock Sync Delay

clock limits (see Figure 11)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(IFCLK)}$	Cycle time		50		ns
2	$t_{w(IFCLK)}$	Pulse width high	22.5		27.5	ns
3	$t_{w(IFCLK)}$	Pulse width low	22.5		27.5	ns
4	$t_{r(IFCLK)}$	Rise time (see Note 7)			2	ns
5	$t_{f(IFCLK)}$	Fall time (see Note 7)			2	ns

NOTE 7: Measured between 10% and 90% levels of IFCLK amplitude

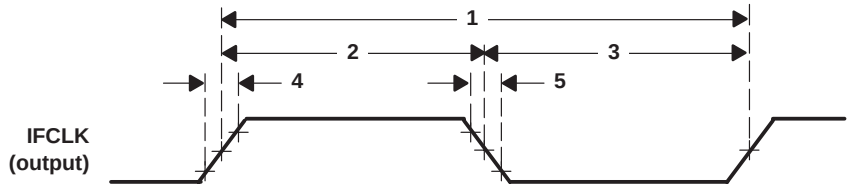


Figure 11. Clock Limits

receive output interface (see Figure 12)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(IFCOL)}$	Delay time, from IFCLK↓ to IFCOL valid (see Note 8)	–2	10	ns
2	$t_{d(IFCRS)}$	Delay time, from IFCLK↓ to IFCRS valid (see Note 9)	–2	10	ns
2	$t_{d(IFLINK)}$	Delay time, from IFCLK↓ to IFLINK valid	–2	10	ns
2	$t_{d(IFRXD)}$	Delay time, from IFCLK↓ to IFRXD valid (see Note 10)	–2	10	ns
2	$t_{d(IFRXDV)}$	Delay time, from IFCLK↓ to IFRXDV invalid (see Note 11)	–2	10	ns
2	$t_{d(IFDUPLEX)}$	Delay time, from IFCLK↓ to IFDUPLEX valid	–2	10	ns

NOTES: 8. For IFRX data, the TNETE2008 asserts IFCOL during the appropriate time slot if there was a collision event during previous time slot.
9. For IFRX data, the TNETE2008 asserts IFCRS during the appropriate time slot if carrier was detected during previous time slot.
10. The TNETE2008 does not echo transmit data back on the IFRXD3–IFRXD0 terminals during normal operations.
11. The TNETE2008 asserts IFRXDV for IFRX data if there are four valid bits of data in the nibble. Dribble bits at the end of the frame are discarded.

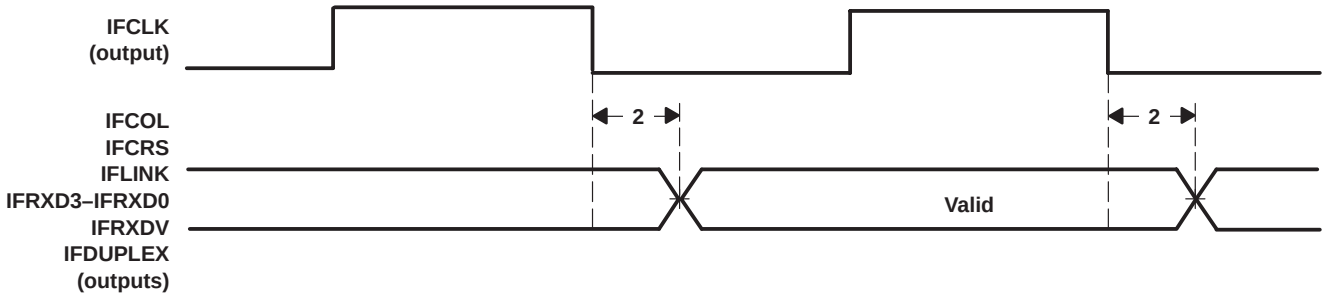


Figure 12. Multiplexed Receive Interface

transmit input interface (see Figure 13)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{su(IFTXEN)}$	Setup time, from IFTXEN valid to IFCLK↑	15		ns
2	$t_{su(IFTXD)}$	Setup time, from IFTXD valid to IFCLK↑	15		ns
2	$t_{su(IFFORCEHD)}$	Setup time, from $\overline{\text{IFFORCEHD}}$ valid to IFCLK↑	15		ns
3	$t_{h(IFTXEN)}$	Hold time, from IFCLK↑ to IFTXEN invalid	0		ns
3	$t_{h(IFTXD)}$	Hold time, from IFCLK↑ to IFTXD invalid	0		ns
3	$t_{h(IFFORCEHD)}$	Hold time, from IFCLK↑ to $\overline{\text{IFFORCEHD}}$ invalid	0		ns

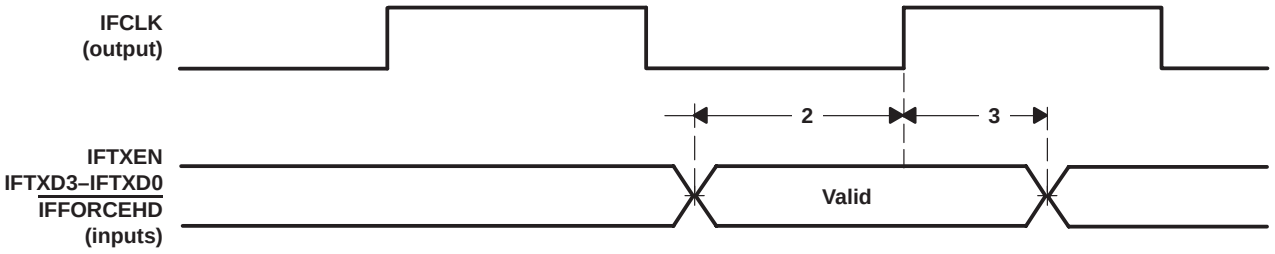


Figure 13. Multiplexed Transmit Interface

LED drive timing

To sample this interface, count 32 clocks from the falling edge of $\overline{\text{RESET}}$, and take samples every 32 clocks (1600 ns) thereafter. Sampling is shown in Table 2.

LED drive (see Figure 14)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{d(Sample\ X)}$	Delay time from RESET↓ to S0 active	625		750	ns
2	$t_{w(Sample\ X)}$	Pulse duration (see Notes 12 and 13)		1600		ns

NOTES: 12. LED interface runs synchronously to CLK signal, 32 clocks/sample at constant numbers of CLK periods. Phase of CLK, relative to LSEL transitions, is not controlled.
13. Active low for odd channels and active high for even channels

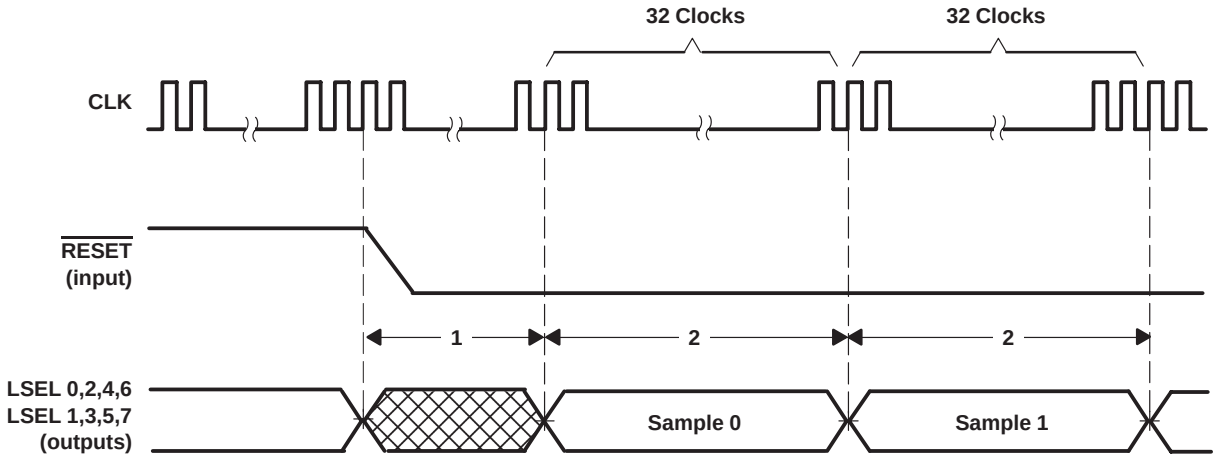


Figure 14. LED Drive Timing

Table 2. LED Drive Timing

SAMPLE (SEE NOTE 14)	LSEL0,1	LSEL2,3	LSEL4,5	LSEL6,7
0	$\overline{\text{link1}}$	$\overline{\text{link3}}$	$\overline{\text{link5}}$	$\overline{\text{link7}}$
1	active0	active2	active4	active6
2	dupcol0	dupcol2	dupcol4	dupcol6
3	link0	link2	link4	link6
4	$\overline{\text{active1}}$	$\overline{\text{active3}}$	$\overline{\text{active5}}$	$\overline{\text{active7}}$
5	$\overline{\text{dupcol1}}$	$\overline{\text{dupcol3}}$	$\overline{\text{dupcol5}}$	$\overline{\text{dupcol7}}$
6 (same as sample 0)	$\overline{\text{link1}}$	$\overline{\text{link3}}$	$\overline{\text{link5}}$	$\overline{\text{link7}}$
7 (same as sample 1)	active0	active2	active4	active6

NOTE 14: In general, sample (n) = sample (n + 6), sample (n – 6).

receive-data timing

The TNETE2008 buffers receive data in an elastic first-in, first-out (FIFO) buffer so that receive data can be synchronous to the TNETE2008 20-MHz clock.

receive data (see Figure 15)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{d(RDLAT)}$	Receive-data latency time	1350	1950	2550	ns
2	$t_{d(CRS)}$	Carrier sense assertion delay	125	850	1300	ns
3	$t_{d(RDV)}$	Delay time, from RCVP/RCVN valid to IFRXD valid	1800	2850	3800	ns
4	$t_{d(CRSHO)}$	Delay time, from RCVP/RCVN idle to IFCRS↓	0	0	450	ns

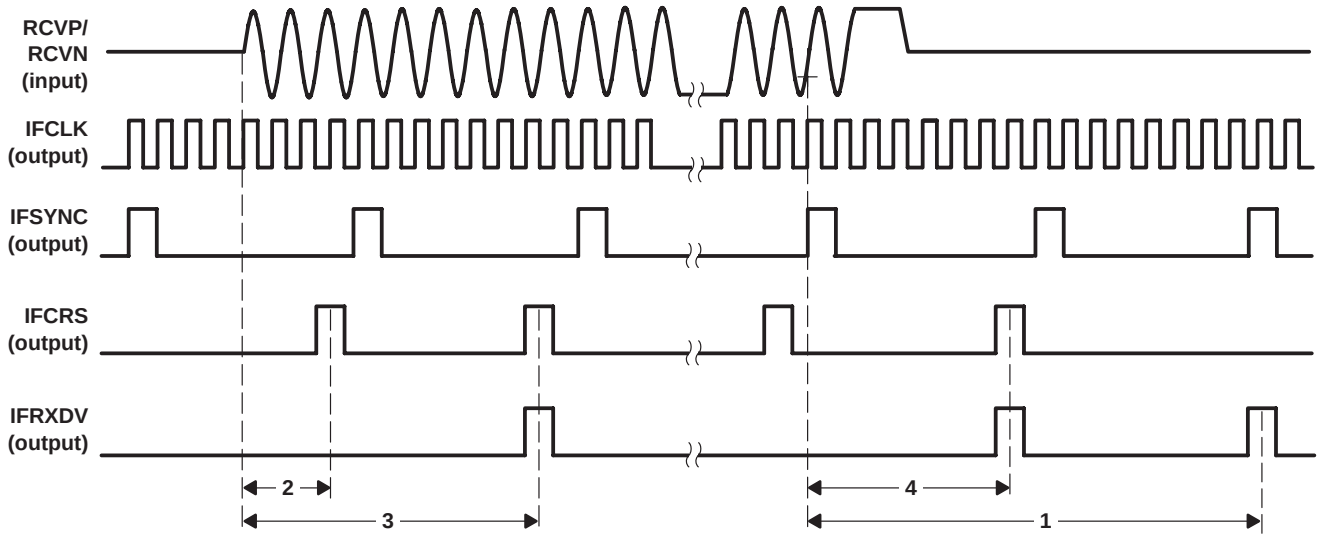


Figure 15. Receive Data

transmit data (see Figure 16)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{d(XMTP/N)}$	Delay time from IFTXEN↑ to XMTP/XMTN active	50	75	100	ns
2	$t_{d(TDLAT)}$	Transmit-data latency time	50	175	500	ns

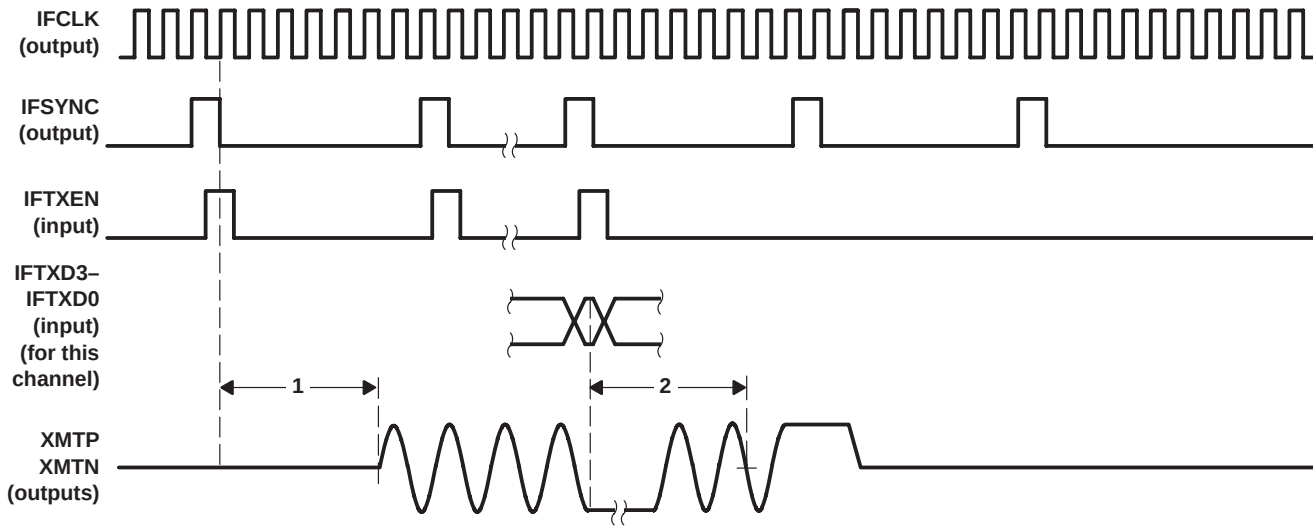


Figure 16. Transmit Data

collision-detection timing

IFCOL is asserted for a minimum of 600 ns when transmission and reception of data occur simultaneously and the mode is in half duplex. IFCOL is not active during link fail or in full-duplex mode. Figure 17 shows the collision-detect timing. During a collision, the data output on IFRXD is not valid received data.

collision detect (see Figure 17)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{d(IFCOLON)}$	Delay time, collision detect RCVP/RCVN valid to IFCOL↑	125	475	1300	ns
2	$t_{d(IFCOLOFF)}$	Delay time, collision off IFTXEN↓ to IFCOL↓	600	700	1450	ns

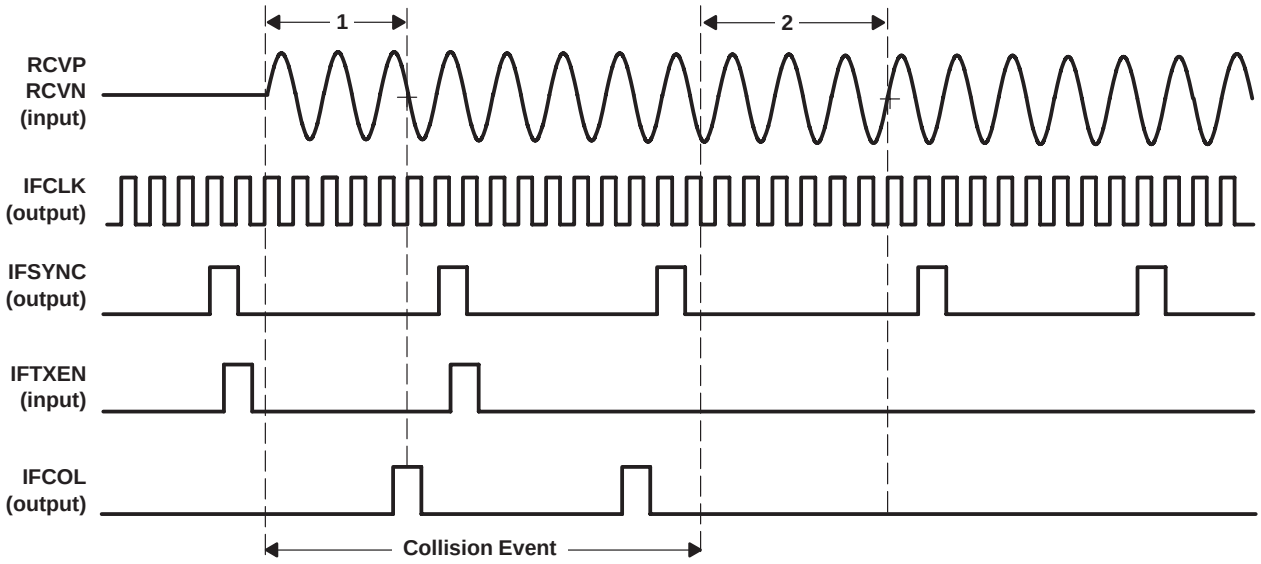


Figure 17. Collision Detect

loopback (see Figure 18)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{d(RDLAT)}$	Receive-data latency time	1350	1900	2550	ns
2	$t_{d(LCRS)}$	Carrier sense assertion delay	300	300	300	ns
3	$t_{d(IFRXDV)}$	Delay time from TXEN↑ active to IFRXDV↑	1750	2300	3100	ns
4	$t_{d(LCRSHO)}$	Delay time from receive idle to IFCRS↓	0	0	300	ns

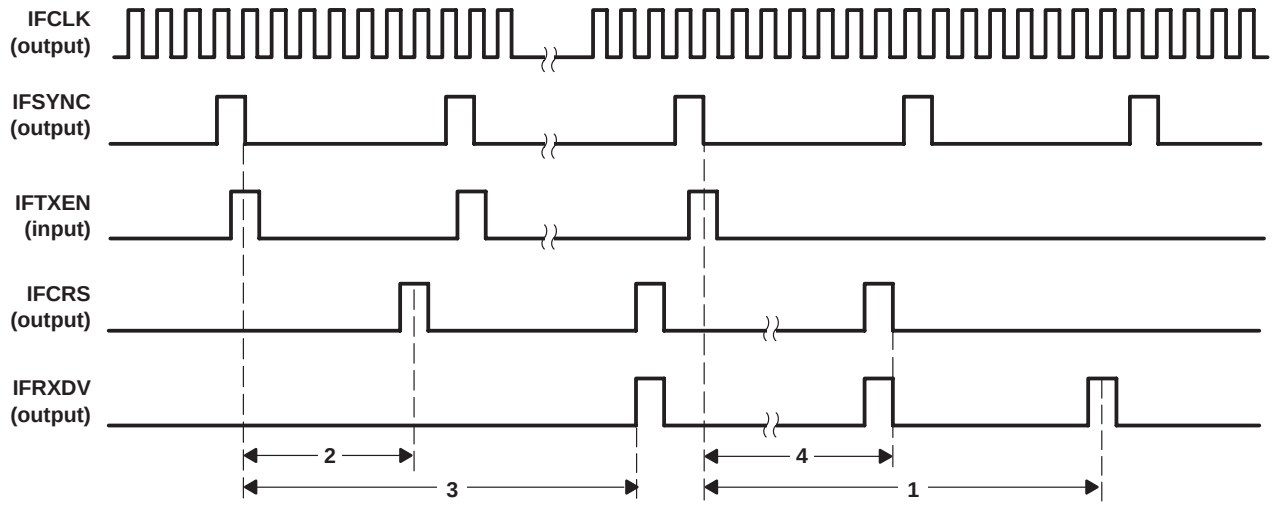


Figure 18. Loopback

PARAMETER MEASUREMENT INFORMATION

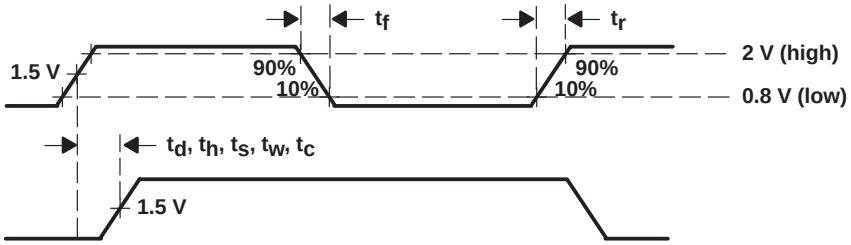
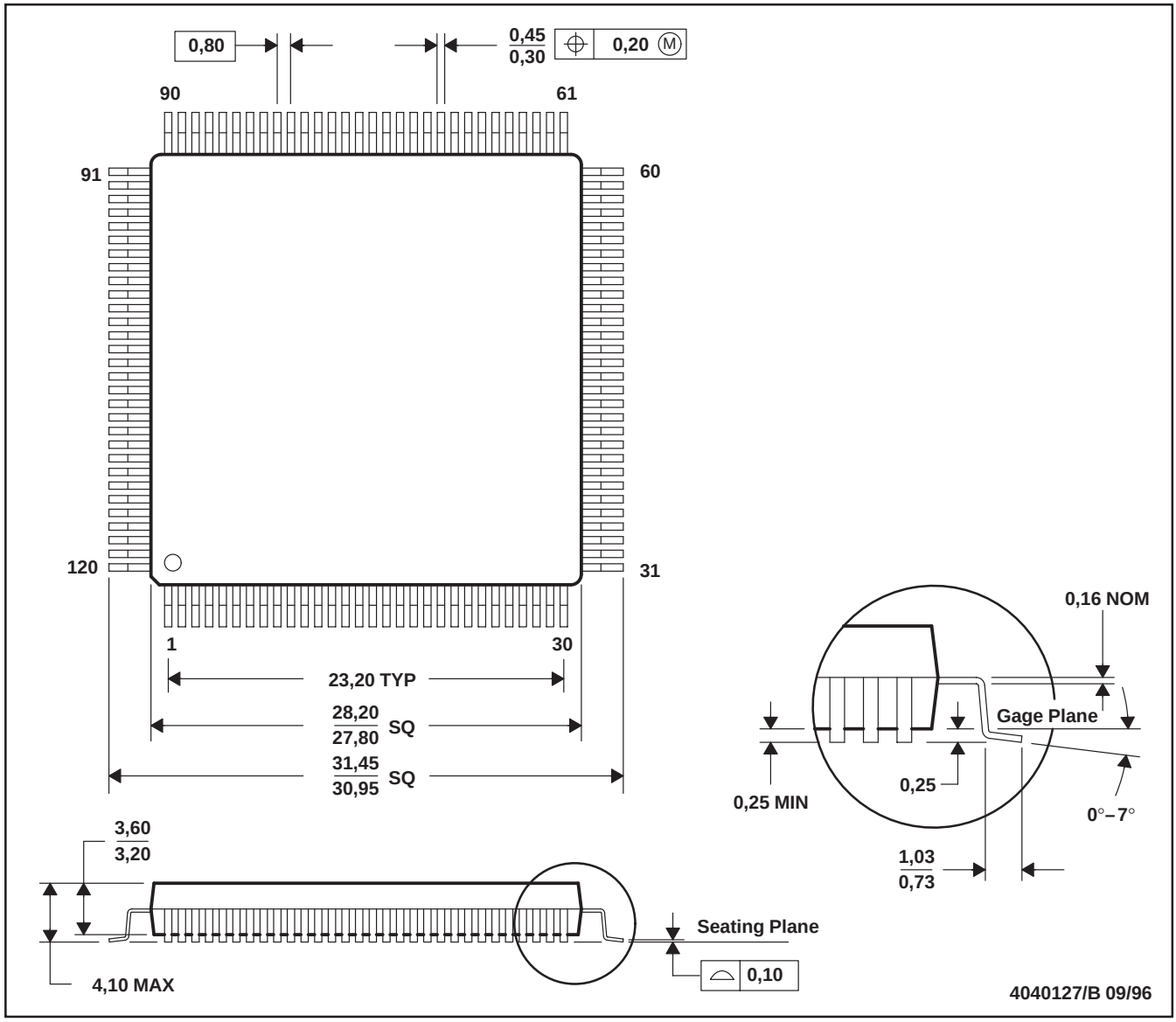


Figure 19. Parameter Measurement

MECHANICAL DATA

PBE (S-PQFP-G120) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat spreader (HSP)
D. Falls within JEDEC MS-022

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TNETE2008PBE	OBSOLETE	HQFP	PBE	120		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265