

March 2006

The SP8714 is a switchable divide by 32/33, 64/65 programmable divider which is guaranteed to operate up to 2100MHz. It will operate from a supply of 2.7V to 5.25V and requires typically 6.8mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers.

### FEATURES

- Operation to 2100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.25V
- Power Down Facility for Battery Economy
- Latched Modulus Control Input
- Push Pull Output Drive
- ESD Protection on All Pins†

### APPLICATIONS

- Cellular Telephones
- Cordless Telephones

† ESD precautions must be observed

Ordering Information		
Industrial Temperature Range		
Miniature Plastic SOIC Package		
SP8714/IG/MPAS	8 Pin SOP/SOIC	Tubes
SP8714/IG/MPAC	8 Pin SOP/SOIC	Tape & Reel
SP8714/IG/MPBQ	8 Pin SOP/SOIC*	Tape & Reel
SP8714/IG/MPBP	8 Pin SOP/SOIC*	Tubes
*Pb Free Matte Tin		

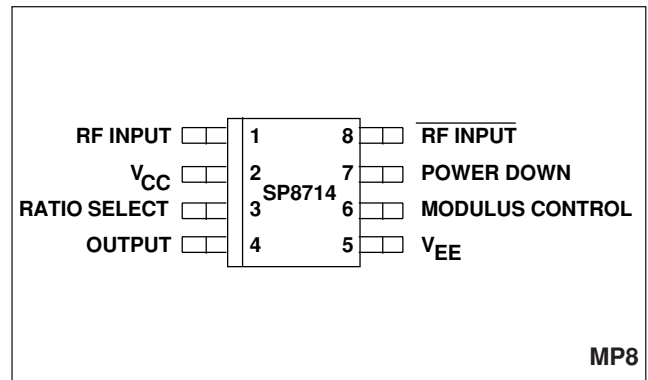


Fig. 1 Pin connections - top view

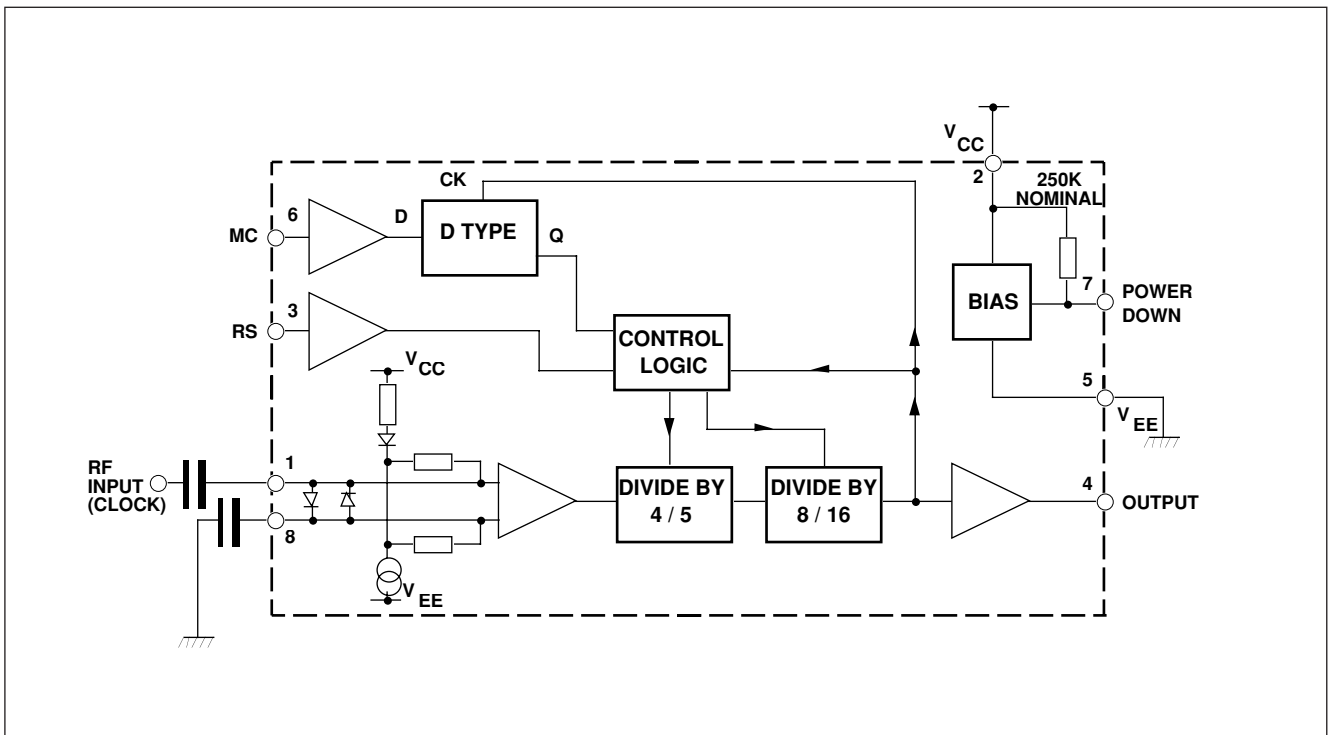


Fig. 2 Block diagram

# SP8714

## ABSOLUTE MAXIMUM RATINGS

Supply voltage ( $V_{EE}=0V$ )	(note 1)	-0.5V to 7V
Control and RF inputs,		
RF output ( $V_{EE}=0V$ )	(note 1)	-0.5V to $V_{CC}+0.5V$
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

## ELECTRICAL CHARACTERISTICS

Guaranteed over the following conditions (unless otherwise stated):

$V_{CC}=+2.7V$  to  $+5.25V$  (with respect to  $V_{EE}$ ), Output load (pin 4) = 10pF,  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$  (note 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current (note 3)		6.8	8.5	mA	Power down input low
Supply current (note 3)		8	50	$\mu A$	Power down input high
Power down high	$V_{CC}-0.5$		$V_{CC}$	V	
Power down low	0		$V_{CC}-2.0$	V	
Modulus control high (note 4)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 32 or 64
Modulus control low (note 4)	0		$0.4V_{CC}$	V	Divide by 33 or 65
Ratio select high (note 4, 9)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 32 or 33
Ratio select low (note 4, 9)	0		$0.4V_{CC}$	V	Divide by 64 or 65
Max. sinewave input frequency	2100			MHz	See Figure 5
Min. sinewave input frequency			200	MHz	See Figure 5
Min. RF input voltage			50	mV RMS	RF input 200MHz to 2100MHz. See Figure 5
Max. RF input voltage	200			mV RMS	RF input 200MHz to 2100MHz. See Figure 5
Output level (pin 4)	500	600		mV p-p	
Modulus set-up time, $t_s$ (notes 5,6,8)	10			ns	RF input = 1GHz
Modulus hold time, $t_h$ (notes 6,8)			1	ns	RF input = 1GHz
Power down time, $t_{pd}$ (notes 7,8)			10	$\mu s$	See Figure 9
Power down recovery time, $t_{pu}$ (notes 7,8)			8	$\mu s$	See Figure 9

### NOTES

- All electrical testing is performed at +85°C.
- Typical values are measured at +25°C and  $V_{CC} = +5V$ .
- Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
- Modulus control is latched at the end of the previous cycle.
- See Figure 4.
- See Figure 8.
- These parameters are not tested but are guaranteed by design.
- The ratio select pin is not intended to be switched dynamically.

**OPERATING NOTES**

The RF inputs are biased internally and are normally coupled to the signal source with suitable capacitors.

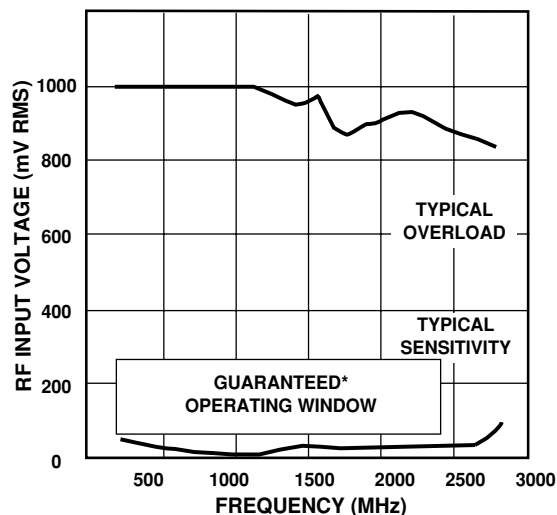
The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8714 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/ $\mu$ s.

POWER DOWN (pin 7) is connected internally to a pull-up resistor. If the battery economy facility is not used, pin 7 should be connected to  $V_{EE}$ .

Ratio Select (Pin 3)	Modulus Control (Pin 6)	Division Ratio
L	L	65
L	H	64
H	L	33
H	H	32

Table 1 Truth table



\* Tested as specified in table of Electrical Characteristics

Fig. 3 Typical input characteristics

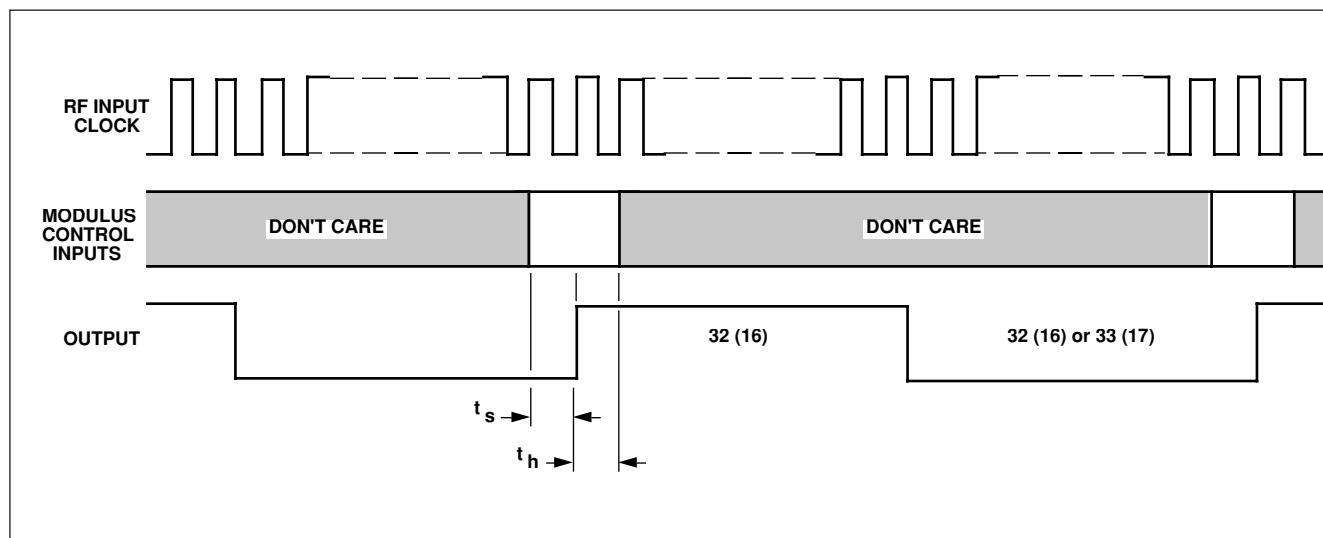


Fig. 4 Modulus control timing diagram

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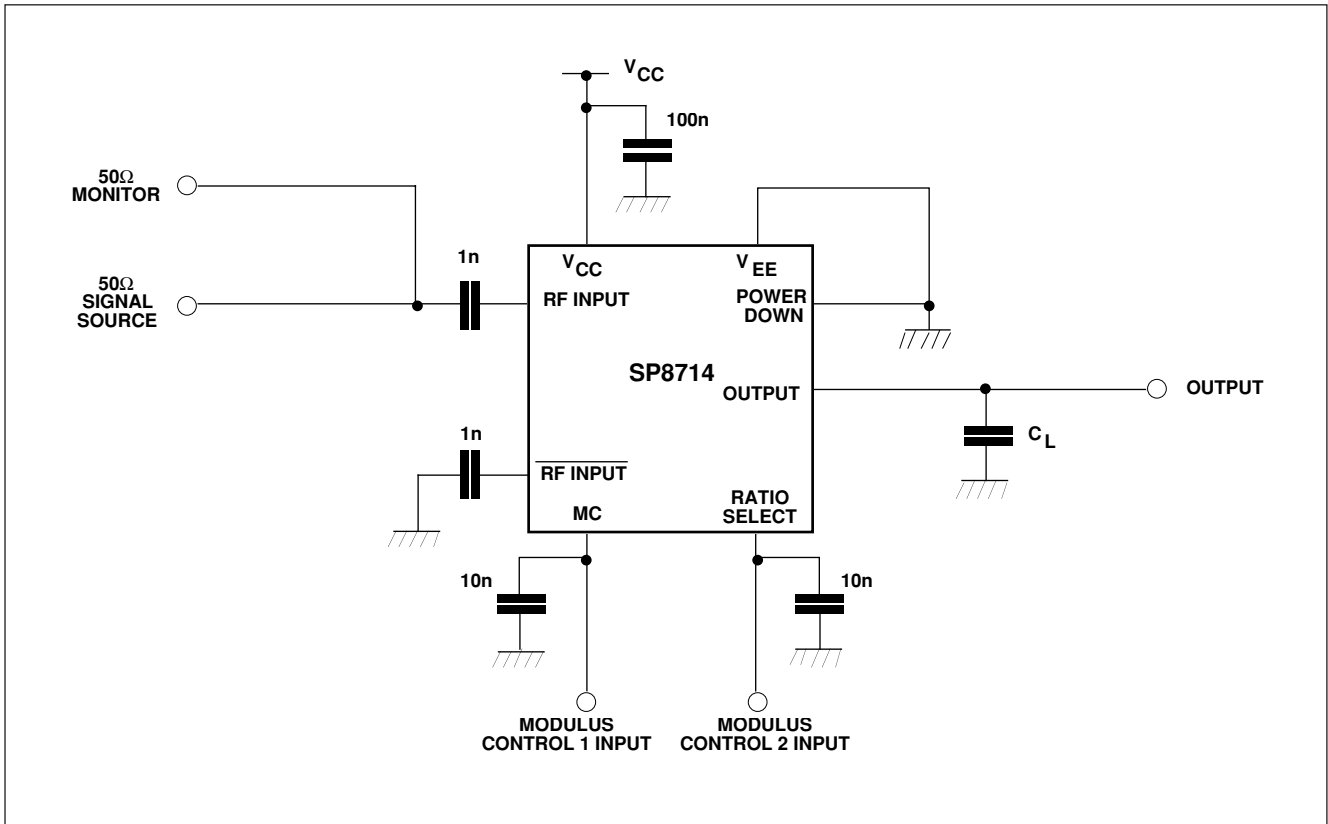


Fig. 5 Toggle frequency test circuit

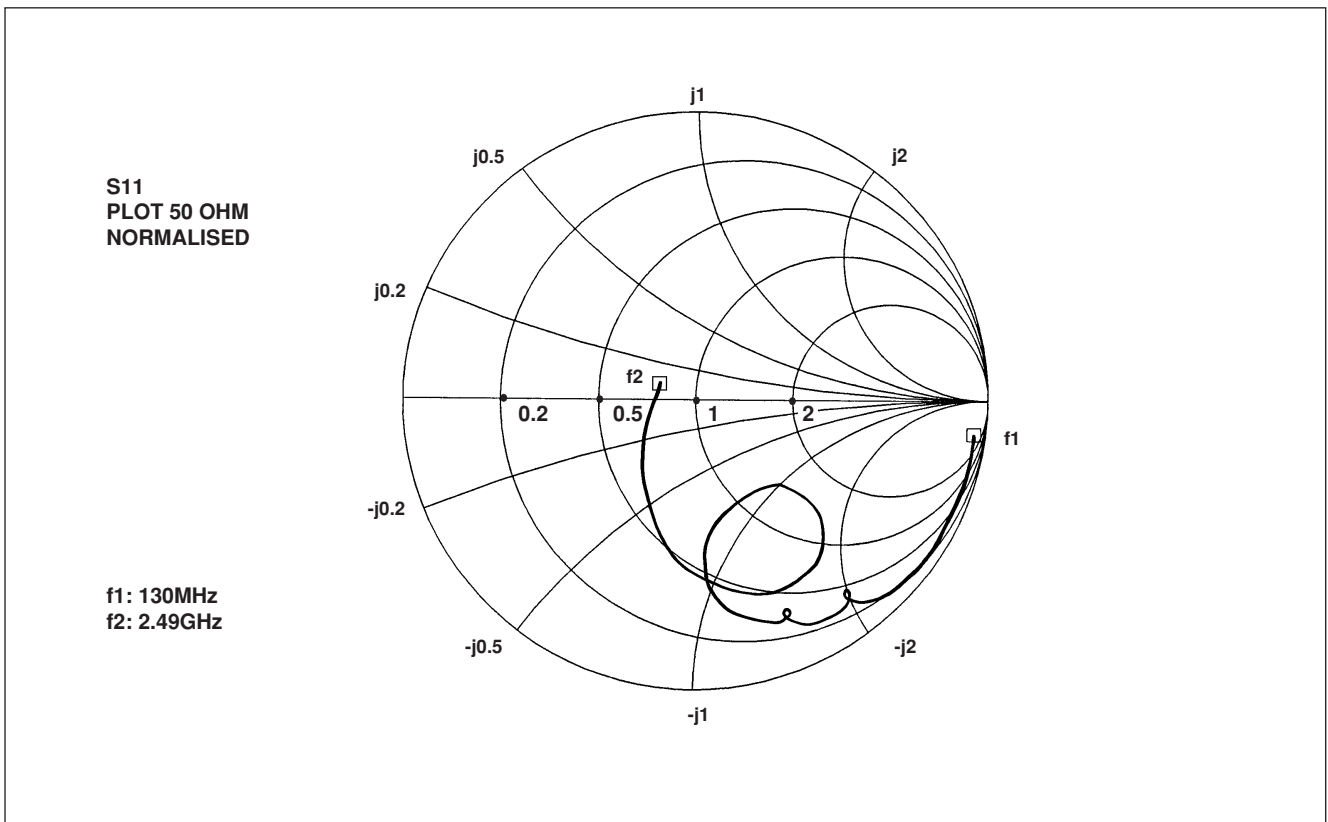


Fig. 6 Typical S11 parameter for pin 1.  $V_{CC} = +5.0V$

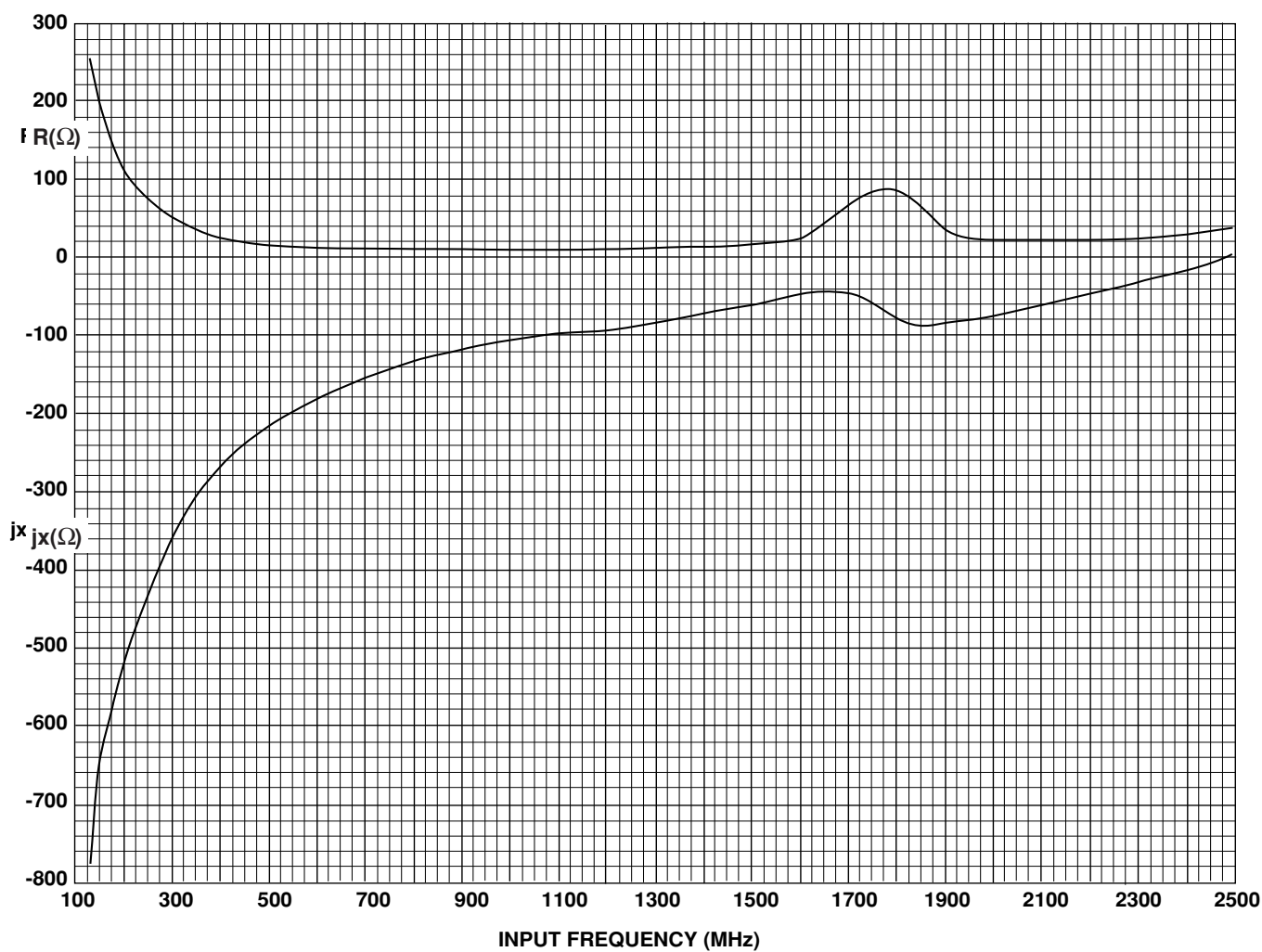


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R ( $\Omega$ )	jx ( $\Omega$ )
130.000	255.068	-733.538
177.200	153.330	-583.339
224.400	88.649	-482.377
271.600	71.050	-411.502
318.800	39.526	-346.620
366.000	38.779	-304.804
413.200	23.809	-269.674
460.400	27.545	-245.161
507.600	22.227	-224.572
554.800	17.767	-203.241
602.000	14.607	-186.545
649.200	13.075	-174.839
596.400	12.583	-160.468
743.600	10.213	-149.642
790.800	11.269	-143.144
838.000	10.509	-132.750
885.200	10.172	-124.495
332.400	10.841	-118.100
979.600	12.260	-109.552
1026.80	14.508	-103.110
1074.00	19.260	-98.149
1121.20	23.285	-99.907
1168.40	18.956	-99.639
1215.60	14.377	-95.033
1262.80	12.711	-89.249
1310.00	12.598	-82.581
1357.20	14.565	-77.212
1404.40	19.164	-71.976
1451.60	15.001	-70.250
1498.80	15.864	-61.898
1546.00	18.993	-53.403
1593.20	26.822	-44.704
1640.40	39.830	-41.522
1687.60	47.875	-43.255
1734.80	63.267	-44.879
1782.00	74.259	-67.801
1829.20	58.878	-86.964
1876.40	42.530	-87.052
1923.60	32.302	-80.484
1970.80	27.333	-73.570
2018.00	24.894	-67.291
2065.20	23.369	-60.620
2112.40	23.577	-54.716
2159.60	23.023	-49.220
2206.80	23.325	-43.340
2254.00	24.623	-37.163
2301.20	26.340	-30.805
2348.40	28.632	-24.040
2395.60	31.161	-17.165
2442.80	34.219	-8.172
2490.00	39.808	-4.368

Table.2 Coefficients for Fig.7

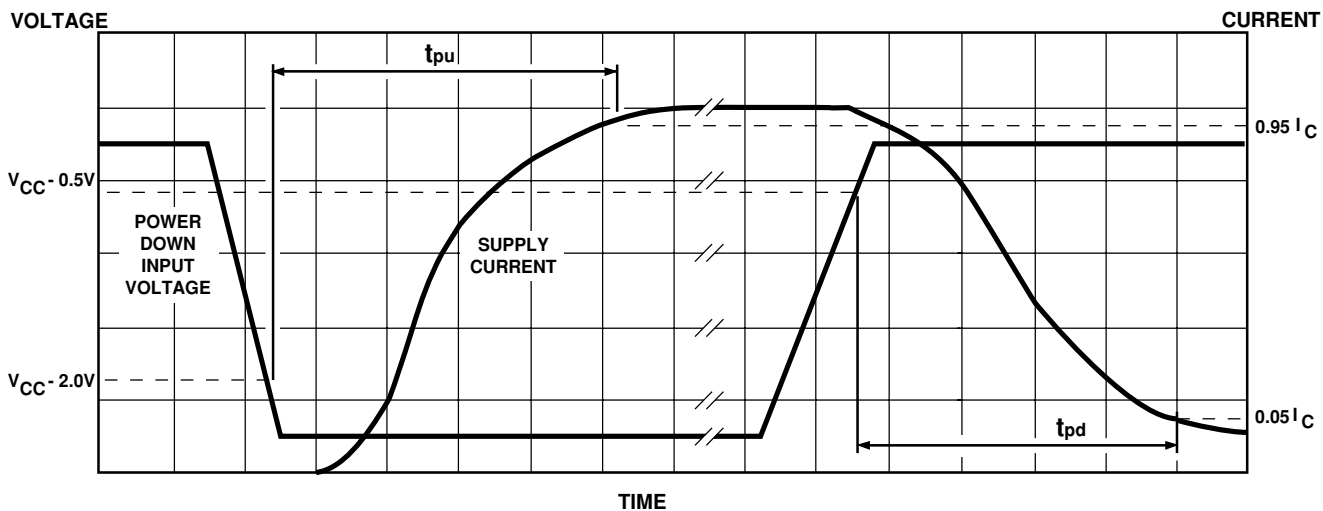


Fig. 8 Power up and power down

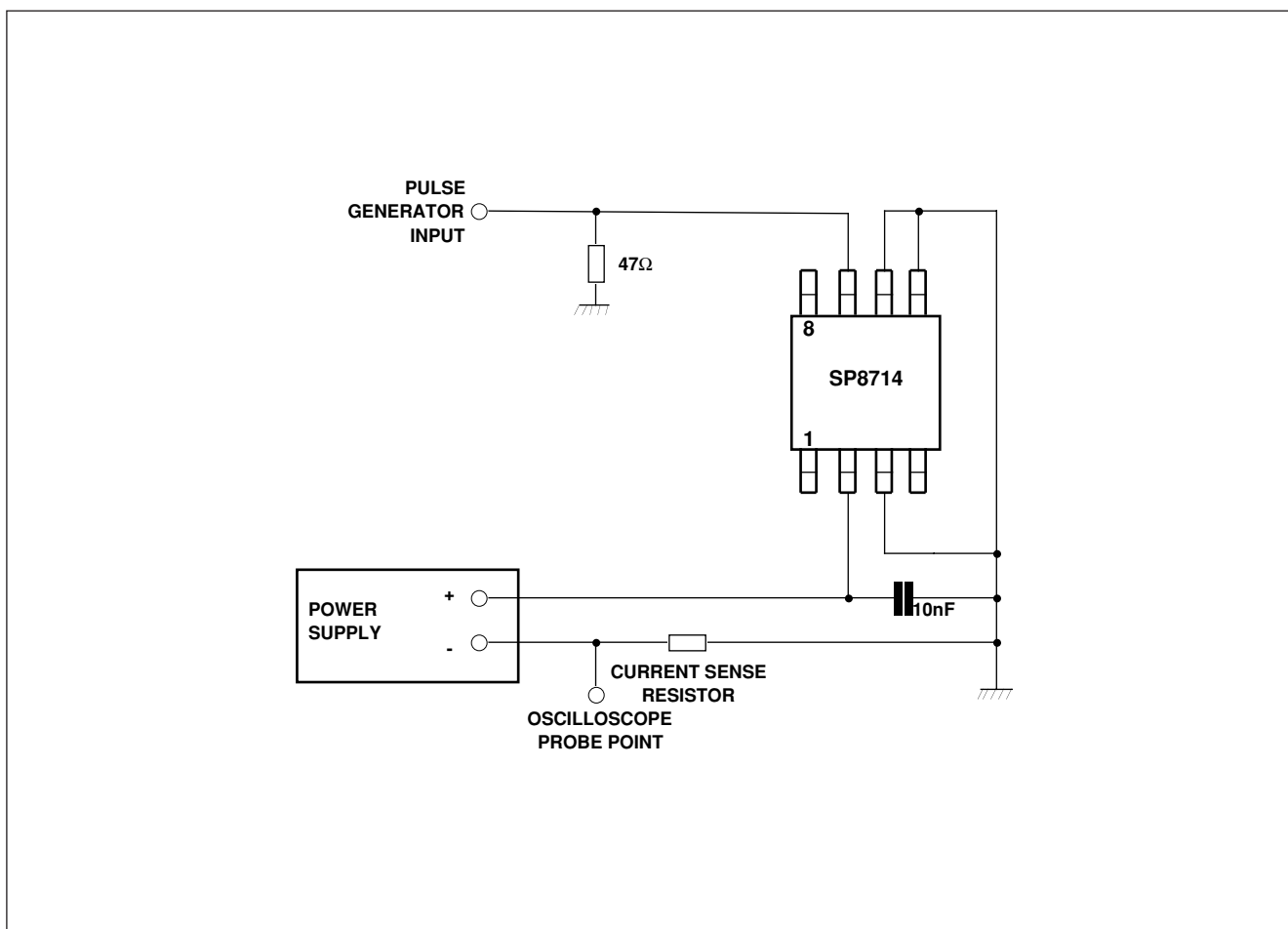
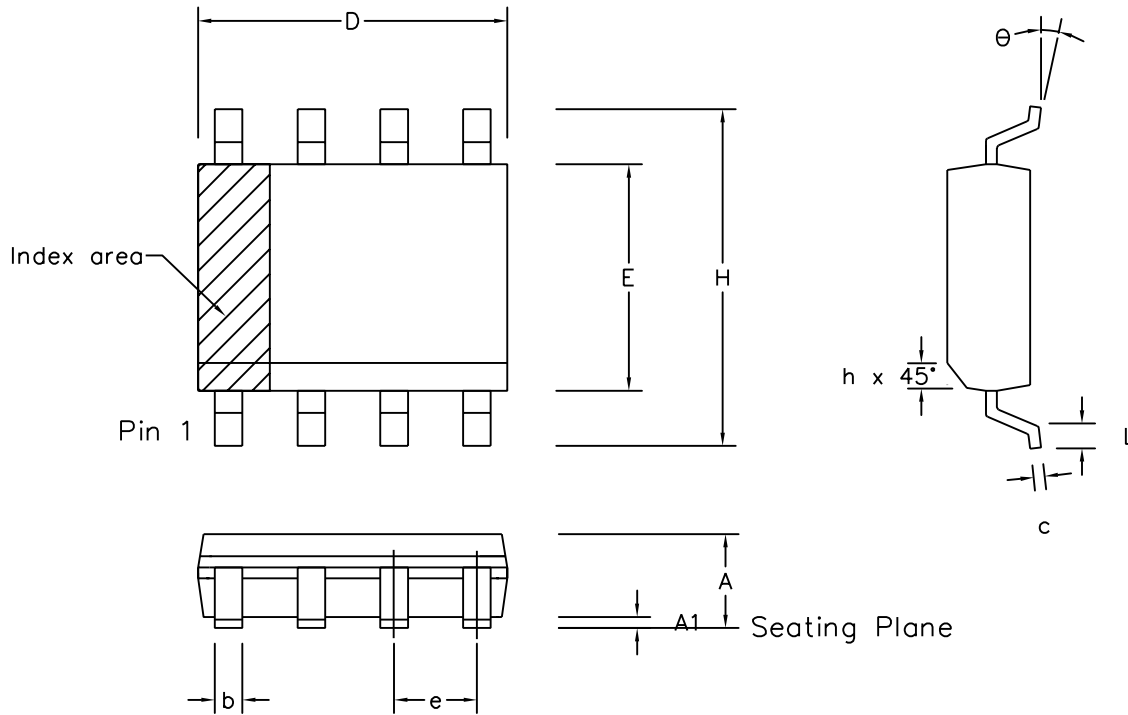


Fig. 9 Power-down time test circuit



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
O	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
Pin Features				
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3	4	5		Previous package codes MP / S	Package Outline for 8 lead SOIC (0.150" Body width)
ACN	6745	201936	202595	203705	212424			
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02			
APPRD.								GPD00010





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