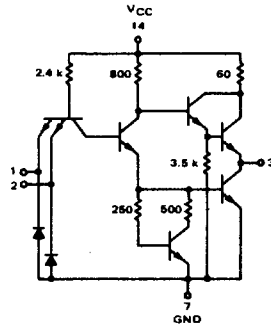


QUAD 2-INPUT "NAND" GATE

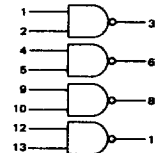
MTTL III MC3100/3000 series

MC3100F • MC3000F
MC3100L • MC3000L,P
 (54H00J) (74H00J,N)

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



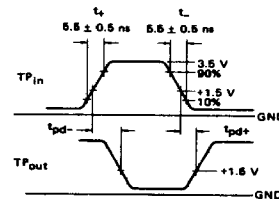
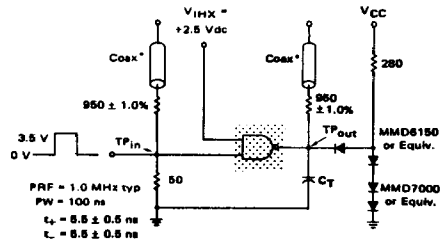
Positive Logic: $3 = \overline{1 \cdot 2}$
 Negative Logic: $3 = \overline{1} \cdot \overline{2}$

Input Loading Factor = 1
 Output Loading Factor = 10

Total Power Dissipation = 88 mW typ/pkg
 Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

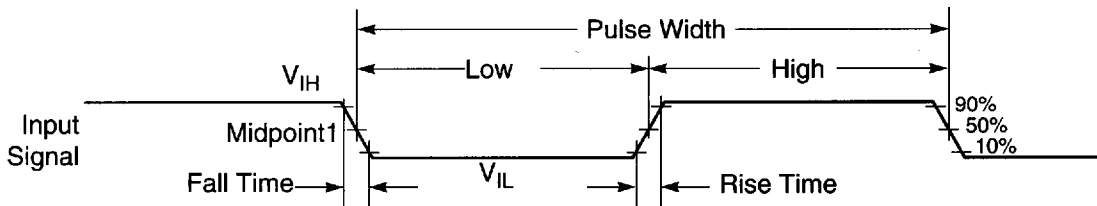
$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

See General Information section for packaging.

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AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference