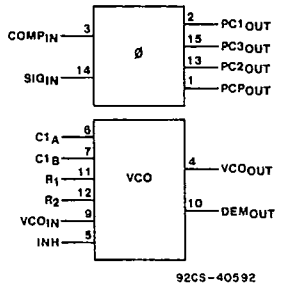
File Number **1854**

Advance Information/
Preliminary Data

CD54/74HC 4046A
CD54/74HCT 4046A

High-Speed CMOS Logic

T-50-17-00



92CS-40592

FUNCTIONAL DIAGRAM

Phase-Locked-Loop with VCO

Features:

- *Operating frequency range of up to 18 MHz (typ.) at V_{CC} = 5 V*
- *Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop*
- *Excellent VCO frequency linearity*
- *VCO-inhibit control for ON/OFF keying and for low standby power consumption*
- *Minimal frequency drift*
- *Operating power supply voltage range: VCO section 3 V to 6 V; digital section 2 V to 6 V*

Applications:

- *FM modulation and demodulation*
- *Frequency synthesis and multiplication*
- *Frequency discrimination*
- *Tone decoding*
- *Data synchronization and conditioning*
- *Voltage-to-frequency conversion*
- *Motor-speed control*

The RCA CD54/74 HC/HCT4046A are high-speed Si-gate CMOS devices that are pin compatible with the CD4046B of the "4000B" series. They are specified in compliance with JEDEC standard no. 7

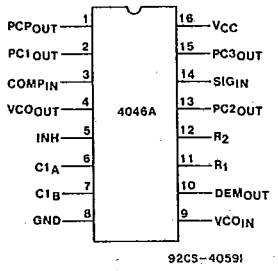
The HC/HCT4046A are phase-locked-loop circuits that contain a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The CD54HC4046A and CD54HCT4046A are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC4046A and CD74HCT4046A are supplied in 16-lead plastic dual-in-line packages (E suffix), and in 16-lead surface mount plastic dual-in-line packages (M suffix). The CD54/74HC/HCT4046A are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range); Standard Outputs - 10 LSTTL Loads Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range: CD74HC/HCT/HCU: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types: 2 to 6 V Operation High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types: 4.5 to 5.5 V Operation Direct LSTTL Input Logic Compatibility V_{IL} = 0.8 V Max., V_{IH} = 2 V Min. CMOS Input Compatibility $I_I \leq 1$ μA @ V_{OL}, V_{OH}*



92CS-40591

TERMINAL ASSIGNMENT

CD54/74HC4046A
CD54/74HCT4046A

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (for -0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ±25 mA
DC V_{CC} OR GOUND CURRENT (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always with the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (for T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4046A
CD54/74HCT4046A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. See logic diagram, Fig. 1.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a guaranteed duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

Phase Comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an Exclusive-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 2. The average of V_{DEM} is equal to 1/2 V_{cc} when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 3.

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CD54/74HCT4046A

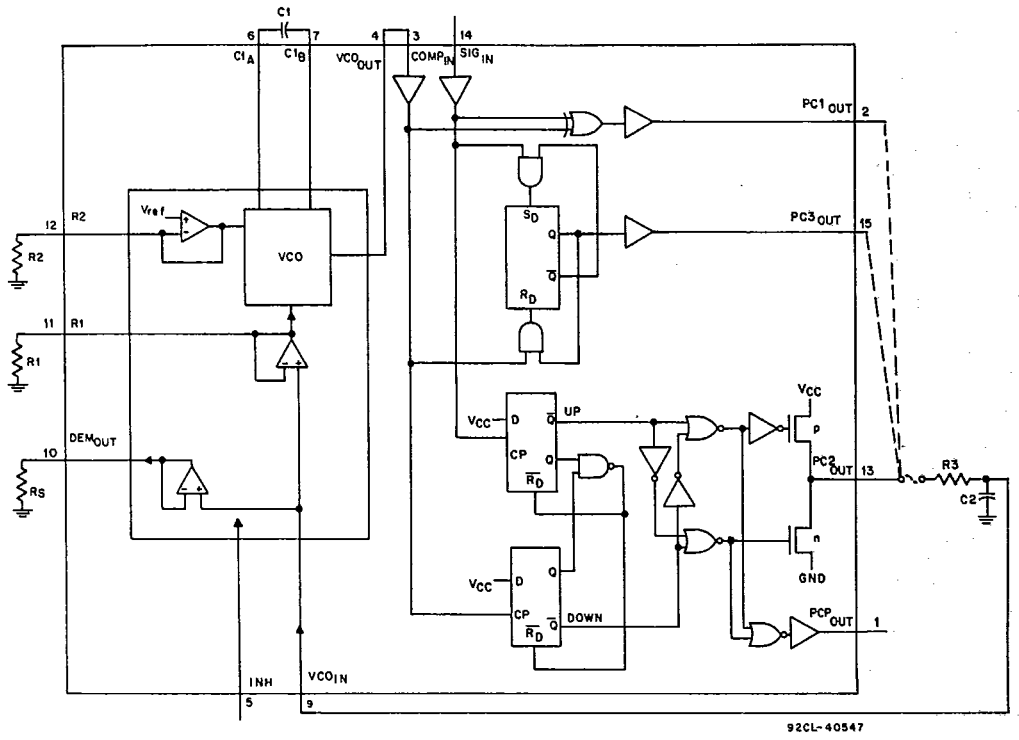

Fig. 1 — Logic diagram.

The frequency capture range ($2f_C$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock behavior even with very noisy input signals. Typical of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.

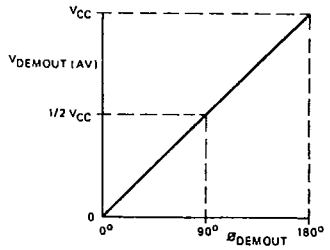

Fig. 2 — Phase comparator 1: average output voltage versus input phase difference:
$V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)(\phi_{SIGIN} - \phi_{COMPIN})$;
$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

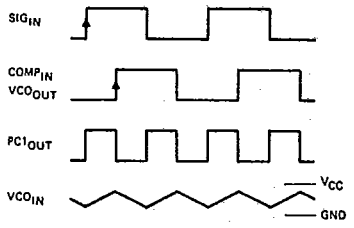

Fig. 3 — Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

CD54/74HC4046A
CD54/74HCT4046A

Phase Comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 1) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMOUNT} = (V_{CC}/4\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10: $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 4. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 5.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n- and p-type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p- and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN}, the VCO adjusts, via PC2, to its lowest frequency.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/2\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 6. Typical waveforms for the PC3 loop locked at f_o are shown in Fig.7.

The phase-to-output response characteristic of PC3 (Fig. 6) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at

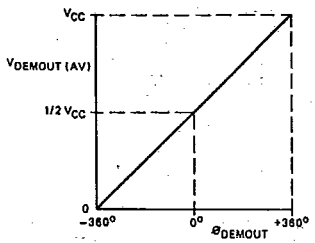

Fig 4 — Phase comparator 2: average output voltage versus input phase difference: $V_{DEMOUT} = V_{PC2OUT} = (V_{CC}/4\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$; $\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

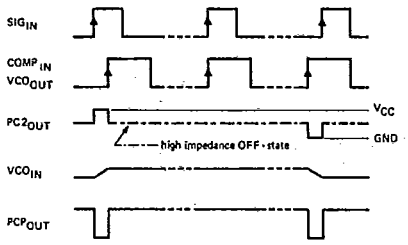

Fig. 5 — Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

the center frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. With no signal present at SIG_{IN}, the VCO adjusts, via PC3, to its highest frequency.

The only difference between the HC and the HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparators' sections are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and the HCT versions.

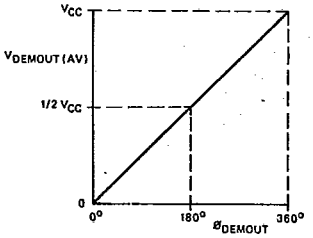

Fig.6 — Phase comparator 3: average output voltage versus input phase difference: $V_{DEMOUT} = V_{PC3OUT} = (V_{CC}/2\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$; $\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

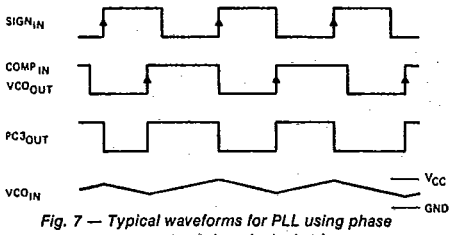

Fig. 7 — Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

CD54/74HC4046A
CD54/74HCT4046A

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4046A/CD54HC4046A										CD74HCT4046A/CD54HCT4046A										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE			
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C			
VCO SECTION	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
INH High-Level Input Voltage V_{IH}			3	2.1	—	—	2.1	—	2.1	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
INH Low-Level Input Voltage V_{IL}			3	—	—	0.9	—	0.9	—	0.9	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
VCO_{OUT} High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	3	2.9	—	—	2.9	—	2.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
VCO_{OUT} Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
C1A, C1B Low Level Output Voltage (Test purposes V_{OL} only)	V_{IL} or V_{IH}	4	4.5	—	—	0.40	—	0.47	—	0.54	V_{IL} or V_{IH}	4.5	—	—	0.40	—	0.47	—	0.54		V
		5.2	6	—	—	0.40	—	0.47	—	0.54	V_{IH}	—	—	—	—	—	—	—	—		
INH VCO_{IN} Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
R1 Range			3	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—		kΩ
			4.5	3	—	300	—	—	—	—		4.5	3	—	300	—	—	—	—		
			6	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—		
R2 Range			3	—	—	—	—	—	—	—			—	—	—	—	—	—	—		kΩ
			4.5	3	—	300	—	—	—	—			3	—	300	—	—	—	—		
			6	—	—	—	—	—	—	—			—	—	—	—	—	—	—		
C1 Capacitance Range			3 4.5 6		0		No LIMIT						0		No LIMIT						pF
VCO_{IN} Operating Voltage Range	Over the range specified for R1 for Linearity See Figs. 8 & 35-38 See Note 2		3	0.9		1.9						4.5	0.9		3.2						V
			4.5	0.9		3.2															
			6	0.9		4.6															

NOTES: 1. The value for R1 & R2 in parallel should exeed 2.7 kΩ.
2. The maximum operating voltage can be as high as V_{CC} -0.9 V, however, this may result in an increased offset voltage.

CD54/74HC4046A
CD54/74HCT4046A

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4046A/CD54HC4046A										CD74HCT4046A/CD54HCT4046A									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
PHASE COMPARATOR SECTION	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level V_{IH} Input Voltage			2	1.5	—	—	1.5	—	1.5	—		4.5								
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—		5.5								
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level V_{IL} Input Voltage			2	—	—	0.5	—	0.5	—	0.5		4.5								
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	V
			6	—	—	1.8	—	1.8	—	1.8		5.5								
PCP_{OUT}, PCn OUT High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
PCP_{OUT}, PCn OUT Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
SIG_{IN}, $COMP_{IN}$ Input Leakage I_I Current	V_{CC} or Gnd		2	—	—	±3	—	±4	—	±5	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±30	—	±38	—	±45	µA
			3	—	—	±7	—	±9	—	±11										
			4.5	—	—	±18	—	±23	—	±29										
			6	—	—	±30	—	±38	—	±45										
PC2 OUT 3-State Off-State Current I_{OZ}	V_{IL} or V_{IH}		6	—	—	±0.5	—	±5	—	±10		5.5	—	—	±0.5	±5	—	—	±10	µA
SIG_{IN}, $COMP_{IN}$ Input Resistance R_I	V_I at Self-Bias Oper. Point; ΔV_I = 0.5 V See Fig. 8		3	—	800	—	—	—	—	—		4.5	—	250	—	—	—	—	—	kΩ
			4.5	—	250	—	—	—	—	—										
			6	—	150	—	—	—	—	—										

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4046A/CD54HC4046A										CD74HCT4046A/CD54HCT4046A									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
DEMODULATOR SECTION	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
Resistor Range R_s	at R_s > 300 kΩ Leakage Current can influence $V_{DEM\ OUT}$		3	50	—	300						4.5	5	—	300					kΩ
			4.5	50	—	300														
			6	50	—	300														
Offset Voltage VCO_{IN} to V_{DEM} V_{OFF}	$V_I = V_{VCO\ IN} = \frac{V_{CC}}{2}$ Values taken over R_S range See Fig. 15		3	—	±30	—						4.5	—	±20	—					mV
			4.5	—	±20	—														
			6	—	±10	—														
Dynamic Output Resistance at DEM_{OUT} R_D	$V_{DEM\ OUT} = \frac{V_{CC}}{2}$		3	—	25	—						4.5	—	25	—					Ω
			4.5	—	25	—														
			6	—	25	—														
Quiescent Device Current I_{CC}	Pins 3, 5 & 14 at V_{CC} Pin 9 at Gnd. I_I at Pins 3 & 14 to be excluded		6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current Per Input Pin 1 unit load ΔI_{CC}*											V_{CC}-2.1 (Excluding Pin 5)	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
INH	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITIONS	V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
PHASE COMPARATOR SECTION															
Propagation Delay, SIG_{IN}, $COMP_{IN}$ to PCI_{OUT} t_{PLH}, t_{PHL}		2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		2	—	300	—	—	—	375	—	—	—	450	—	—	
		4.5	—	60	—	68	—	75	—	85	—	90	—	102	
		6	—	51	—	—	—	64	—	—	—	77	—	—	
SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		2	—	245	—	—	—	305	—	—	—	307	—	—	
		4.5	—	49	—	58	—	61	—	73	—	74	—	87	
		6	—	42	—	—	—	52	—	—	—	63	—	—	
Output Transition Time t_{THL}, t_{TLH}		2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Output Enable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$ t_{PZH}, t_{PZL}		2	—	265	—	—	—	330	—	—	—	400	—	—	
		4.5	—	53	—	60	—	66	—	75	—	80	—	90	
		6	—	45	—	—	—	56	—	—	—	68	—	—	
Output Disable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$ t_{PHZ}, t_{PLZ}		2	—	315	—	—	—	395	—	—	—	475	—	—	
		4.5	—	63	—	68	—	79	—	85	—	95	—	102	
		6	—	54	—	—	—	67	—	—	—	81	—	—	
AC Coupled Input Sensitivity (p-p) at SIG_{IN} or $COMP_{IN}$	V_I (p-p)	3	TYPICAL 11		11										mV
		4.5	15		15										
		6	33		33										
VCO SECTION															
Frequency Stability with Temperature Change $\frac{\Delta f}{\Delta T}$	R_1 = 100kΩ, R_2 = ∞	3					Typ. 0.11		Typ. 0.11						%/°C
		4.5													
		6													
Max. Frequency f_{max}	C_l = 50 pF, R_1 = 3.5kΩ, R_2 = ∞	3													MHz
		4.5	24		24										
		6													
	C_l = 0 pF, R_1 = 9.1kΩ, R_2 = ∞	3													MHz
		4.5	38		38										
		6													
Center Frequency	C_l = 40 pF, R_1 = 3kΩ, R_2 = ∞, $VCO_{IN} = \frac{V_{CC}}{2}$	3													MHz
		4.5	17		17										
		6													
Frequency Linearity, Δf_{VCO}	R_1 = 100kΩ, R_2 = ∞, C_1 = 100 pF	3													%
		4.5	0.4		0.4										
		6													
Offset Frequency	R_2 = 220kΩ, C_1 = 1 nF	3													kHz
		4.5	400		400										
		6													
DEMODULATOR SECTION															
V_{OUT} V_S f_{IN}	R_1 = 100 kΩ, R_2 = ∞, C_1 = 100 pF, R_S = 10 kΩ, R_3 = 100 kΩ, C_2 = 100 pF	3	—		—										mV/kHz
		4.5	330		330										
		6	—		—										

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Figure References for DC Characteristics

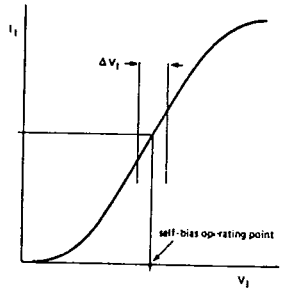

Fig. 8 — Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

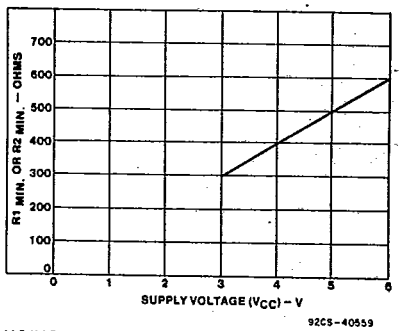

Fig. 9-HC/HCT4046A R1 (min) or R2 (min) vs supply voltage (V_{CC}).

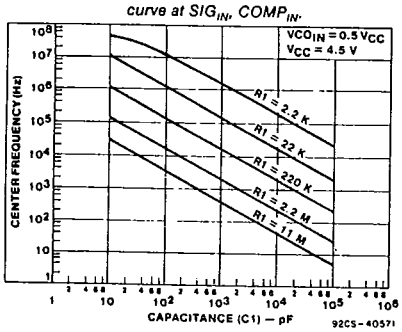

Fig. 10-HCT4046A typical center frequency vs R1, C1 (V_{CC}=4.5 V).

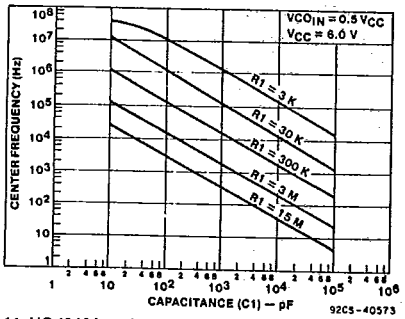

Fig. 11-HC4046A typical center frequency vs R1, C1 (V_{CC}=6 V).

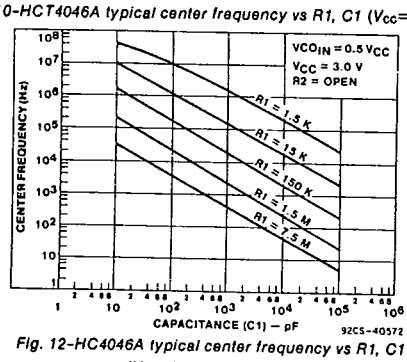

Fig. 12-HC4046A typical center frequency vs R1, C1 (V_{CC}=3 V, R2=open).

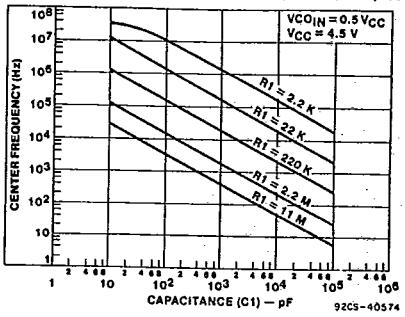

Fig. 13-HCT4046A typical center frequency vs R1, C1 (V_{CC}=4.5 V).

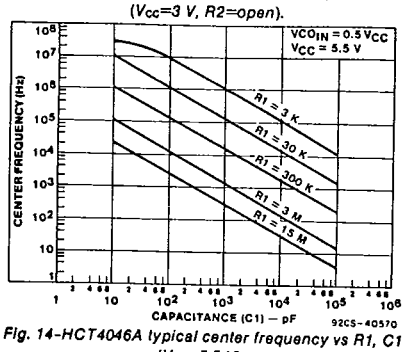

Fig. 14-HCT4046A typical center frequency vs R1, C1 (V_{CC}=5.5 V).

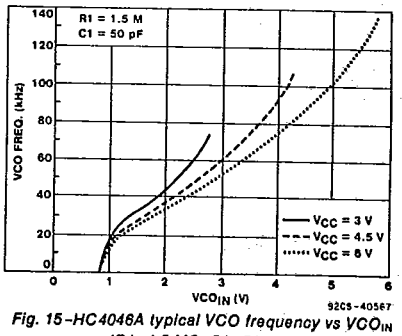

Fig. 15-HC4046A typical VCO frequency vs VCO_{IN} (R1=1.5 MΩ, C1=50 pF).

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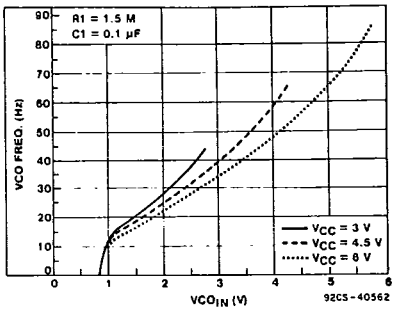

Fig. 16-HC4046A typical VCO frequency vs VCO_{IN} ($R1=1.5\ M\Omega$, $C1=0.1\ \mu F$).

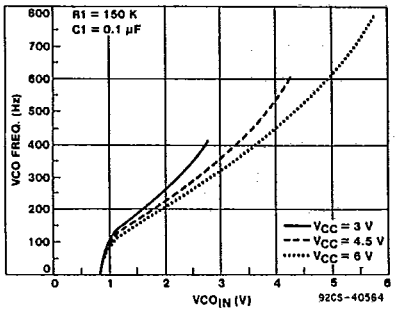

Fig. 17-HC4046A typical VCO frequency vs VCO_{IN} ($R1=150\ k\Omega$, $C1=0.1\ \mu F$).

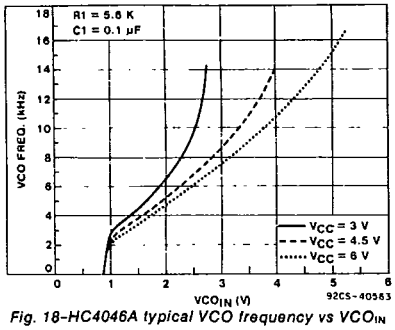

Fig. 18-HC4046A typical VCO frequency vs VCO_{IN} ($R1=5.6\ k\Omega$, $C1=0.1\ \mu F$).

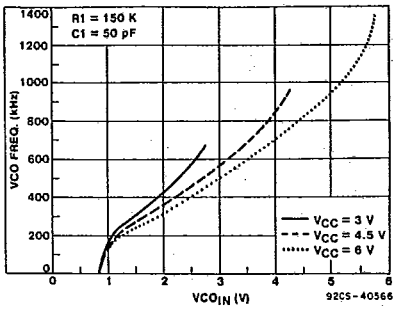

Fig. 19-HC4046A typical VCO frequency vs VCO_{IN} ($R1=150\ k\Omega$, $C1=50\ pF$).

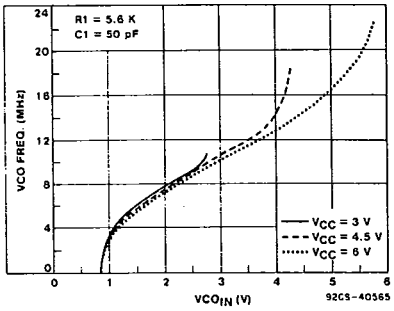

Fig. 20-HC4046A typical VCO frequency vs VCO_{IN} ($R1=5.6\ k\Omega$, $C1=50\ pF$).

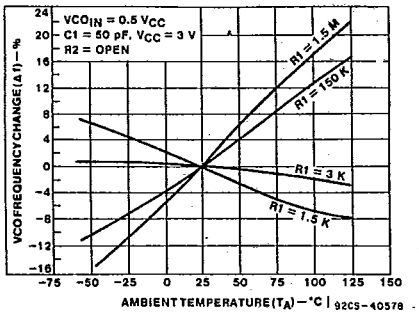

Fig. 21-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 ($V_{CC}=3\ V$).

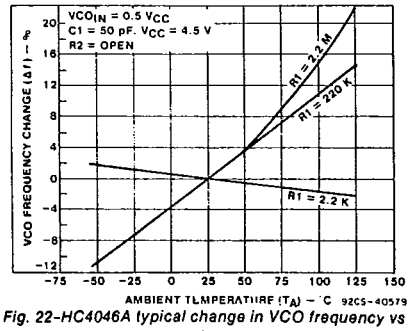

Fig. 22-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 ($V_{CC}=4.5\ V$).

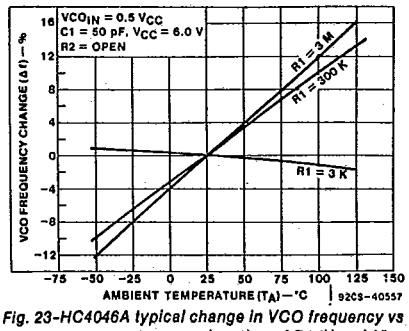

Fig. 23-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 ($V_{CC}=6\ V$).

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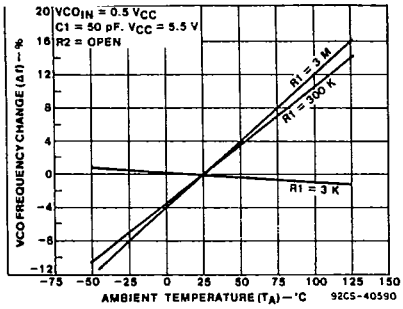

Fig. 24-HCT4046A typical change in VCO frequency vs ambient temperature as a function of R1.

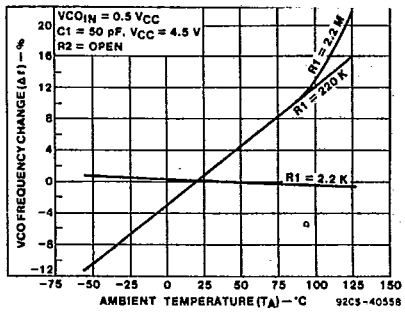

Fig. 25-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 (V_{CC}=4.5 V).

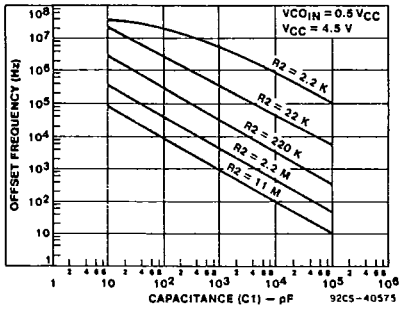

Fig. 26-HC4046A offset frequency vs R2, C1 (V_{CC}=4.5 V).

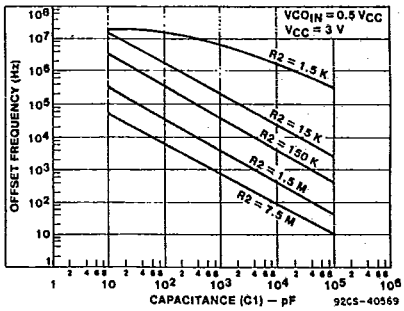

Fig. 27-HC4046A offset frequency vs R2, C1 (V_{CC}=3 V).

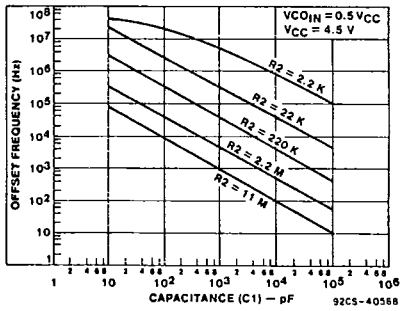

Fig. 28-HCT4046A offset frequency vs R2, C1 (V_{CC}=4.5 V).

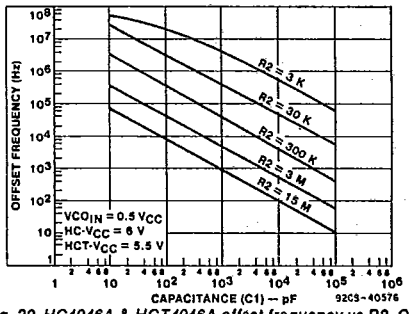

Fig. 29-HC4046A & HCT4046A offset frequency vs R2, C1 (V_{CC}=6 V, V_{CC}=5.5 V).

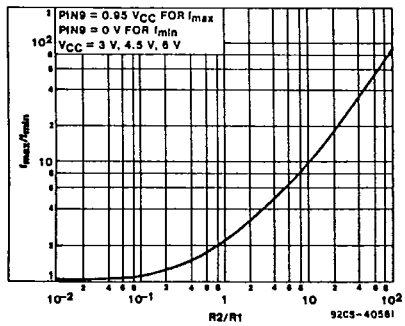

Fig. 30-HC4046A f_{max}/f_{min} vs R2/R1 (V_{CC}=3 V, 4.5 V, 6 V).

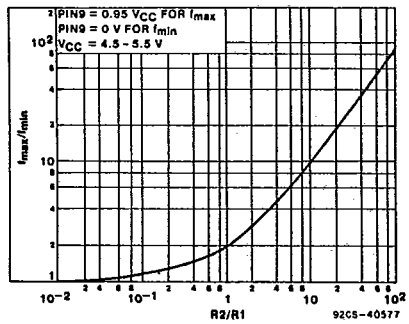

Fig. 31-HCT4046A f_{max}/f_{min} vs R2/R1 (V_{CC}=4.5 V-5.5 V).

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CD54/74HCT4046A

AC WAVEFORMS

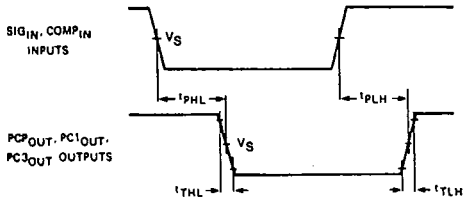


Fig. 32 — Waveforms showing input (SIG$_{IN}$ COMP$_{IN}$) to output (PCP$_{OUT}$, PC1$_{OUT}$, PC3$_{OUT}$) propagation delays and the output transition times.

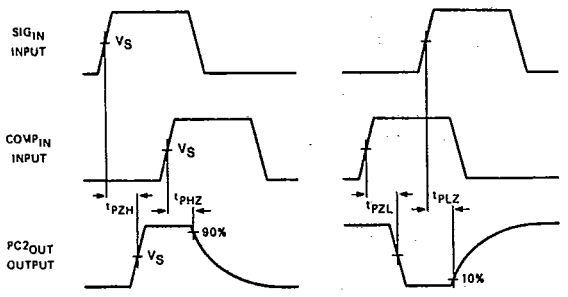
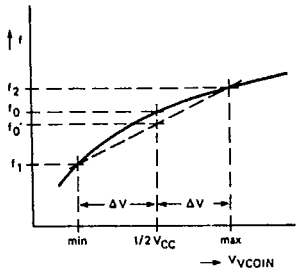


Fig. 33 — Waveforms showing the 3-state enable and disable times for PC2$_{OUT}$.

	HC	HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V



$\Delta V = 0.5$ V over the V_{CC} range:

for VCO linearity

$$f'_O = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_O - f_O}{f'_O} \times 100\%$$

Fig. 34 — Definition of VCO frequency linearity.

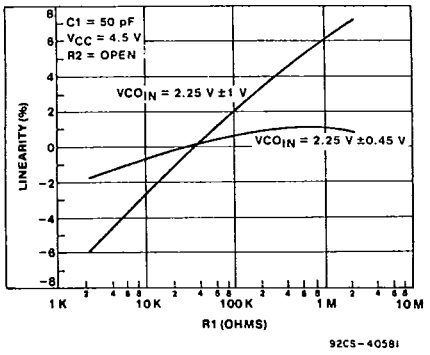


Fig. 35-HC4046A VCO linearity vs R1 (V_{CC}=4.5 V).

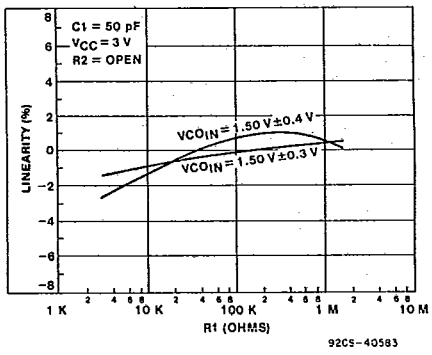


Fig. 36-HC4046A VCO linearity vs R1 (V_{CC}=3 V).

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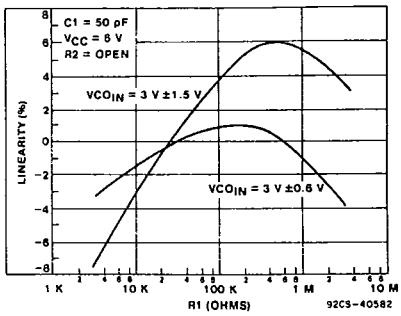

Fig. 37-HC4046A VCO linearity vs R1 (V_{CC}=6 V).

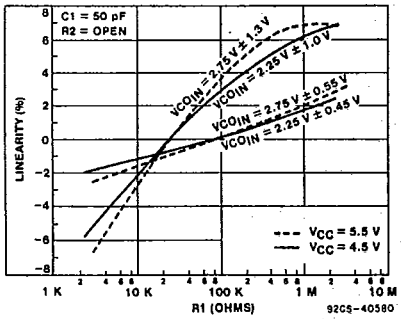

Fig. 38-HCT4046A VCO linearity vs R1 (V_{CC}=4.5 V, V_{CC}=5.5 V).

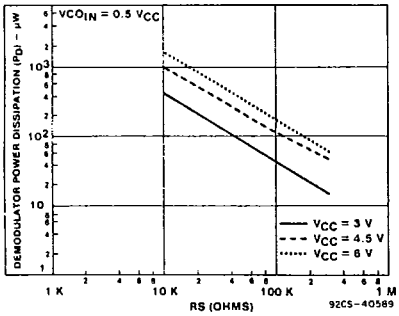

Fig. 39-HC4046A demodulator power dissipation vs RS (typ.) (V_{CC}=3 V; 4.5 V; 6 V).

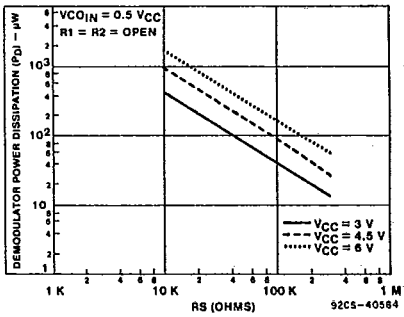

Fig. 40-HCT4046A demodulator power dissipation vs RS (typ.) (V_{CC}=3 V; 4.5 V; 6 V).

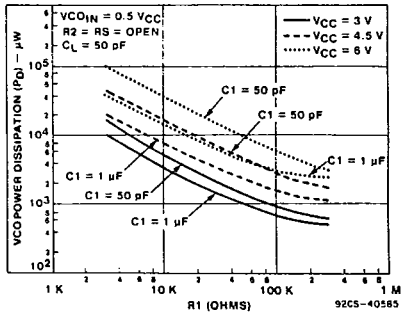

Fig. 41-HC4046A VCO power dissipation vs R1 (C1=50 pF; 1 µF).

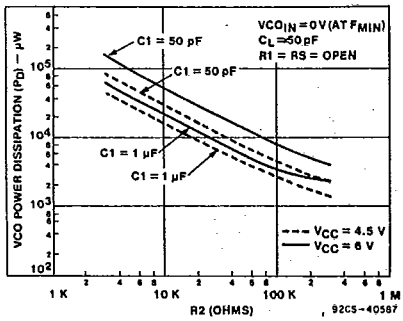

Fig. 42-HCT4046A VCO power dissipation vs R2 (C1=50 pF; 1 µF).

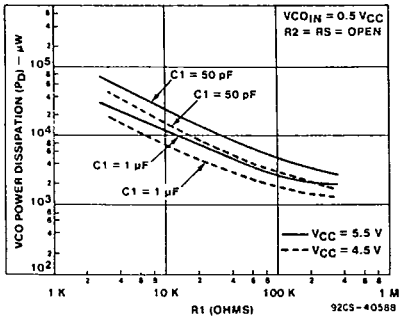

Fig. 43-HCT4046A VCO power dissipation vs R1 (C1=50 pF; 1 µF).

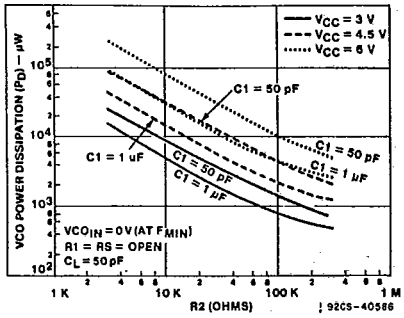

Fig. 44-HC4046A VCO power dissipation vs R2 (C1=50 pF, 1 µF).

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CHIP SECTION	HC	HCT	UNIT
COMPARATOR 1	48	50	pF
COMPARATORS 2 & 3	39	48	
VCO	61	53	

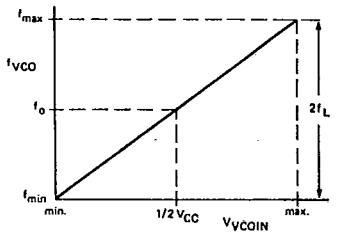
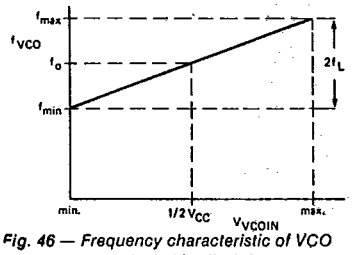
APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

References should be made to Figs.10 through 14 as indicated in the table.

Values of the selected components should be within the following ranges.

R1 between 3 kΩ and 300 kΩ;
R2 between 3 kΩ and 300 kΩ;
R1 + R2 parallel value > 2.7 kΩ;
C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2 or PC3	**VCO Frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Figs. 10-14. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  *Fig. 45— Frequency characteristic of VCO operating without offset: f_o = center frequency: $2f_L$ = frequency lock range.*
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Figs. 10-14.
	PC2 or PC3	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 30. Use Fig. 31 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ, < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Figs. 26-29.  *Fig. 46 — Frequency characteristic of VCO operating with offset: f_o = center frequency; $2f_L$ = frequency lock range.*

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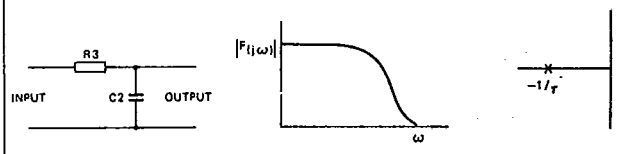
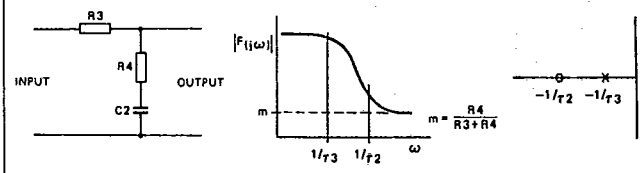
APPLICATION INFORMATION (Cont'd.)

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency with offset (continued)	PC1, PC2 or PC3	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Figs. 26-29. Calculate f_{off} from equation $f_{off} = f_{CO} = f_L$. Obtain the values of C1 and R2 by using Figs. 26-29. Calculate the value of R1 from the value of C1 and the product R1C1.
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with $\phi_{DEMOUT} = 90°$ and $V_{VCOIN} = 1/2\ V_{CC}$ (see Fig. 2).
	PC2	VCO adjusts to f_o with $\phi_{DEMOUT} = -360°$ and $V_{VCOIN} = 0$ V (see Fig. 4).
	PC3	VCO adjusts to f_o with $\phi_{DEMOUT} = +360°$ and $V_{VCOIN} = V_{CC}$ (see Fig. 6).
PLL Frequency capture range	PC1, PC2 or PC3	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $\tau > 2f_c' \approx 1/\pi\ (2\pi f_L/\tau_1)^{1/2}$ *Fig. 47 — Simple loop filter for PLL without offset.*  (a) τ_1 = R3 x C2; (b) amplitude characteristic (c) pole-zero diagram τ_2 = R4 x C2; τ_3 = (R3 + R4) x C2 *Fig. 48 - Simple loop filter for PLL with offset.*

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL locks on harmonics at center frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at $\phi_{DEMOUT} = 90°$
	PC2	$f_r = f_i$, small ripple content at $\phi_{DEMOUT} = 0°$
	PC3	$f_r = f_{SIG_{IN}}$, large ripple content at $\phi_{DEMOUT} = 180°$