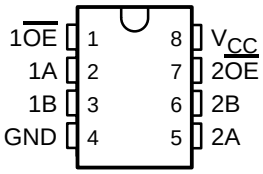
- **Low and Flat On-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typical)**
- **0- to 5-V Rail-to-Rail Switching on Data I/O Ports**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **TTL- and LVTTL-Compatible Data I/O Ports**
- **LVTTL-Compatible Control Inputs**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C_{io} = 3.5 pF Typical)**
- **Fast Switching Speeds ($f_{\overline{OE}}$ = 20 MHz Max)**
- **High-Bandwidth Data Path (Up To 533 MHz)**
- **Low Power Consumption (I_{CC} = 250 μA Typical)**
- **I_{off} on A and B Port for Partial-Power-Down Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Hot Plug, Hot Docking, Memory Interleaving, Bus Isolation, and Low-Distortion Signal Gating**

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

Texas Instruments bus switches provide high-performance, low-power replacements for standard bus-interface devices when signal buffering (current drive) is not required. The CB3Q family of high-bandwidth bus switches offers low and flat on-state resistance (r_{on}), 0- to 5-V rail-to-rail switching on the data input/output (I/O) ports, and low data I/O capacitance (C_{io}) to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the CB3Q family provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3306 is a dual FET bus switch featuring independent line switches. Each switch is enabled when the associated output-enable ($\overline{OE}$) input is low, allowing bidirectional data flow between ports A and B. Each switch is disabled when the associated $\overline{OE}$ input is high, producing a high-impedance state between ports A and B. The very low r_{on} of the switch allows connections to be made with minimal propagation delay.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube	SN74CB3Q3306D	BU306
		Tape and reel	SN74CB3Q3306DR	
	TSSOP – PW	Tape and reel	SN74CB3Q3306PWR	BU306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

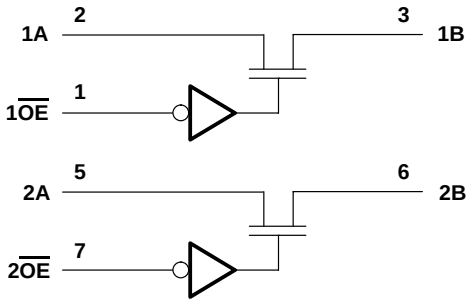
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 97°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 5.5 V or GND				±1	µA
I_{OZ}‡		V_{CC} = 3.6 V,	$V_{I/O}$ = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	$V_{I/O}$ = 0 to 5.5 V				±1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	V_{IN} = V_{CC} or GND		250	700	µA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			25	µA
I_{CCD}¶		V_{CC} = 3.6 V, A and B pins open, Per $\overline{OE}$ control input switching at 50% duty cycle				0.03	0.1	mA/ MHz
C_{in}	Control inputs	V_{IN} = 5.5 V, 3.3 V, or 0,	V_{CC} = 3.3 V			2.5	3.5	pF
$C_{io(OFF)}$		$V_{I/O}$ = 5.5 V, 3.3 V, or 0,	V_{CC} = 3.3 V,	Switch off, $\overline{OE}$ = V_{CC}		3.5	5	pF
$C_{io(ON)}$		$V_{I/O}$ = 5.5 V, 3.3 V, or 0,	V_{CC} = 3.3 V,	Switch on, $\overline{OE}$ = GND		8	10.5	pF
r_{on}#		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	8	Ω
			V_I = 1.7 V,	I_O = –15 mA		5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4	6	
			V_I = 2.4 V,	I_O = –15 mA		5	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single $\overline{OE}$ control input. The total I_{CC} can be calculated with the following formula: Total I_{CC} = I_{CC} + (I_{CCD} × 1$\overline{OE}$ frequency) + (I_{CCD} × 2$\overline{OE}$ frequency).
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$‖	$\overline{OE}$	A or B		10		20	MHz
t_{pd}☆	A or B	B or A		0.2		0.2	ns
t_{en}	$\overline{OE}$	A or B	1.5	6.5	1.5	5.5	ns
t_{dis}	$\overline{OE}$	A or B	1	6	1	5	ns

‖ Maximum toggle frequency for $\overline{OE}$ control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0)
☆ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

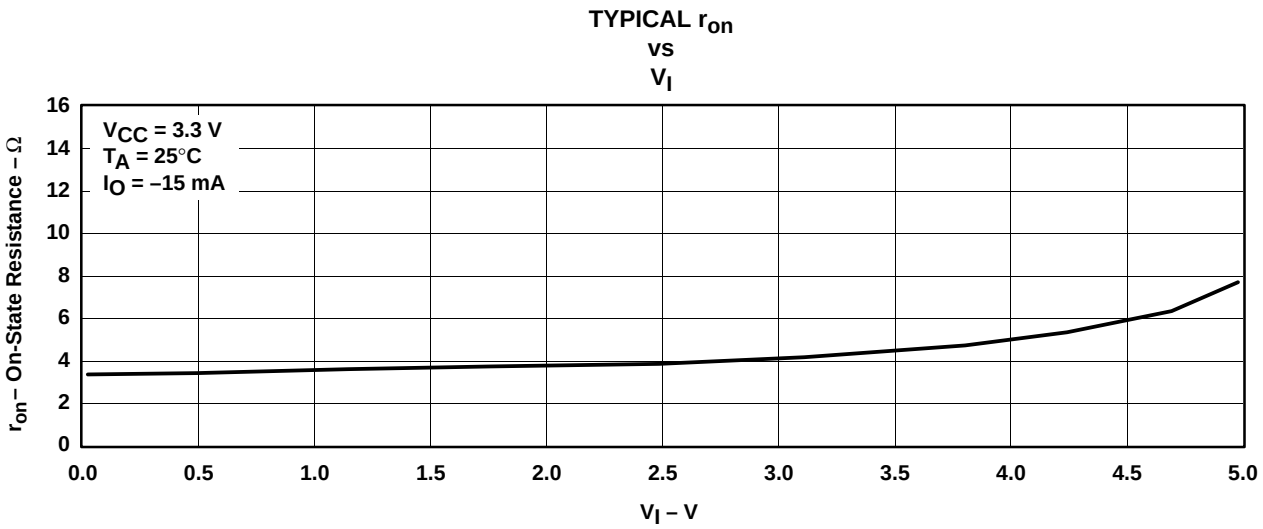


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = –15 mA

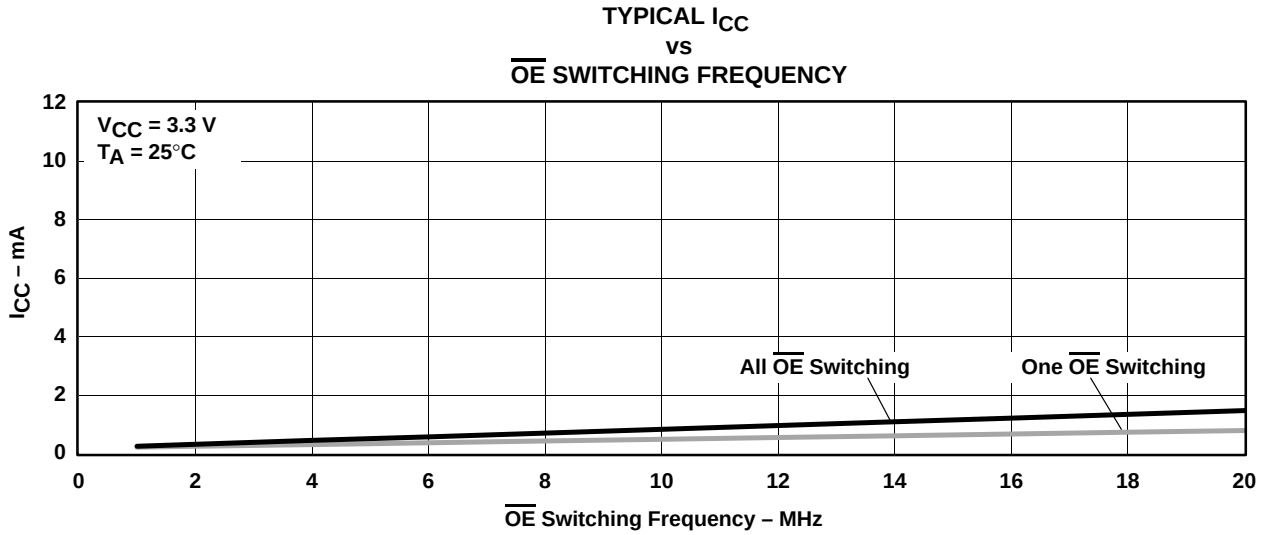
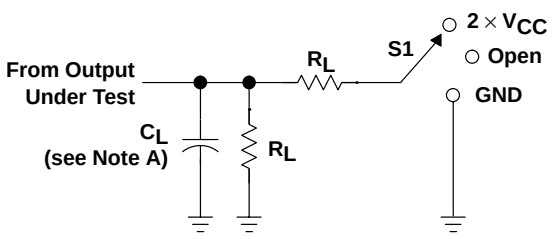


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

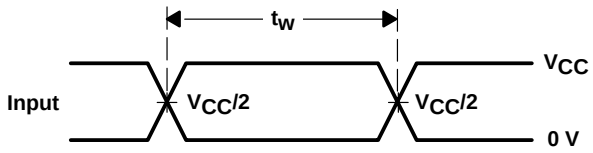
PARAMETER MEASUREMENT INFORMATION



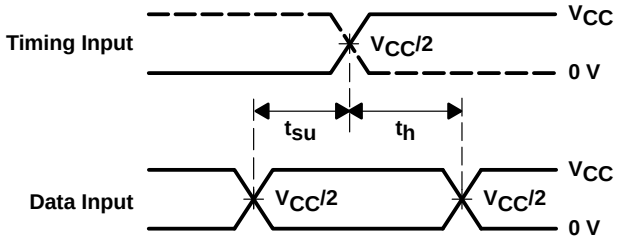
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

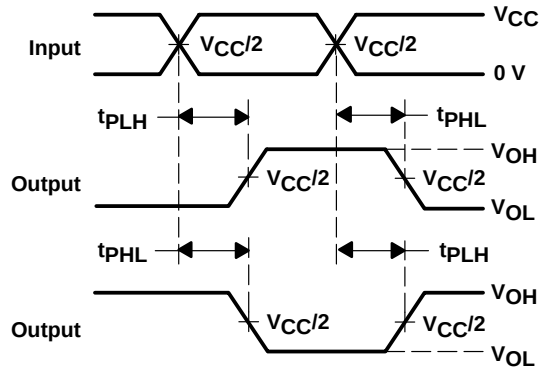
V_{CC}	C_L	R_L	V_Δ
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	50 pF	500 Ω	0.3 V



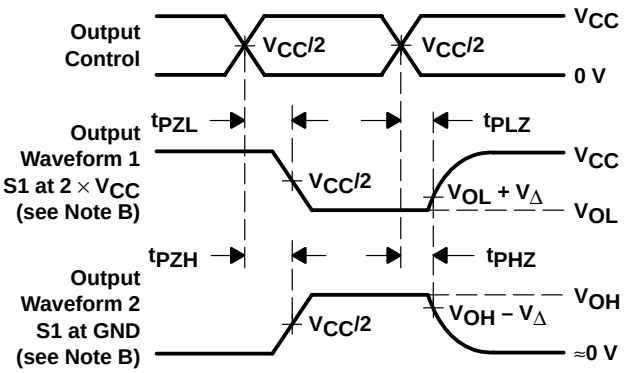
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

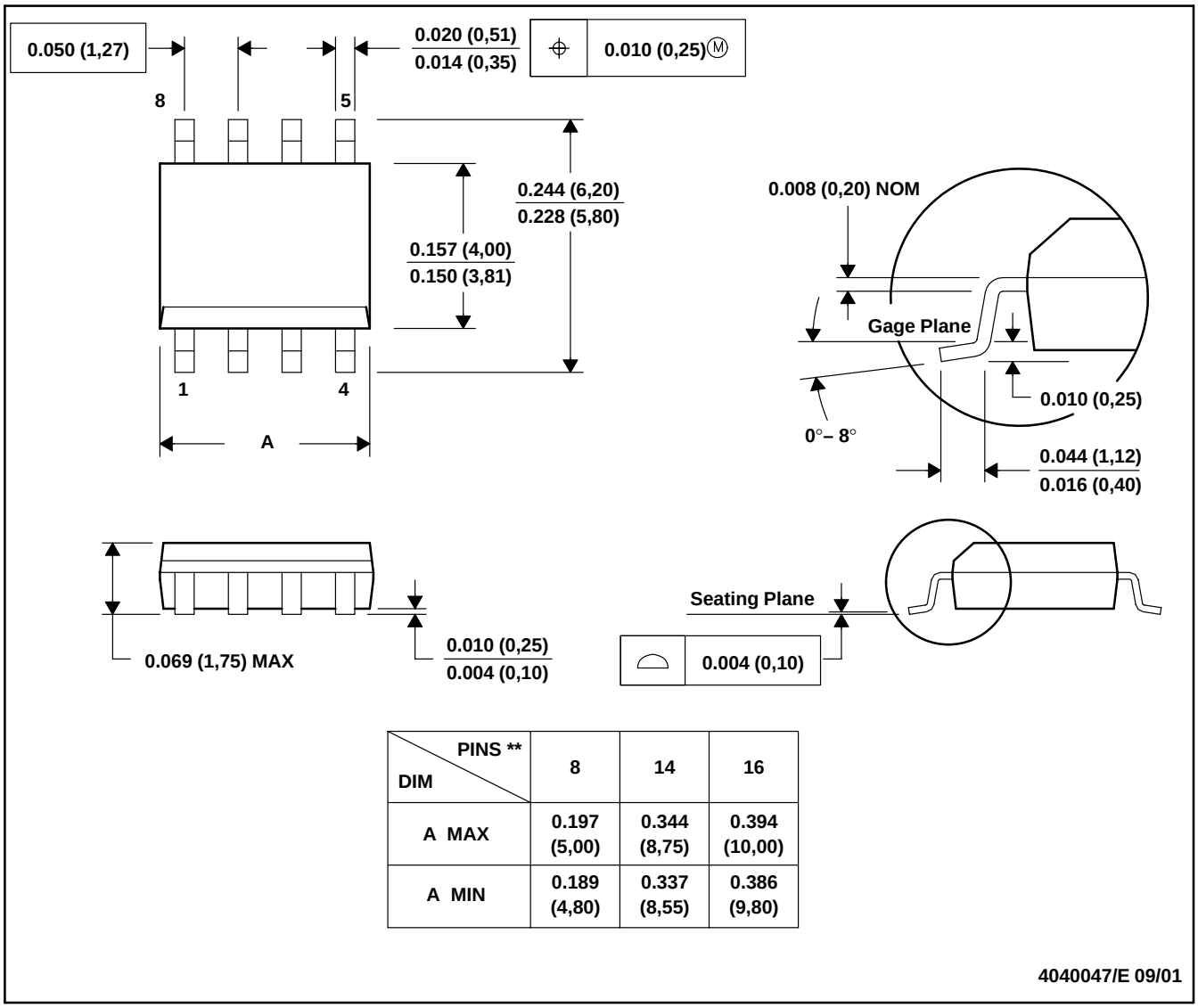
Figure 3. Load Circuit and Voltage Waveforms

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



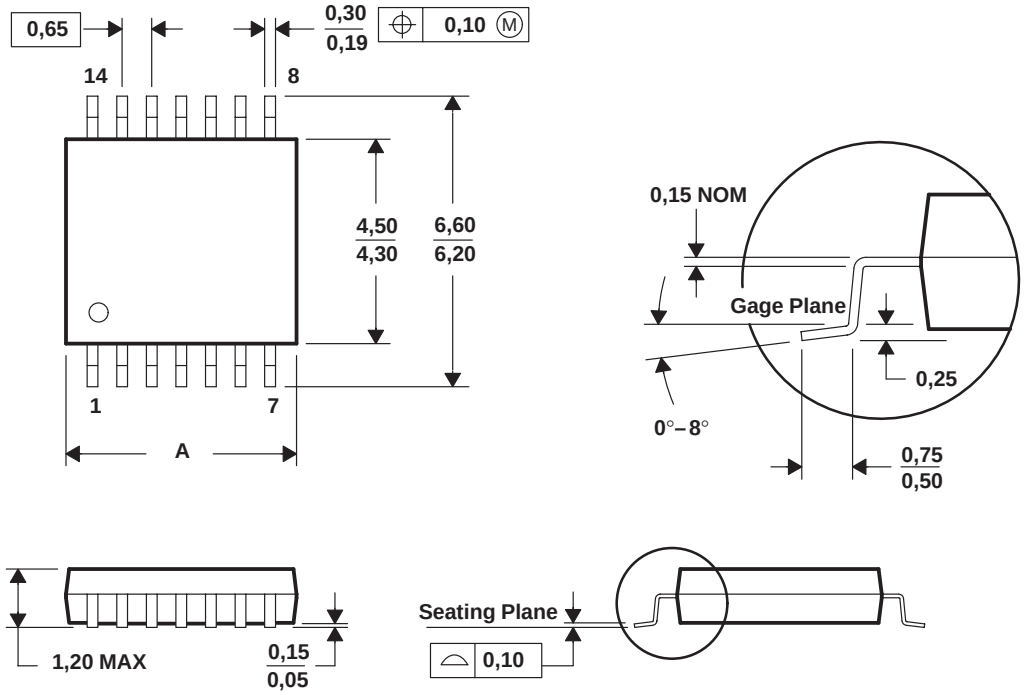
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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