## Features

- QuadPort™ datapath switching element (DSE) family allows four independent ports of access for data path management and switching

- High-bandwidth data throughput up to 10 Gb/s

- 133-MHz[1] port speed x 18-bit-wide interface × 4 ports

- High-speed clock to data access 4.2 ns (maximum)

- Synchronous pipelined device
  - 1 Mb (64K × 18) switch array

- 0.25-micron CMOS for optimum speed/power

- IEEE 1149.1 JTAG boundary scan

- Width and depth expansion capabilities

- BIST (Built-In Self-Test) controller

- Dual Chip Enables on all ports for easy depth expansion

- Separate upper-byte and lower-byte controls on all ports

- Simple array partitioning
  - Internal mask register controls counter wrap-around
  - Counter-Interrupt flags to indicate wrap-around
  - Counter and mask registers readback on address

- 272-ball BGA package (27-mm × 27-mm × 2.33-mm ball pitch)

- Industrial temperature ranges

- 3.3 V low operating power
  - Active = 750 mA (maximum)
  - Standby = 15 mA (maximum)

## Functional Description

The Quadport Datapath Switching Element (DSE) family offers four ports that may be clocked at independent frequencies from one another. Each port can read or write up to 133 MHz[1], giving the device up to 10 Gb/s of data throughput. The device is 1-Mb (64 K × 18) in density. Simultaneous reads are allowed to access the same address location; however, simultaneous read and write to the same address location is not allowed. Any port can write to a certain location while other ports are reading that location simultaneously, if the timing spec for port to port delay ($t_{CCS}$) is met. The result of writing to the same location by more than one port at the same time is undefined.

Data is registered for decreased cycle time. Clock to data valid $t_{CD2}$ = 4.2 ns. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address the counter will self-increment the address internally (more details to follow). The internal write pulse width is independent of the duration of the R/W input signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE_0}$ or LOW on $CE_1$ for one clock cycle will power down the internal circuitry to reduce the static power consumption. One cycle is required with chip enables asserted to reactivate the outputs.

The CY7C0430CV (64 K × 18 device) supports burst contains for simple array partitioning. Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with an external address when the port's Counter Load pin (CNTLD) is asserted LOW. When the port's Counter Increment pin (CNTINC) is asserted, the address counter will increment on each subsequent LOW-to- HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until CNTINC is deasserted. The counter can address the entire switch array and will loop back to the start. Counter Reset (CNTRST) is used to reset the burst counter. A counter-mask register is used to control the counter wrap. The counter and mask register operations are described in more details in the following sections.
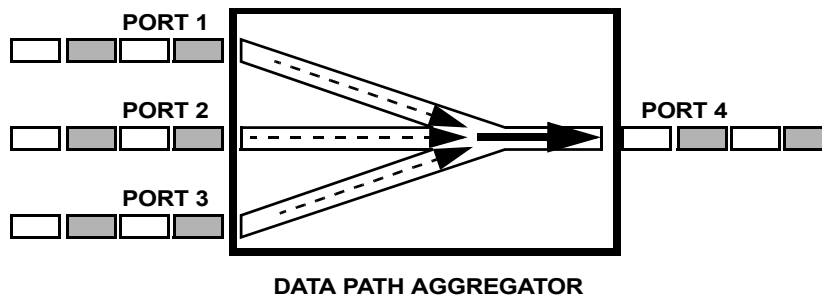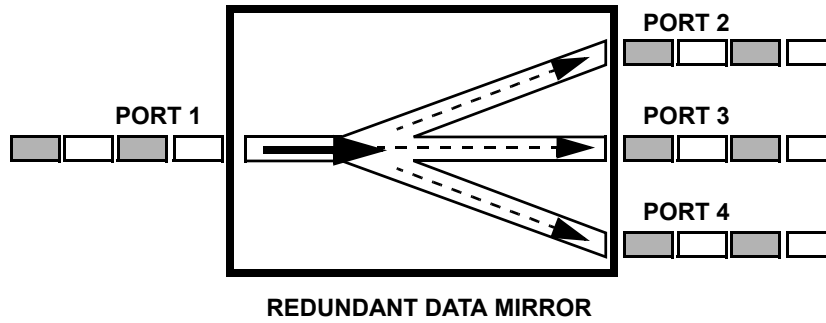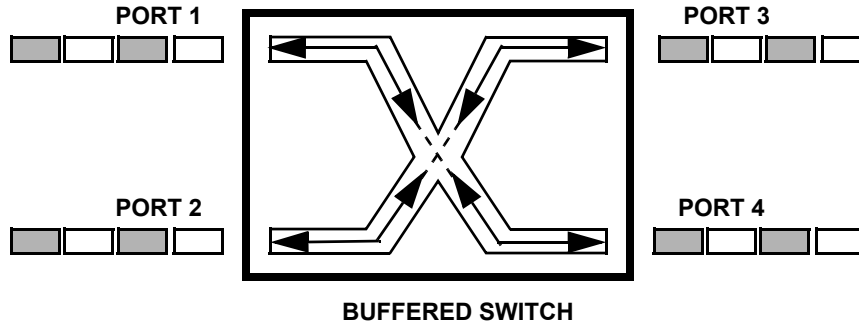
The counter or mask register values can be read back on the bidirectional address lines by activating MKRD or CNTRD, respectively.
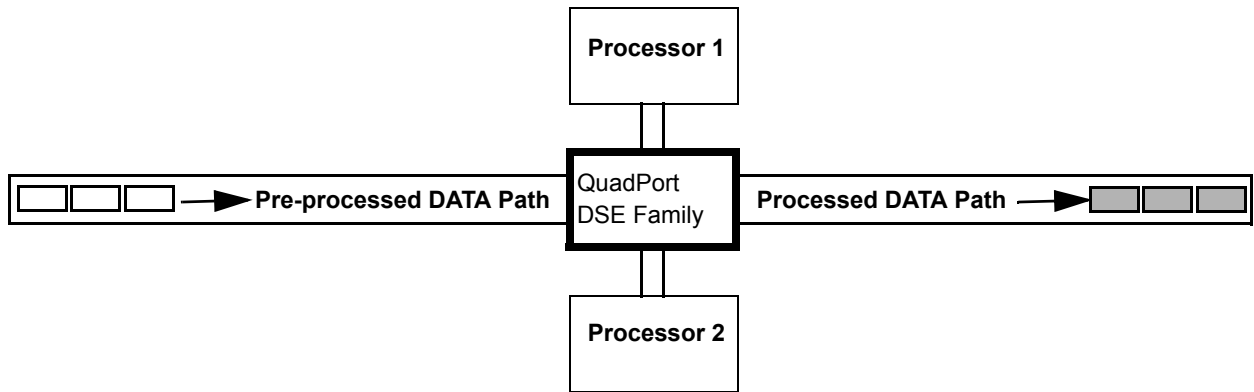
The new features included for the QuadPort DSE family include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around, readback of mask register value on address lines, interrupt flags for message passing, BIST, JTAG for boundary scan, and asynchronous Master Reset.

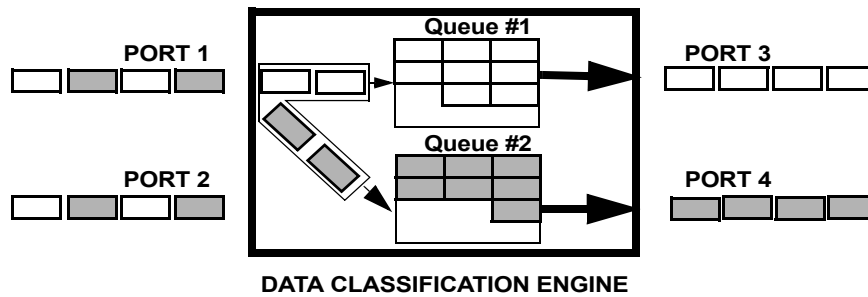**Cypress Semiconductor Corporation**   •   198 Champion Court   •   San Jose, CA 95134-1709   •   408-943-2600
Document Number: 38-06027 Rev. *F

Revised July 31, 2013

## QuadPort DSE Family Applications

**PORT 1**

**PORT 3**

**PORT 2**

**PORT 4**

**BUFFERED SWITCH**

**PORT 2**

**PORT 1**

**PORT 3**

**PORT 4**

**REDUNDANT DATA MIRROR**

**PORT 1**

**PORT 2**

**PORT 4**

**PORT 3**

**DATA PATH AGGREGATOR**

**DATA PATH MANAGER FOR
PARALLEL PACKET PROCESSING**



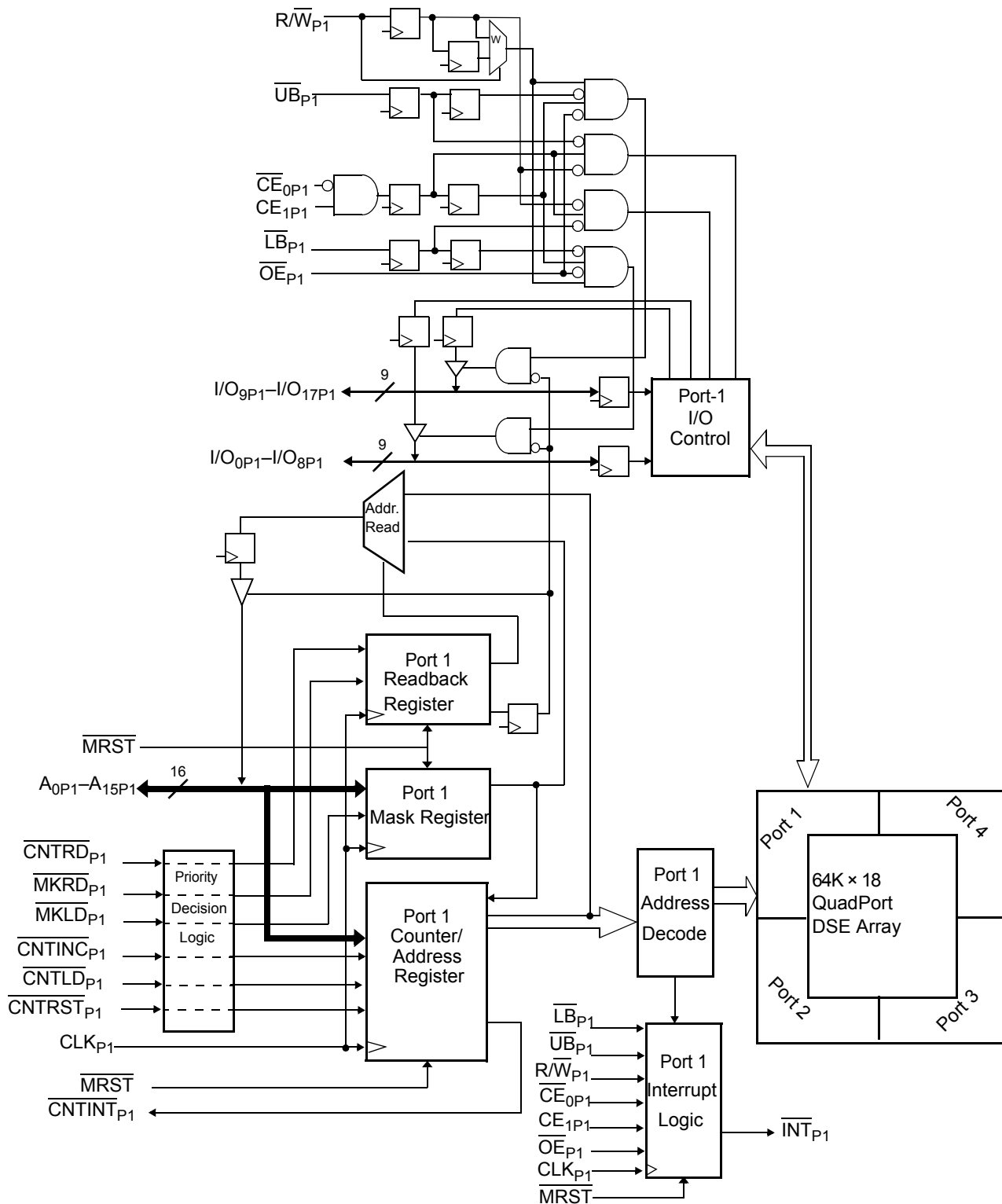**DATA CLASSIFICATION ENGINE**

## Top Level Logic Block Diagram
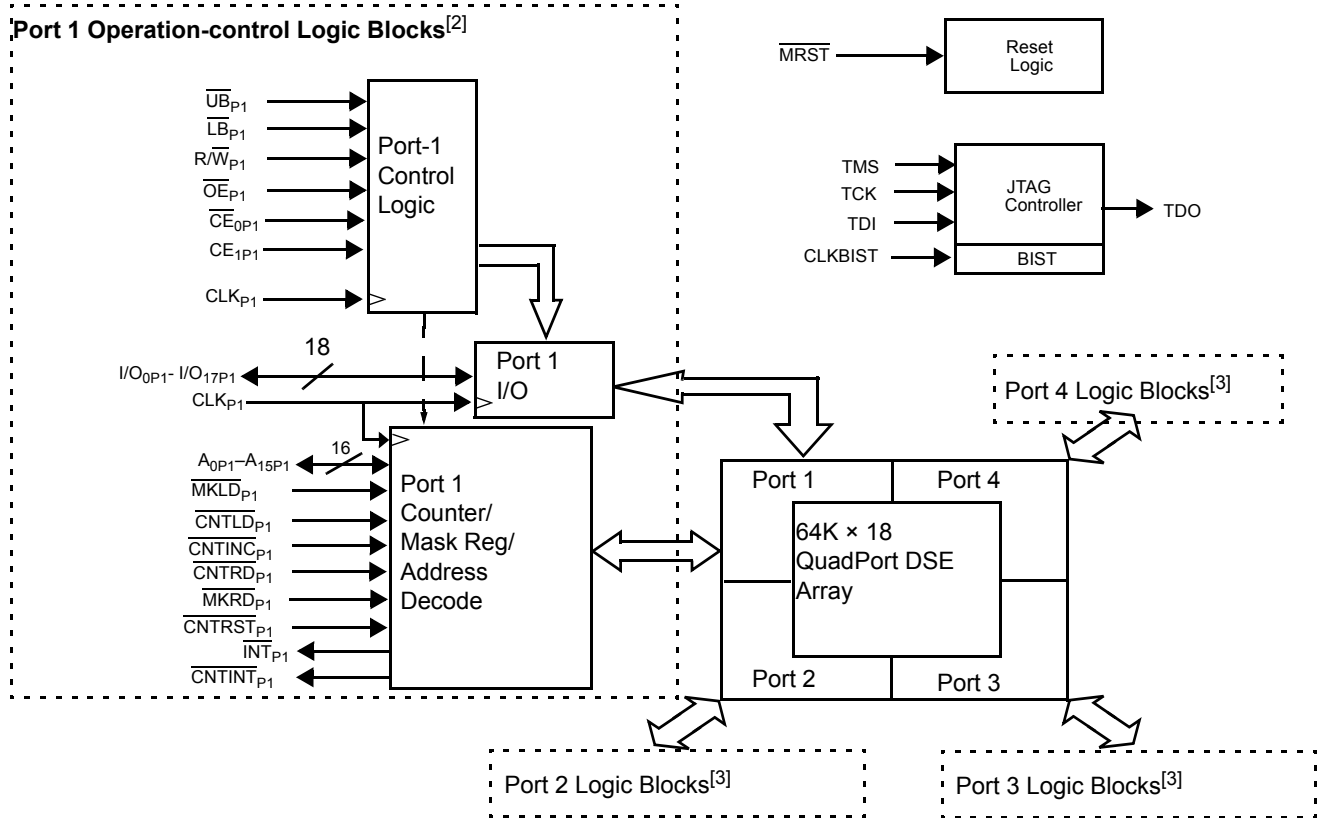


**Notes**
2. Port 1 Control Logic Block is detailed on page 4.
3. Port 2, Port 3, and Port 4 Logic Blocks are similar to Port 1 Logic Blocks.

## Port 1 Operation Control Logic Block Diagram

(Address Readback is independent of CEs)

# Contents

## Pin Configuration

**Figure 1.  272-Ball BGA pinout (Top View)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{LB}$ P1 | I/O17 P2 | I/O15 P2 | I/O13 P2 | I/O11 P2 | I/O9 P2 | I/O16 P1 | I/O14 P1 | I/O12 P1 | I/O10 P1 | I/O10 P4 | I/O12 P4 | I/O14 P4 | I/O16 P4 | I/O9 P3 | I/O11 P3 | I/O13 P3 | I/O15 P3 | I/O17 P3 | $\overline{LB}$ P4 |
| **B** | VDD1 | $\overline{UB}$ P1 | I/O16 P2 | I/O14 P2 | I/O12 P2 | I/O10 P2 | I/O17 P1 | I/O13 P1 | I/O11 P1 | TMS | TDI | I/O11 P4 | I/O13 P4 | I/O17 P4 | I/O10 P3 | I/O12 P3 | I/O14 P3 | I/O16 P3 | $\overline{UB}$ P4 | VDD1 |
| **C** | A14 P1 | A15 P1 | CE1 P1 | $\overline{CE0}$ P1 | R/$\overline{W}$ P1 | I/O15 P1 | VSS2 | VSS2 | I/O9 P1 | TCK | TDO | I/O9 P4 | VSS2 | VSS2 | I/O15 P4 | R/$\overline{W}$ P4 | $\overline{CE0}$ P4 | CE1 P4 | A15 P4 | A14 P4 |
| **D** | VSS1 | A12 P1 | A13 P1 | $\overline{OE}$ P1 | VDD2 | VSS2 | VSS2 | VDD2 | VDD | VSS | VSS | VDD | VDD2 | VSS2 | VSS2 | VDD2 | $\overline{OE}$ P4 | A13 P4 | A12 P4 | VSS1 |
| **E** | A10 P1 | A11 P1 | $\overline{MKRD}$ P1 | $\overline{CNTRD}$ P1 | | | | | | | | | | | | | $\overline{CNTRD}$ P4 | $\overline{MKRD}$ P4 | A11 P4 | A10 P4 |
| **F** | A7 P1 | A8 P1 | A9 P1 | $\overline{CNTINT}$ P1 | | | | | | | | | | | | | $\overline{CNTINT}$ P4 | A9 P4 | A8 P4 | A7 P4 |
| **G** | VSS1 | A5 P1 | A6 P1 | $\overline{CNTINC}$ P1 | | | | | | | | | | | | | $\overline{CNTINC}$ P4 | A6 P4 | A5 P4 | VSS1 |
| **H** | A3 P1 | A4 P1 | $\overline{MKLD}$ P1 | $\overline{CNTLD}$ P1 | | | | | | | | | | | | | $\overline{CNTLD}$ P4 | $\overline{MKLD}$ P4 | A4 P4 | A3 P4 |
| **J** | VDD1 | A1 P1 | A2 P1 | VDD | | | | | GND[4] | GND[4] | GND[4] | GND[4] | | | | | VDD | A2 P4 | A1 P4 | VDD1 |
| **K** | A0 P1 | $\overline{INT}$ P1 | $\overline{CNTRST}$ P1 | CLK P1 | | | | | GND[4] | GND[4] | GND[4] | GND[4] | | | | | CLK P4 | $\overline{CNTRST}$ P4 | $\overline{INT}$ P4 | A0 P4 |
| **L** | A0 P2 | $\overline{INT}$ P2 | $\overline{CNTRST}$ P2 | VSS | | | | | GND[4] | GND[4] | GND[4] | GND[4] | | | | | VSS | $\overline{CNTRST}$ P3 | $\overline{INT}$ P3 | A0 P3 |
| **M** | VDD1 | A1 P2 | A2 P2 | CLK P2 | | | | | GND[4] | GND[4] | GND[4] | GND[4] | | | | | CLK P3 | A2 P3 | A1 P3 | VDD1 |
| **N** | A3 P2 | A4 P2 | $\overline{MKLD}$ P2 | $\overline{CNTLD}$ P2 | | | | | | | | | | | | | $\overline{CNTLD}$ P3 | $\overline{MKLD}$ P3 | A4 P3 | A3 P3 |
| **P** | VSS1 | A5 P2 | A6 P2 | $\overline{CNTINC}$ P2 | | | | | | | | | | | | | $\overline{CNTINC}$ P3 | A6 P3 | A5 P3 | VSS1 |
| **R** | A7 P2 | A8 P2 | A9 P2 | $\overline{CNTINT}$ P2 | | | | | | | | | | | | | $\overline{CNTINT}$ P3 | A9 P3 | A8 P3 | A7 P3 |
| **T** | A10 P2 | A11 P2 | $\overline{MKRD}$ P2 | $\overline{CNTRD}$ P2 | | | | | | | | | | | | | $\overline{CNTRD}$ P3 | $\overline{MKRD}$ P3 | A11 P3 | A10 P3 |
| **U** | VSS1 | A12 P2 | A13 P2 | $\overline{OE}$ P2 | VDD2 | VSS2 | VSS2 | VDD2 | VDD | VSS | VSS | VDD | VDD2 | VSS2 | VSS2 | VDD2 | $\overline{OE}$ P3 | A13 P3 | A12 P3 | VSS1 |
| **V** | A14 P2 | A15 P2 | CE1 P2 | $\overline{CE0}$ P2 | R/$\overline{W}$ P2 | I/O6 P2 | VSS2 | VSS2 | I/O0 P2 | NC | NC | I/O0 P3 | VSS2 | VSS2 | I/O6 P3 | R/$\overline{W}$ P3 | $\overline{CE0}$ P3 | CE1 P3 | A15 P3 | A14 P3 |
| **W** | VDD1 | $\overline{UB}$ P2 | I/O7 P1 | I/O5 P1 | I/O3 P1 | I/O1 P1 | I/O8 P2 | I/O4 P2 | I/O2 P2 | $\overline{MRST}$ | CLKBIST | I/O2 P3 | I/O4 P3 | I/O8 P3 | I/O1 P4 | I/O3 P4 | I/O5 P4 | I/O7 P4 | $\overline{UB}$ P3 | VDD1 |
| **Y** | $\overline{LB}$ P2 | I/O8 P1 | I/O6 P1 | I/O4 P1 | I/O2 P1 | I/O0 P1 | 1/O7 P2 | I/O5 P2 | I/O3 P2 | I/O1 P2 | I/O1 P3 | I/O3 P3 | I/O5 P3 | I/O7 P3 | I/O0 P4 | I/O2 P4 | I/O4 P4 | I/O6 P4 | I/O8 P4 | $\overline{LB}$ P3 |

**Note**
4. Central Leads are for thermal dissipation only. They are connected to device $V_{SS}$.

## Selection Guide

| Description | CY7C0430CV –133 | Unit |
|---|---|---|
| $f_{MAX2}$ | 133[5] | MHz |
| Max Access Time (Clock to Data) | 4.2 | ns |
| Max Operating Current $I_{CC}$ | 750 | mA |
| Max Standby Current for $I_{SB1}$ (All ports TTL Level) | 200 | mA |
| Max Standby Current for $I_{SB3}$ (All ports CMOS Level) | 15 | mA |

**Note**
5.  $f_{MAX2}$ for industrial is 133 MHz.

## Pin Definitions

| Port 1 | Port 2 | Port 3 | Port 4 | Description |
|---|---|---|---|---|
| $A_{0P1}$–$A_{15P1}$ | $A_{0P2}$–$A_{15P2}$ | $A_{0P3}$–$A_{15P3}$ | $A_{0P4}$–$A_{15P4}$ | **Address Input/Output.** |
| $I/O_{0P1}$–$I/O_{17P1}$ | $I/O_{0P2}$–$I/O_{17P2}$ | $I/O_{0P3}$–$I/O_{17P3}$ | $I/O_{0P4}$–$I/O_{17P4}$ | **Data Bus Input/Output.** |
| $CLK_{P1}$ | $CLK_{P2}$ | $CLK_{P3}$ | $CLK_{P4}$ | **Clock Input.** This input can be free running or strobed. Maximum clock input rate is $f_{MAX2}$. |
| $\overline{LB}_{P1}$ | $\overline{LB}_{P2}$ | $\overline{LB}_{P3}$ | $\overline{LB}_{P4}$ | **Lower Byte Select Input.** Asserting this signal LOW enables read and write operations to the lower byte. For read operations both the LB and OE signals must be asserted to drive output data on the lower byte of the data pins. |
| $\overline{UB}_{P1}$ | $\overline{UB}_{P2}$ | $\overline{UB}_{P3}$ | $\overline{UB}_{P4}$ | **Upper Byte Select Input.** Same function as $\overline{LB}$, but to the upper byte. |
| $\overline{CE}_{0P1}$,$CE_{1P1}$ | $\overline{CE}_{0P2}$,$CE_{1P2}$ | $\overline{CE}_{0P3}$,$CE_{1P3}$ | $\overline{CE}_{0P4}$,$CE_{1P4}$ | **Chip Enable Input.** To select any port, both $\overline{CE}_0$ AND $CE_1$ must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$). |
| $\overline{OE}_{P1}$ | $\overline{OE}_{P2}$ | $\overline{OE}_{P3}$ | $\overline{OE}_{P4}$ | **Output Enable Input.** This signal must be asserted LOW to enable the I/O data lines during read operations. OE is asynchronous input. |
| $R/\overline{W}_{P1}$ | $R/\overline{W}_{P2}$ | $R/\overline{W}_{P3}$ | $R/\overline{W}_{P4}$ | **Read/Write Enable Input.** This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH. |
| $\overline{MRST}$ | | | | **Master Reset Input.** This is one signal for All Ports. $\overline{MRST}$ is an asynchronous input. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A MRST operation is required at power-up. |
| $\overline{CNTRST}_{P1}$ | $\overline{CNTRST}_{P2}$ | $\overline{CNTRST}_{P3}$ | $\overline{CNTRST}_{P4}$ | **Counter Reset Input.** Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST is second to MRST in priority with respect to counter and mask register operations. |
| $\overline{MKLD}_{P1}$ | $\overline{MKLD}_{P2}$ | $\overline{MKLD}_{P3}$ | $\overline{MKLD}_{P4}$ | **Mask Register Load Input.** Asserting this signal LOW loads the mask register with the external address available on the address lines. MKLD operation has higher priority over CNTLD operation. |
| $\overline{CNTLD}_{P1}$ | $\overline{CNTLD}_{P2}$ | $\overline{CNTLD}_{P3}$ | $\overline{CNTLD}_{P4}$ | **Counter Load Input.** Asserting this signal LOW loads the burst counter with the external address present on the address pins. |
| $\overline{CNTINC}_{P1}$ | $\overline{CNTINC}_{P2}$ | $\overline{CNTINC}_{P3}$ | $\overline{CNTINC}_{P4}$ | **Counter Increment Input.** Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. |
| $\overline{CNTRD}_{P1}$ | $\overline{CNTRD}_{P2}$ | $\overline{CNTRD}_{P3}$ | $\overline{CNTRD}_{P4}$ | **Counter Readback Input.** When asserted LOW, the internal address value of the counter will be read back on the address lines. During CNTRD operation, both CNTLD and CNTINC must be HIGH. Counter readback operation has higher priority over mask register readback operation. Counter readback operation is independent of port chip enables. If address readback operation occurs with chip enables active ($\overline{CE}_0$ = LOW, $CE_1$ = HIGH), the data lines (I/Os) will be three-stated. The readback timing will be valid after one no-operation cycle plus $t_{CD2}$ from the rising edge of the next cycle. |

## Pin Definitions (continued)

| Port 1 | Port 2 | Port 3 | Port 4 | Description |
|---|---|---|---|---|
| $\overline{MKRD}_{P1}$ | $\overline{MKRD}_{P2}$ | $\overline{MKRD}_{P3}$ | $\overline{MKRD}_{P4}$ | **Mask Register Readback Input**. When asserted LOW, the value of the mask register will be readback on address lines. During mask register readback operation, all counter and MKLD inputs must be HIGH (see Counter and Mask Register Operations truth table). Mask register readback operation is independent of port chip enables. If address readback operation occurs with chip enables active ($\overline{CE}_0$ = LOW, $CE_1$ = HIGH), the data lines (I/Os) will be three-stated. The readback will be valid after one no-operation cycle plus $t_{CD2}$ from the rising edge of the next cycle. |
| $\overline{CNTINT}_{P1}$ | $\overline{CNTINT}_{P2}$ | $\overline{CNTINT}_{P3}$ | $\overline{CNTINT}_{P4}$ | **Counter Interrupt Flag Output**. Flag is asserted LOW for one clock cycle when the counter wraps around to location zero. |
| $\overline{INT}_{P1}$ | $\overline{INT}_{P2}$ | $\overline{INT}_{P3}$ | $\overline{INT}_{P4}$ | **Interrupt Flag Output**. Interrupt permits communications between all four ports. The upper four memory locations can be used for message passing. Example of operation: $\overline{INT}_{P4}$ is asserted LOW when another port writes to the mailbox location of Port 4. Flag is cleared when Port 4 reads the contents of its mailbox. The same operation is applicable to ports 1, 2, and 3. |
| TMS | | | | **JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK. |
| TCK | | | | **JTAG Test Clock Input**. This can be CLK of any port or an external clock connected to the JTAG TAP. |
| TDI | | | | **JTAG Test Data Input**. This is the only data input. TDI inputs will shift data serially in to the selected register. |
| TDO | | | | **JTAG Test Data Output**. This is the only data output. TDO transitions occur on the falling edge of TCK. TDO normally three-stated except when captured data is shifted out of the JTAG TAP. |
| CLKBIST | | | | BIST Clock Input. |
| GND | | | | Thermal Ground for Heat Dissipation. |
| $V_{SS}$ | | | | Ground Input. |
| $V_{DD}$ | | | | Power Input. |
| $V_{SS1}$ | | | | Address Lines Ground Input. |
| $V_{DD1}$ | | | | Address Lines Power Input. |
| $V_{SS2}$ | | | | Data Lines Ground Input. |
| $V_{DD2}$ | | | | Data Lines Power Input. |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ............................... –65 °C to + 150 °C

Ambient temperature with
power applied .......................................... –55 °C to + 125 °C

Supply voltage to ground potential ..............–0.5 V to + 4.6 V

DC voltage applied to
outputs in high-Z state ......................... –0.5 V to $V_{CC}$ + 0.5 V

DC input voltage ................................... –0.5 V to $V_{CC}$ + 0.5 V

Output current into outputs (LOW) .............................. 20 mA

Static discharge voltage.......................................... > 2200 V

Latch up current...................................................... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ |
|---|---|---|
| Industrial | –40 °C to +85 °C | 3.3 V $\pm$ 150 mV |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Quadport DSE Family | | | Unit |
|---|---|---|---|---|---|
| | | −133 | | | |
| | | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH voltage ($V_{CC}$ = Min., $I_{OH}$ = –4.0 mA) | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage ($V_{CC}$ = Min., $I_{OH}$ = +4.0 mA) | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | 2.0 | – | | V |
| $V_{IL}$ | Input LOW voltage | | – | 0.8 | V |
| $I_{OZ}$ | Output leakage current | –10 | – | 10 | μA |
| $I_{CC}$ | Operating current ($V_{CC}$ = Max., $I_{OUT}$ = 0 mA) Outputs Disabled, $\overline{CE}$ = $V_{IL}$, f = $f_{max}$ | – | 350 | 700 | mA |
| $I_{SB1}$ | Standby current (four ports toggling at TTL Levels,0 active) $\overline{CE}_{1\text{-}4} \geq V_{IH}$, f = $f_{MAX}$ | – | 80 | 200 | mA |
| $I_{SB2}$ | Standby current (four ports toggling at TTL Levels, 1 active) $\overline{CE}_1 \mid \overline{CE}_2 \mid \overline{CE}_3 \mid \overline{CE}_4 \leq V_{IL}$, f = $f_{MAX}$ | – | 150 | 300 | mA |
| $I_{SB3}$ | Standby current (four ports CMOS Level, 0 active) $\overline{CE}_{1-4} \geq V_{IH}$, f = 0 | – | 1.5 | 15 | mA |
| $I_{SB4}$ | Standby current (four ports CMOS Level, 1 active and toggling) $\overline{CE}_1 \mid \overline{CE}_2 \mid \overline{CE}_3 \mid \overline{CE}_4 \leq V_{IL}$, f = $f_{MAX}$ | – | 110 | 290 | mA |

## JTAG TAP Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH voltage | $I_{OH} = -4.0$ mA | 2.4 | – | V |
| $V_{OL1}$ | Output LOW voltage | $I_{OL} = 4.0$ mA | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | | 2.0 | – | V |
| $V_{IL}$ | Input LOW voltage | | – | 0.8 | V |
| $I_X$ | Input leakage current | $GND \leq V_I \leq V_{DD}$ | −100 | 100 | μA |

## Capacitance

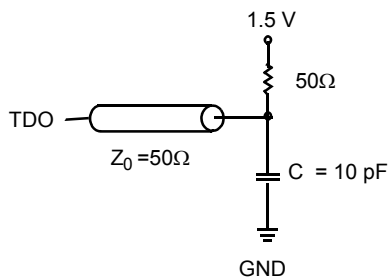| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ (All Pins) | Input Capacitance | $T_A = 25$ °C, f = 1 MHz, $V_{CC} = 3.3$ V | 10 | pF |
| $C_{OUT}$ (All Pins) | Output Capacitance | | 10 | pF |
| $C_{IN}$ (CLK Pins) | Input Capacitance | | 15 | pF |
| $C_{OUT}$ (CLK Pins) | Output Capacitance | | 15 | pF |

## AC Test Loads and Waveforms
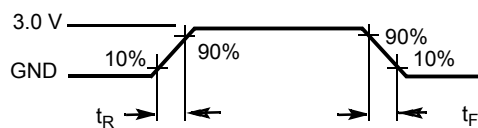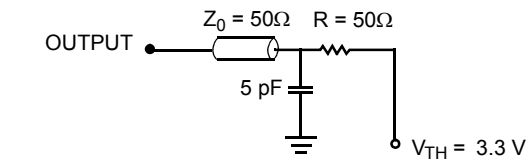
**Figure 2. AC Test Load**
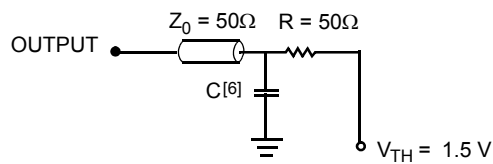


(a) Normal Load
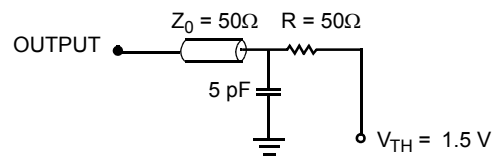
(b) Three-State Delay

(c) TAP Load

All Input Pulses

**Note**
6. Test conditions: C = 10 pF.

## JTAG Timing and Switching Waveforms

| Parameter | Description | Quadport DSE Family | | Unit |
|---|---|---|---|---|
| | | −133 | | |
| | | Min | Max | |
| $f_{JTAG}$ | Maximum JTAG TAP Controller Frequency | – | 10 | MHz |
| $t_{TCYC}$ | TCK Clock Cycle Time | 100 | – | ns |
| $t_{TH}$ | TCK Clock High Time | 40 | – | ns |
| $t_{TL}$ | TCK Clock Low Time | 40 | – | ns |
| $t_{TMSS}$ | TMS Set-up to TCK Clock Rise | 20 | – | ns |
| $t_{TMSH}$ | TMS Hold After TCK Clock Rise | 20 | – | ns |
| $t_{TDIS}$ | TDI Set-up to TCK Clock Rise | 20 | – | ns |
| $t_{TDIH}$ | TDI Hold after TCK Clock Rise | 20 | – | ns |
| $t_{TDOV}$ | TCK Clock Low to TDO Valid | – | 20 | ns |
| $t_{TDOX}$ | TCK Clock Low to TDO Invalid | 0 | – | ns |
| $f_{BIST}$ | Maximum CLKBIST Frequency | – | 50 | MHz |
| $t_{BH}$ | CLKBIST High Time | 6 | – | ns |
| $t_{BL}$ | CLKBIST Low Time | 6 | – | ns |
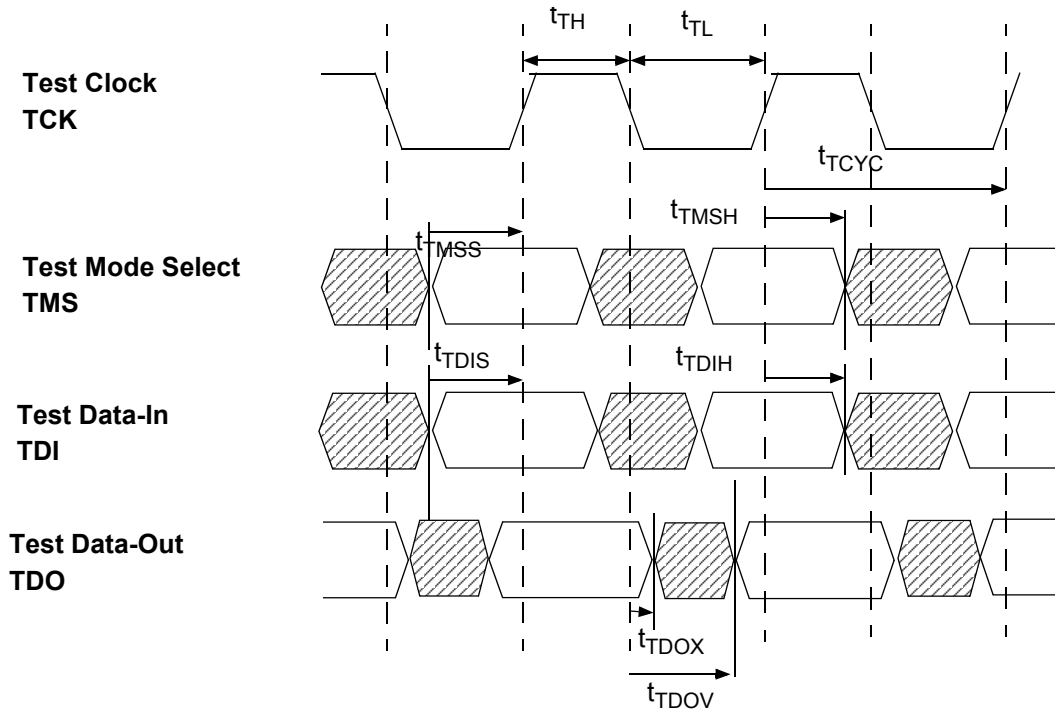
## Switching Characteristics

Over the Industrial Operating Range

| Parameter [7] | Description | CY7C0430CV | | Unit |
| | | −133 | | |
| | | Min | Max | |
|---|---|---|---|---|
| $f_{MAX2}$[8] | Maximum Frequency | – | 133 | MHz |
| $t_{CYC2}$[8] | Clock Cycle Time | 7.5 | – | ns |
| $t_{CH2}$ | Clock HIGH Time | 3 | – | ns |
| $t_{CL2}$ | Clock LOW Time | 3 | – | ns |
| $t_R$ | Clock Rise Time | – | 2 | ns |
| $t_F$ | Clock Fall Time | – | 2 | ns |
| $t_{SA}$ | Address Set-up Time | 2.3 | – | ns |
| $t_{HA}$ | Address Hold Time | 0.7 | – | ns |
| $t_{SC}$ | Chip Enable Set-up Time | 2.3 | – | ns |
| $t_{HC}$ | Chip Enable Hold Time | 0.7 | – | ns |
| $t_{SW}$ | R/$\overline{W}$ Set-up Time | 2.3 | – | ns |
| $t_{HW}$ | R/$\overline{W}$ Hold Time | 0.7 | – | ns |
| $t_{SD}$ | Input Data Set-up Time | 2.3 | – | ns |
| $t_{HD}$ | Input Data Hold Time | 0.7 | – | ns |
| $t_{SB}$ | Byte Set-up Time | 2.3 | – | ns |
| $t_{HB}$ | Byte Hold Time | 0.7 | – | ns |
| $t_{SCLD}$ | $\overline{CNTLD}$ Set-up Time | 2.3 | – | ns |
| $t_{HCLD}$ | $\overline{CNTLD}$ Hold Time | 0.7 | – | ns |
| $t_{SCINC}$ | $\overline{CNTINC}$ Set-up Time | 2.3 | – | ns |
| $t_{HCINC}$ | $\overline{CNTINC}$ Hold Time | 0.7 | – | ns |
| $t_{SCRST}$ | $\overline{CNTRST}$ Set-up Time | 2.3 | – | ns |
| $t_{HCRST}$ | $\overline{CNTRST}$ Hold Time | 0.7 | – | ns |
| $t_{SCRD}$ | $\overline{CNTRD}$ Set-up Time | 2.3 | – | ns |
| $t_{HCRD}$ | $\overline{CNTRD}$ Hold Time | 0.7 | – | ns |
| $t_{SMLD}$ | $\overline{MKLD}$ Set-up Time | 2.3 | – | ns |
| $t_{HMLD}$ | $\overline{MKLD}$ Hold Time | 0.7 | – | ns |
| $t_{SMRD}$ | $\overline{MKRD}$ Set-up Time | 2.3 | – | ns |
| $t_{HMRD}$ | $\overline{MKRD}$ Hold Time | 0.7 | – | ns |
| $t_{OE}$ | Output Enable to Data Valid | – | 6.5 | ns |
| $t_{OLZ}$[9] | $\overline{OE}$ to Low-Z | 1 | – | ns |
| $t_{OHZ}$[9] | $\overline{OE}$ to High-Z | 1 | 6 | ns |

**Notes**
7. If data is simultaneously written and read to the same address location and $t_{CCS}$ is violated, the data read from the address, as well as the subsequent data remaining in the address is undefined.
8. $f_{MAX2}$ for industrial is 133 MHz. $t_{CYC2}$ Min. for industrial is 7.5 ns.
9. This parameter is guaranteed by design, but it is not production tested.

## Switching Characteristics (continued)

Over the Industrial Operating Range

| Parameter [7] | Description | CY7C0430CV −133 Min | CY7C0430CV −133 Max | Unit |
|---|---|---|---|---|
| $t_{CD2}$ | Clock to Data Valid | – | 4.2 | ns |
| $t_{CA2}$ | Clock to Counter Address Readback Valid | – | 4.7 | ns |
| $t_{CM2}$ | Clock to Mask Register Readback Valid | – | 4.7 | ns |
| $t_{DC}$ | Data Output Hold After Clock HIGH | 1 | – | ns |
| $t_{CKHZ}$ | Clock HIGH to Output High-Z | 1 | 4.8 | ns |
| $t_{CKLZ}$ [9] | Clock HIGH to Output Low-Z | 1 | – | ns |
| $t_{SINT}$ | Clock to $\overline{INT}$ Set Time | 1 | 7.5 | ns |
| $t_{RINT}$ | Clock to $\overline{INT}$ Reset Time | 1 | 7.5 | ns |
| $t_{SCINT}$ | Clock to $\overline{CNTINT}$ Set Time | 1 | 7.5 | ns |
| $t_{RCINT}$ | Clock to $\overline{CNTINT}$ Reset Time | 1 | 7.5 | ns |
| **Master Reset Timing** | | | | |
| $t_{RS}$ | Master Reset Pulse Width | 7.5 | – | ns |
| $t_{RSR}$ | Master Reset Recovery Time | 7.5 | – | ns |
| $t_{ROF}$ | Master Reset to Output Flags Reset Time | – | 6.5 | ns |
| **Port to Port Delays** | | | | |
| $t_{CCS}$ [7] | Clock to Clock Set-up Time (time required after a write before you can read the same address location) | 6.5 | – | ns |

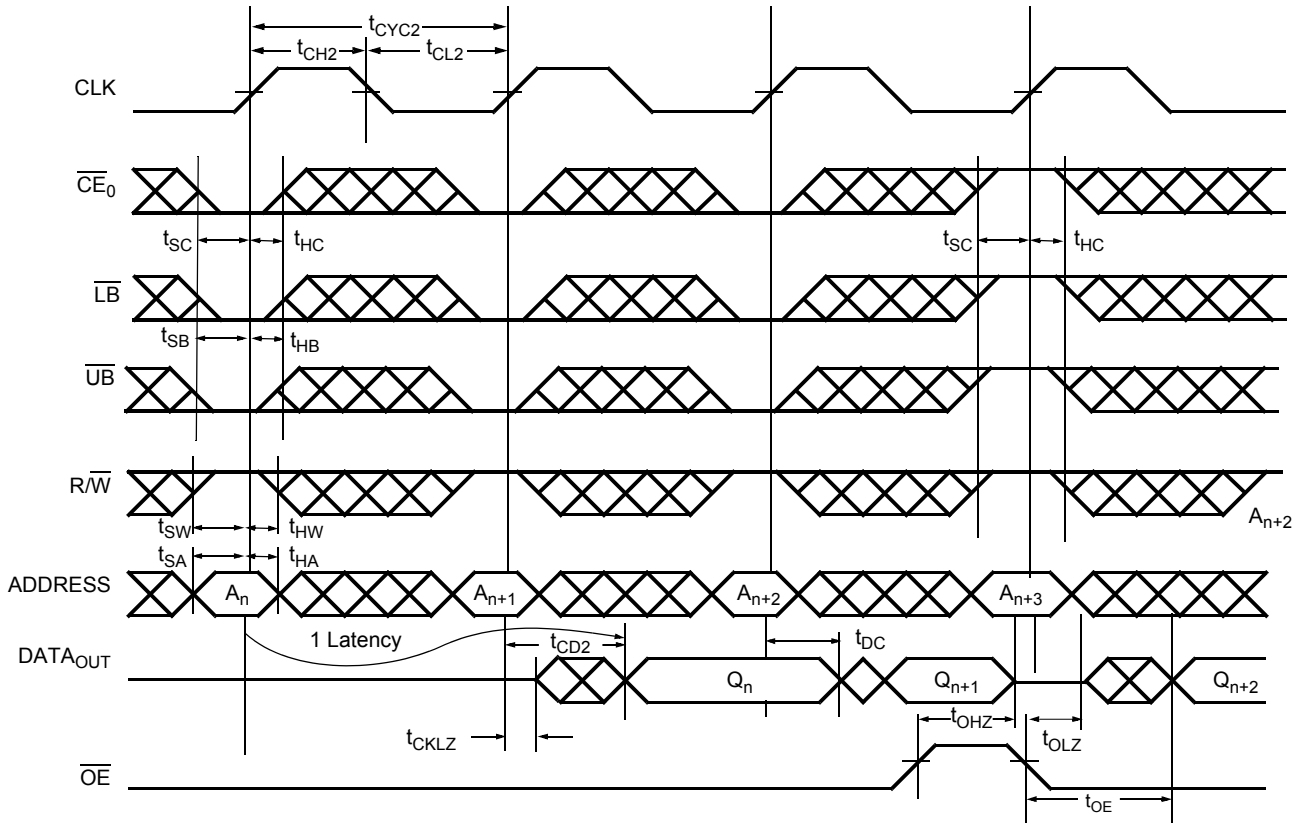## Switching Waveforms

**Figure 3.  Master Reset[10]**
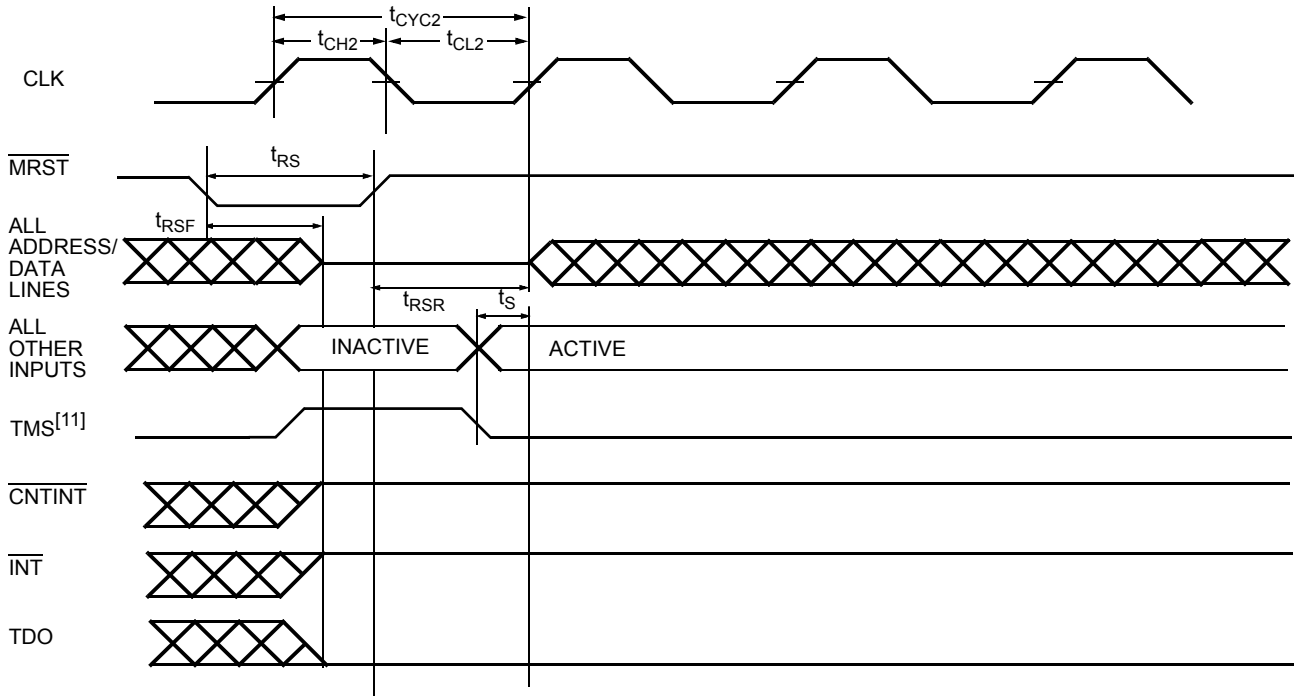


**Notes**
10. $t_S$ is the set-up time required for all input control signals.
11. To Reset the test port without resetting the device, TMS must be held low for five clock cycles.

## Switching Waveforms (continued)

**Figure 4. Read Cycle**[12, 13, 14, 15, 16]



**Notes**
12. $\overline{OE}$ is asynchronously controlled; all other inputs (excluding $\overline{MRST}$) are synchronous to the rising clock edge.
13. CNTLD = $V_{IL}$, $\overline{MKLD}$ = $V_{IH}$, CNTINC = x, and $\overline{MRST}$ = CNTRST = $V_{IH}$.
14. The output is disabled (high-impedance state) by $\overline{CE}$ = $V_{IH}$ following the next rising edge of the clock.
15. Addresses do not have to be accessed sequentially. Note 13 indicates that address is constantly loaded on the rising edge of the CLK. Numbers are for reference only.
16. $\overline{CE}$ is internal signal. $\overline{CE}$ = VIL if $\overline{CE_0}$ = $V_{IL}$ and CE₁ = $V_{IH}$.

## Switching Waveforms (continued)

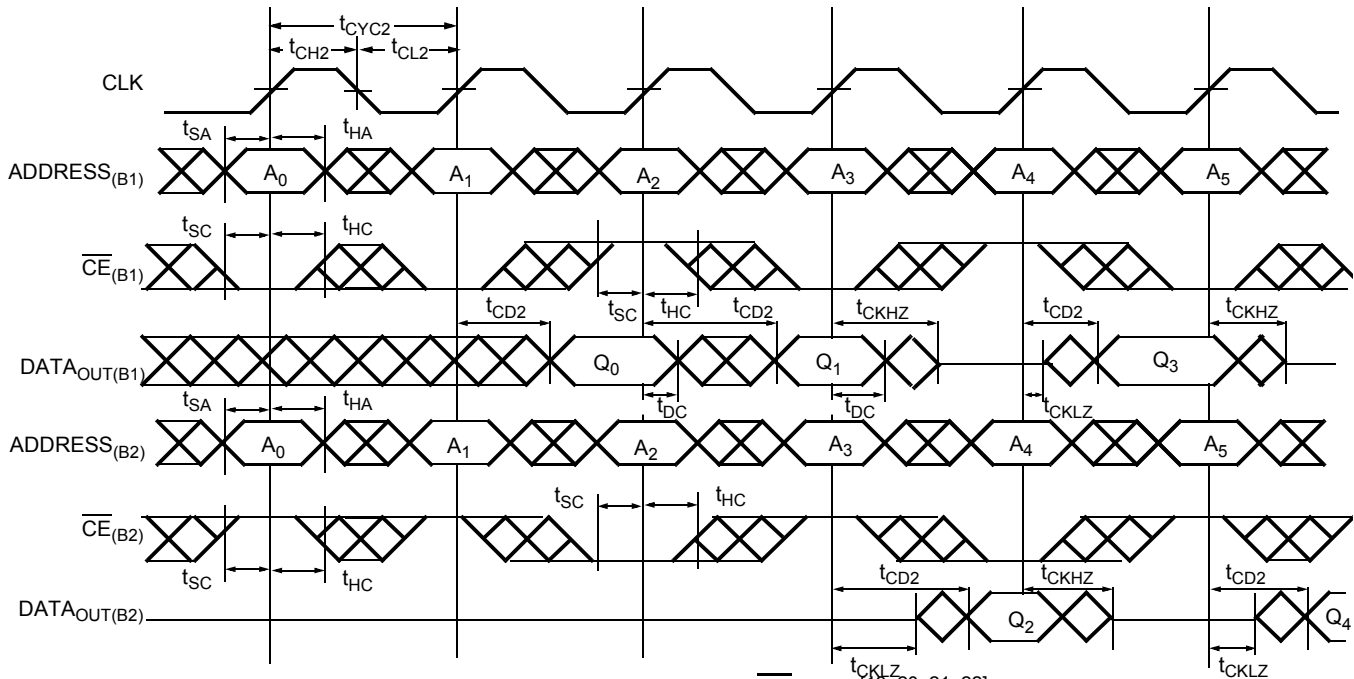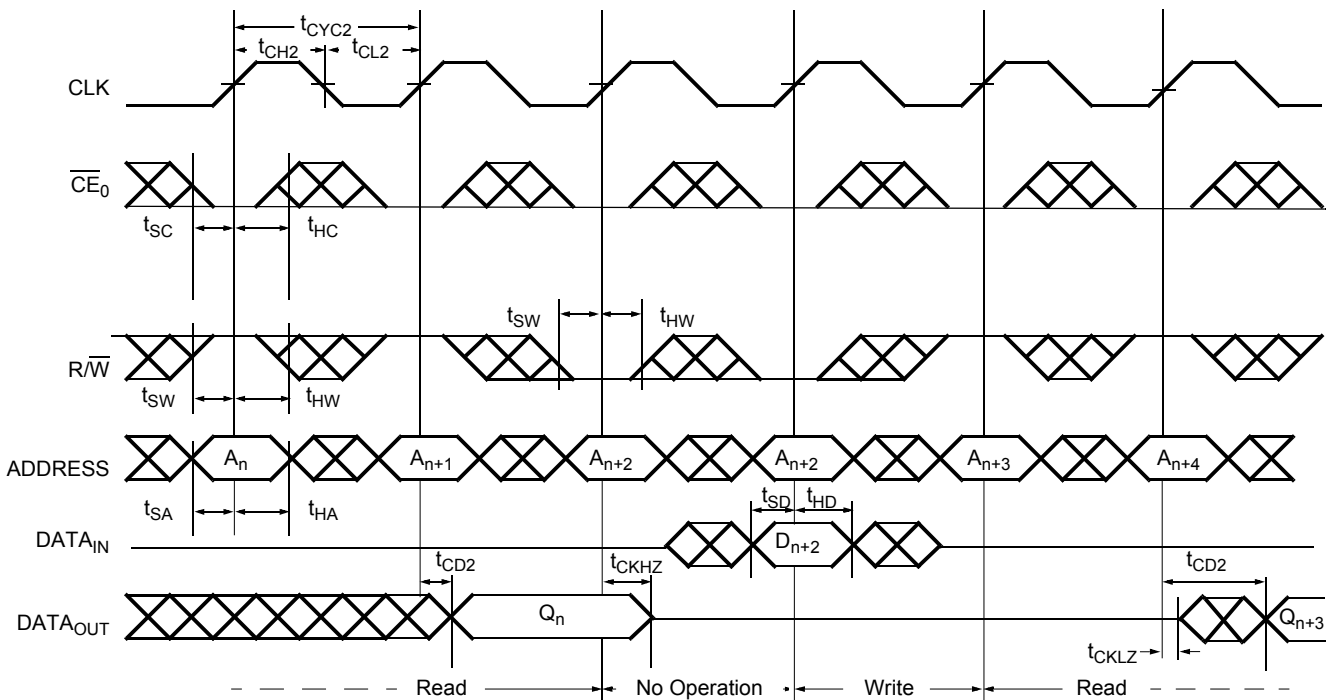**Figure 5. Bank Select Read**[17, 18]



**Figure 6. Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)**[19, 20, 21, 22]



**Notes**
17. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each bank consists of one QuadPort DSE device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
18. $\overline{LB} = \overline{UB} = \overline{OE} = \overline{CNTLD} = V_{IL}$; $\overline{MRST} = \overline{CNTRST} = \overline{MKLD} = V_{IH}$.
19. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
20. $\overline{LB} = \overline{UB} = \overline{CNTLD} = V_{IL}$; $\overline{MRST} = \overline{CNTRST} = \overline{MKLD} = V_{IH}$.
21. Addresses do not have to be accessed sequentially since $\overline{CNTLD} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference only.
22. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

## Switching Waveforms (continued)

**Figure 7. Read-to-Write-to-Read ($\overline{OE}$ Controlled)**[19, 20, 21, 22]
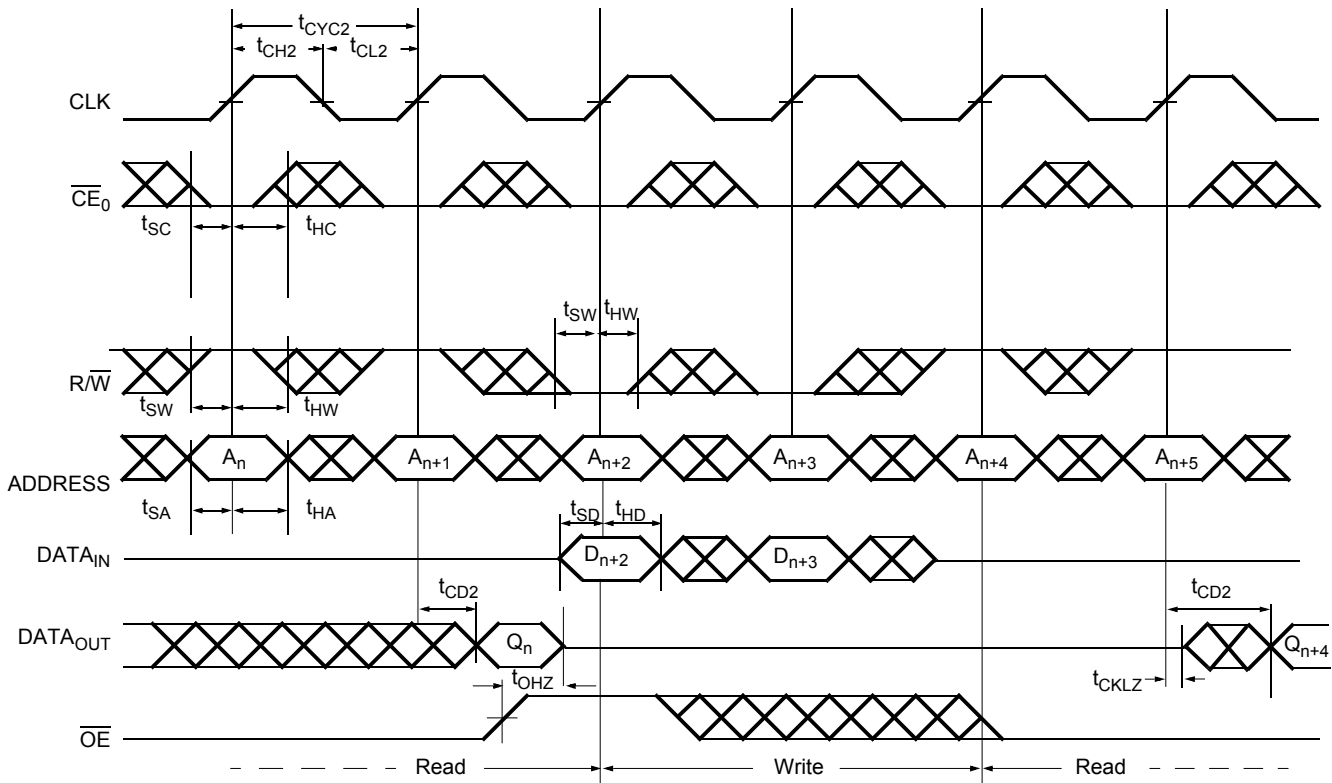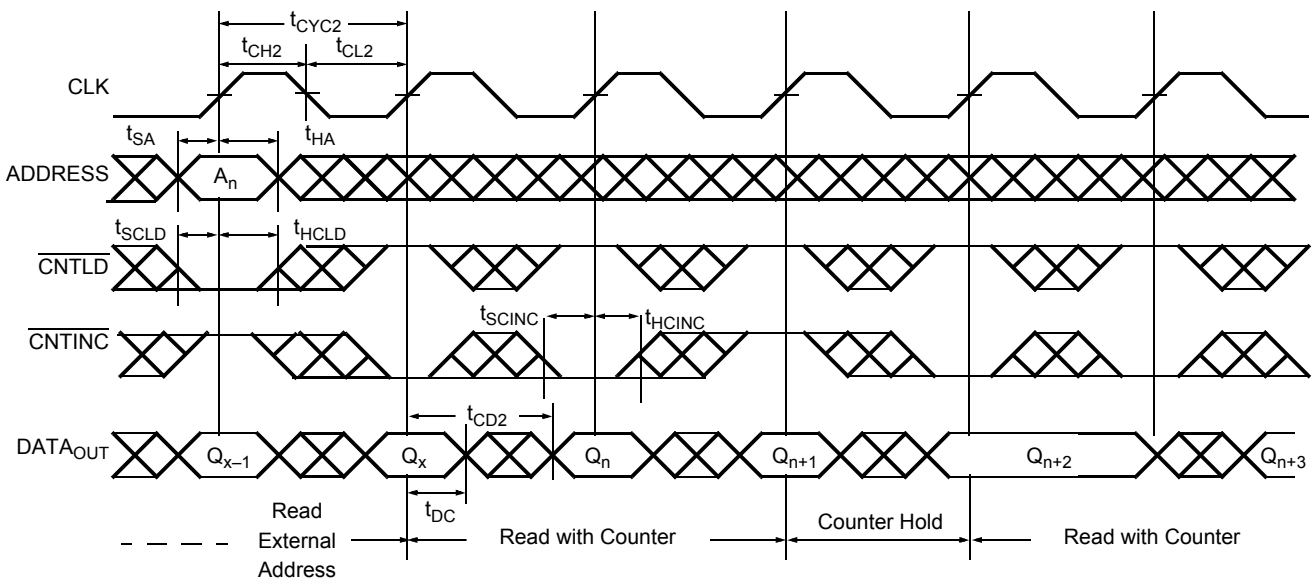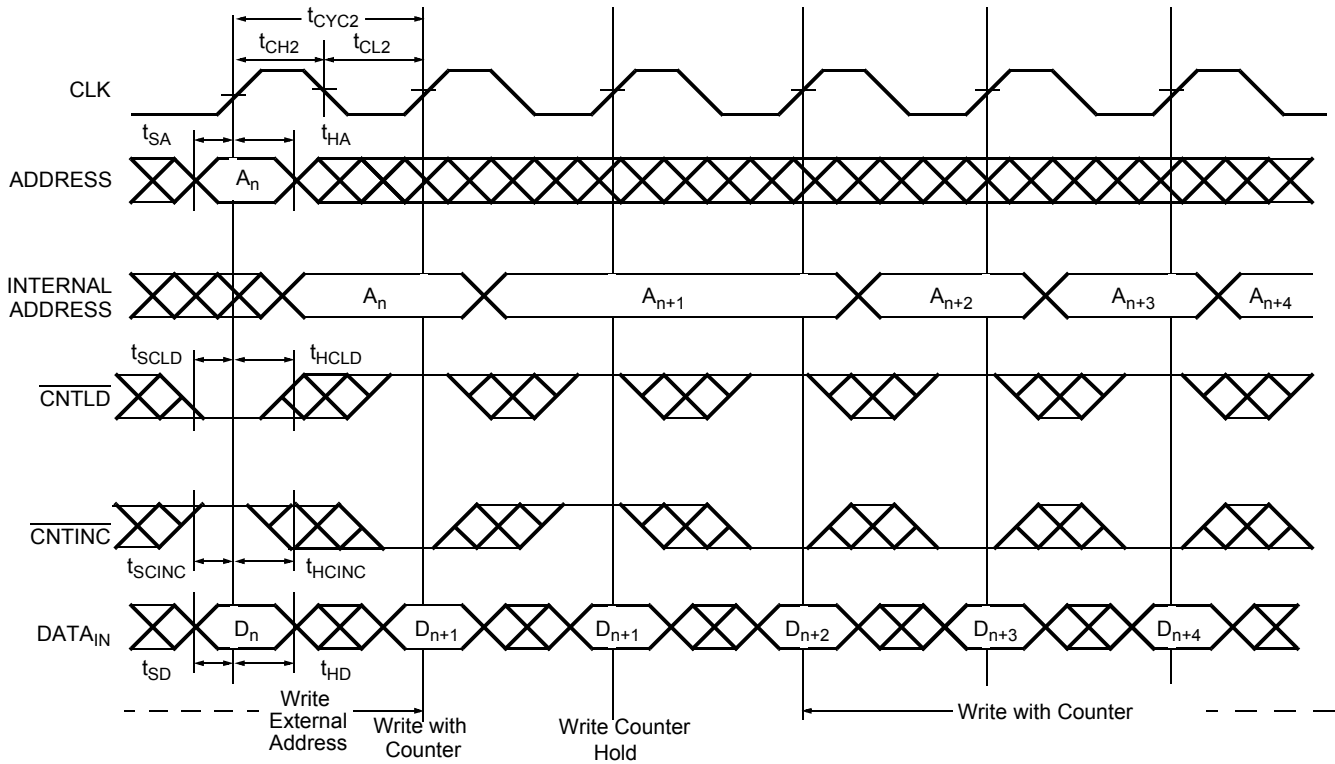
**Figure 8. Read with Address Counter Advance**[23, 24]

**Notes**
23. $\overline{CE}_0 = \overline{OE} = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = R/\overline{W} = \overline{CNTRST} = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = \overline{CNTRD} = V_{IH}$.
24. The "Internal Address" is equal to the "External Address" when $\overline{CNTLD} = V_{IL}$.

## Switching Waveforms (continued)

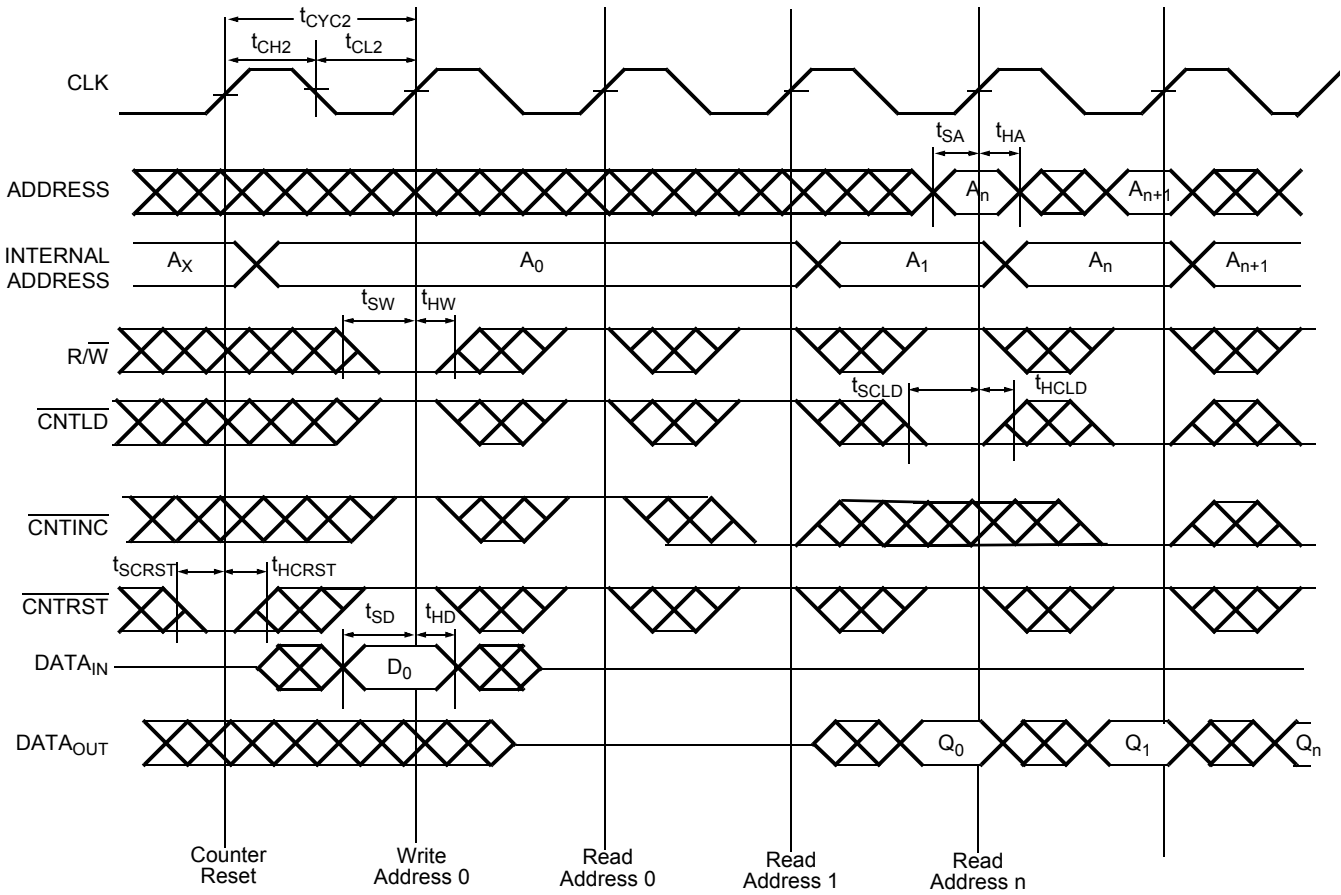**Figure 9. Write with Address Counter Advance** [25, 26]

## Switching Waveforms (continued)

### Figure 10. Counter Reset [27, 28, 29]



**Notes**
27. Addresses do not have to be accessed sequentially since $\overline{\text{CNTLD}}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference only.
28. $\overline{\text{CE}_0}$ = $\overline{\text{LB}}$ = $\overline{\text{UB}}$ = $V_{IL}$; $\text{CE}_1$ = $\overline{\text{MRST}}$ = $\overline{\text{MKLD}}$ = $\overline{\text{MKRD}}$ = $\overline{\text{CNTRD}}$ = $V_{IH}$.
29. No dead cycle exists during counter reset. A Read or Write cycle may be coincidental with the counter reset.

## Switching Waveforms (continued)

### Figure 11. Load and Read Address Counter[30]
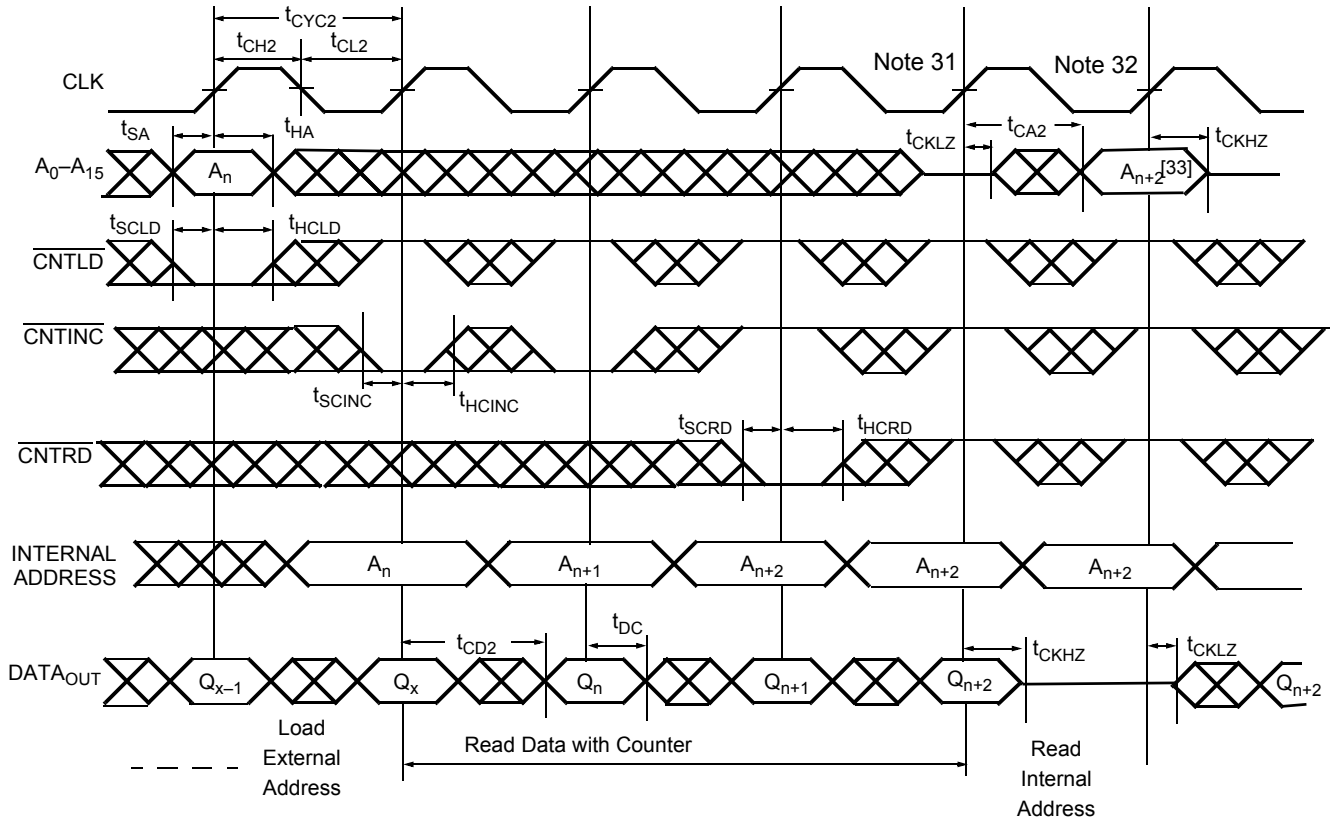
**Notes**
30. $\overline{CE}_0 = \overline{OE} = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = R/\overline{W} = \overline{CNTRST} = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = V_{IH}$.
31. Address in output mode. Host must not be driving address bus after time $t_{CKLZ}$ in next clock cycle.
32. Address in input mode. Host can drive address bus after $t_{CKHZ}$.
33. This is the value of the address counter being read out on the address lines.

## Switching Waveforms (continued)

**Figure 12. Load and Read Mask Register** [34]

**Notes**
34. $CE_0 = \overline{OE} = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = R/\overline{W} = \overline{CNTRST} = \overline{MRST} = \overline{CNTLD} = \overline{CNTRD} = \overline{CNTINC} = V_{IH}$.
35. This is the value of the Mask Register read out on the address lines.

## Switching Waveforms (continued)

### Figure 13. Port 1 Write to Port 2 Read [36, 37, 38]

## Switching Waveforms (continued)

**Figure 14. Counter Interrupt** [39, 40, 41]



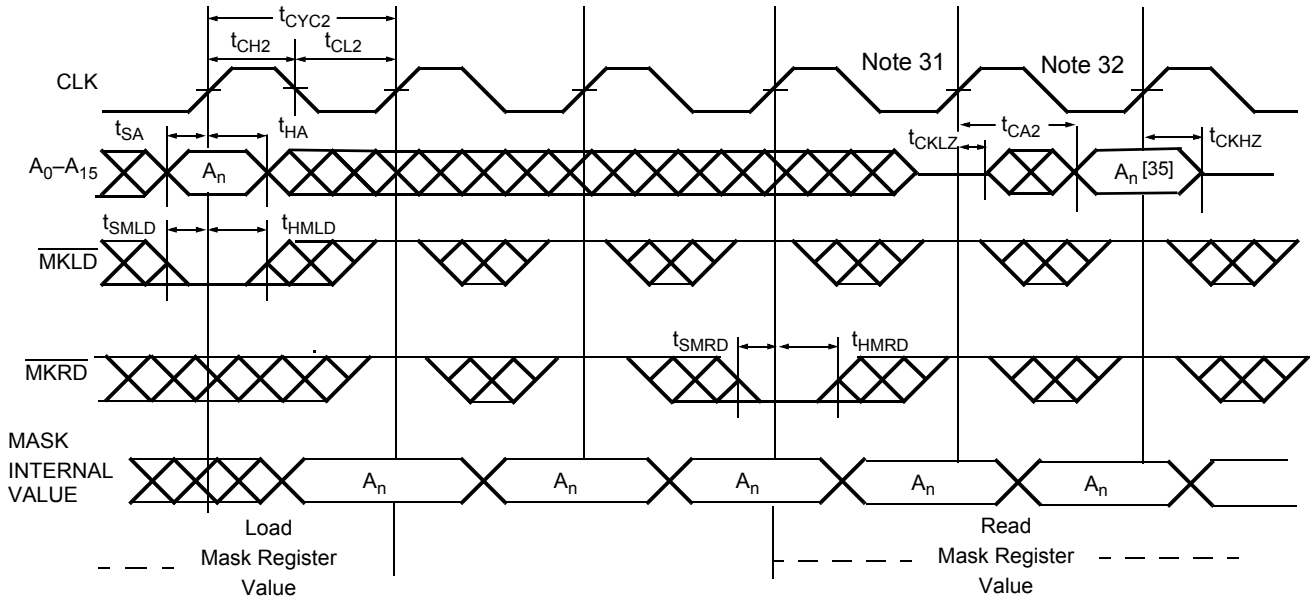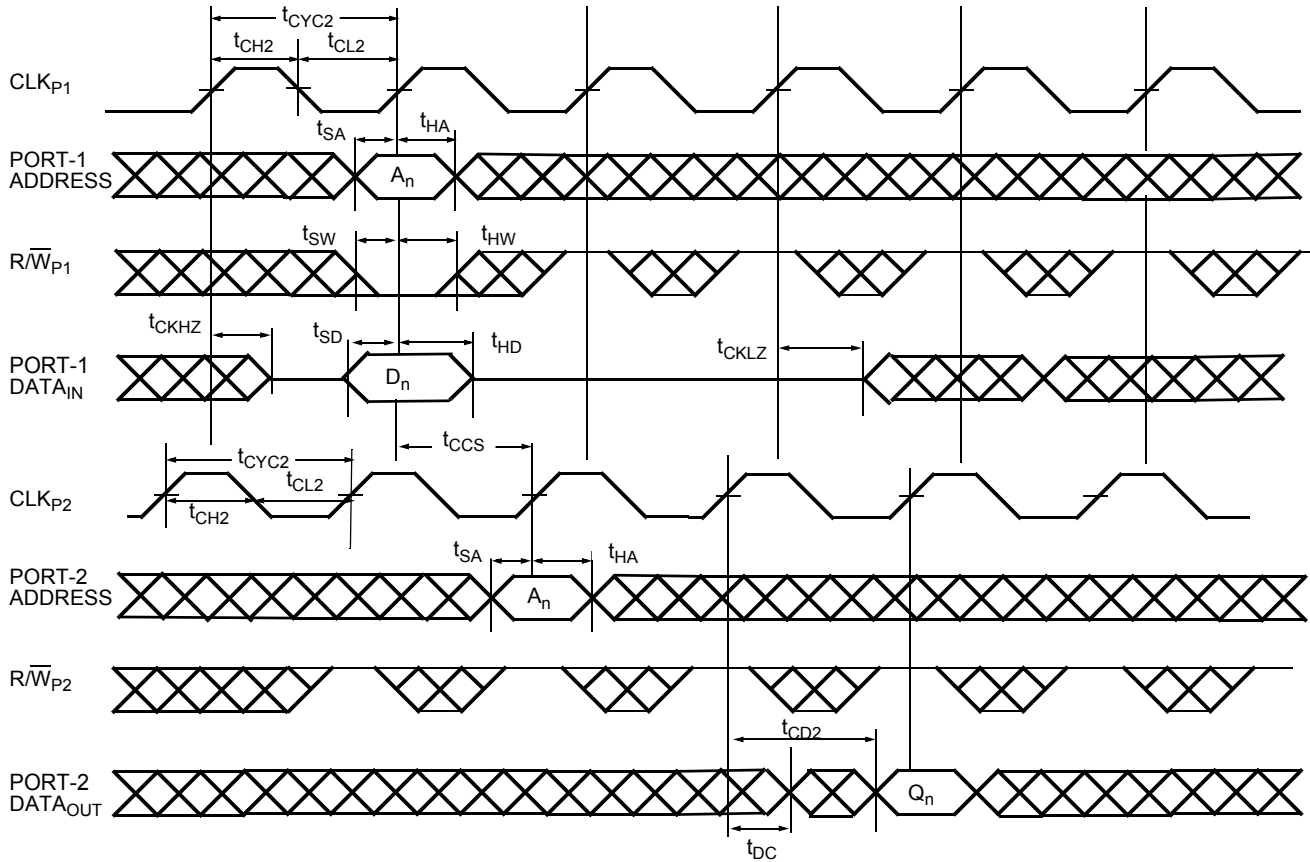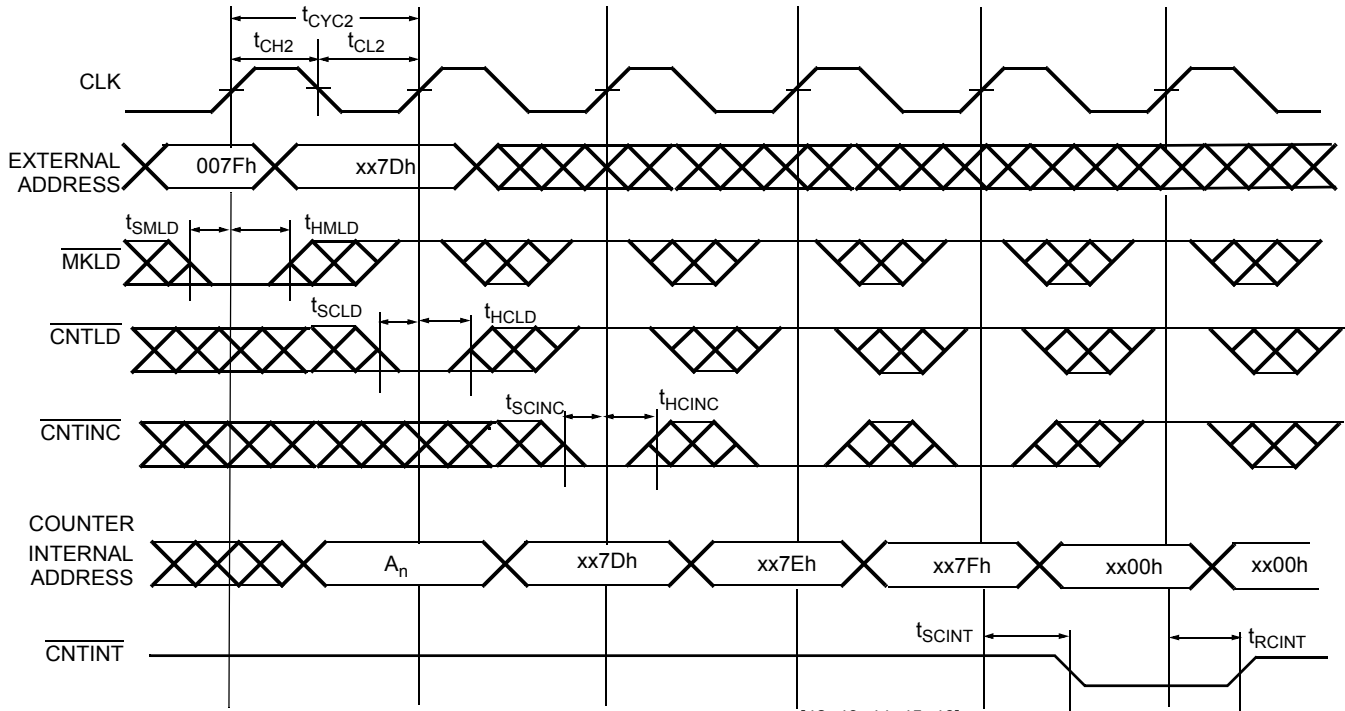**Figure 15. Mailbox Interrupt Timing** [42, 43, 44, 45, 46]
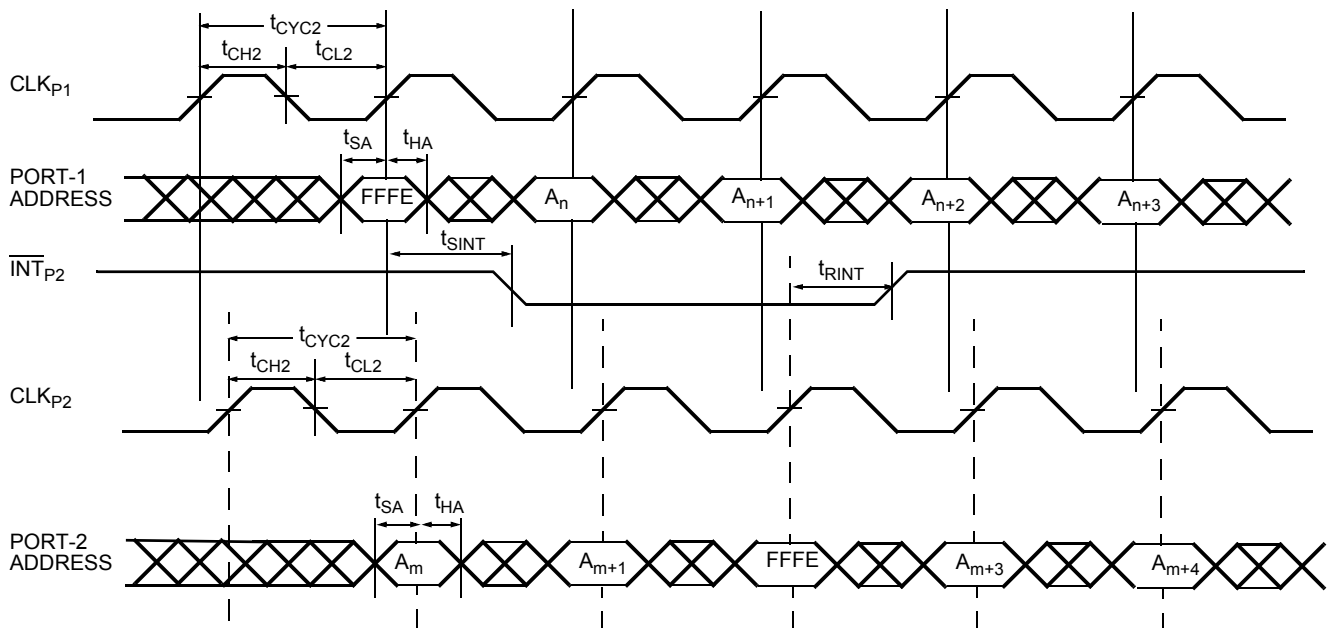


**Notes**
39. $\overline{CE_0} = \overline{OE} = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = R/\overline{W} = \overline{CNTRST} = \overline{MRST} = \overline{CNTRD} = \overline{MKRD} = V_{IH}$.
40. $\overline{CNTINT}$ is always driven.
41. $\overline{CNTINC}$ goes LOW as the counter address masked portion is incremented from xx7Fh to xx00h. The "x" is "Don't Care."
42. $\overline{CE_0} = \overline{OE} = \overline{LB} = \overline{UB} = \overline{CNTLD} = V_{IL}$; $CE_1 = \overline{CNTRST} = \overline{MRST} = \overline{CNTRD} = \overline{CNTINC} = \overline{MKRD} = \overline{MKLD} = V_{IH}$.
43. Address "FFFE" is the mailbox location for Port 2.
44. Port 1 is configured for Write operation, and Port 2 is configured for Read operation.
45. Port 1 and Port 2 are used for simplicity. All four ports can write to or read from any mailbox.
46. Interrupt flag is set with respect to the rising edge of the write clock, and is reset with respect to the rising edge of the read clock.

**Table 1. Read/Write and Enable Operation (Any Port)**[47, 48, 49]

| Inputs | | | | | Outputs | Operation |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | CLK | $\overline{CE_0}$ | $CE_1$ | $R/\overline{W}$ | $I/O_0$–$I/O_{17}$ | |
| X | ⌐ | H | X | X | High-Z | Deselected |
| X | ⌐ | X | L | X | High-Z | Deselected |
| X | ⌐ | L | H | L | $D_{IN}$ | Write |
| L | ⌐ | L | H | H | $D_{OUT}$ | Read |
| H | X | L | H | X | High-Z | Outputs Disabled |

**Table 2. Address Counter and Counter-Mask Register Control Operation (Any Port)**[47, 50, 51]

| CLK | MRST | CNTRST | MKLD | CNTLD | CNTINC | CNTRD | MKRD | Mode | Operation |
|---|---|---|---|---|---|---|---|---|---|
| X | L | X | X | X | X | X | X | Master-Reset | Counter/Address Register Reset and Mask Register Set (resets entire chip as per reset state table) |
| ⌐ | H | L | X | X | X | X | X | Reset | Counter/Address Register Reset |
| ⌐ | H | H | L | X | X | X | X | Load | Load of Address Lines into Mask Register |
| ⌐ | H | H | H | L | X | X | X | Load | Load of Address Lines into Counter/Address Register |
| ⌐ | H | H | H | H | L | X | X | Increment | Counter Increment |
| ⌐ | H | H | H | H | H | L | X | Readback | Readback Counter on Address Lines |
| ⌐ | H | H | H | H | H | H | L | Readback | Readback Mask Register on Address Lines |
| ⌐ | H | H | H | H | H | H | H | Hold | Counter Hold |

**Notes**
47. "X" = "Don't Care," "H" = $V_{IH}$, "L" = $V_{IL}$.
48. $\overline{OE}$ is an asynchronous input signal.
49. When $\overline{CE}$ changes state, deselection and read happen after one cycle of latency.
50. $\overline{CE_0} = \overline{OE} = V_{IL}$; $CE_1 = R/\overline{W} = V_{IH}$.
51. Counter operation and mask register operation are independent of Chip Enables.

## Master Reset

The QuadPort DSE device undergoes a complete reset by taking its Master Reset (MRST) input LOW. The Master Reset input can switch asynchronously to the clocks. A Master Reset initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). A Master Reset also forces the Mailbox Interrupt (INT) flags and the Counter Interrupt (CNTINT) flags HIGH, resets the BIST controller, and takes all registered control signals to a deselected read state.[52] A Master Reset must be performed on the QuadPort DSE device after power-up.

## Interrupts

The upper four memory locations may be used for message passing and permit communications between ports. Table 3 shows the interrupt operation for all ports. For the 1-Mb QuadPort DSE device, the highest memory location FFFF is the mailbox for Port 1, FFFE is the mailbox for Port 2, FFFD is the mailbox for Port 3, and FFFC is the mailbox for Port 4. Table 3 shows that in order to set Port 1 $\overline{INT}_{P1}$ flag, a write by any other port to address FFFF will assert $\overline{INT}_{P1}$ LOW. A read of FFFF location by Port 1 will reset $\overline{INT}_{P1}$ HIGH. When one port writes to the other port's mailbox, the Interrupt flag ($\overline{INT}$) of the port that the mailbox belongs to is asserted LOW. The Interrupt is reset when the owner (port) of the mailbox reads the contents of the mailbox. The interrupt flag is set in a flow-through mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-through mode (i.e., it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. If an application does not require message passing, INT pins should be treated as no-connect and should be left floating. When two ports or more, write to the same mailbox at the same time $\overline{INT}$ will be asserted but the contents of the mailbox are not guaranteed to be valid.

**Table 3. Interrupt Operation Example**

| Function | Port 1 | | Port 2 | | Port 3 | | Port 4 | |
|---|---|---|---|---|---|---|---|---|
| | $A_{0P1-15P1}$ | $\overline{INT}_{P1}$ | $A_{0P2-15P2}$ | $\overline{INT}_{P2}$ | $A_{0P3-15P3}$ | $\overline{INT}_{P3}$ | $A_{0P4-15P4}$ | $\overline{INT}_{P4}$ |
| Set Port 1 $\overline{INT}_{P1}$ Flag | X | L | FFFF | X | FFFF | X | FFFF | X |
| Reset Port 1 $\overline{INT}_{P1}$ Flag | FFFF | H | X | X | X | X | X | X |
| Set Port 2 $\overline{INT}_{P2}$ Flag | FFFE | X | X | L | FFFE | X | FFFE | X |
| Reset Port 2 $\overline{INT}_{P2}$ Flag | X | X | FFFE | H | X | X | X | X |
| Set Port 3 $\overline{INT}_{P3}$ Flag | FFFD | X | FFFD | X | X | L | FFFD | X |
| Reset Port 3 $\overline{INT}_{P3}$ Flag | X | X | X | X | FFFD | H | X | X |
| Set Port 4 $\overline{INT}_{P4}$ Flag | FFFC | X | FFFC | X | FFFC | X | X | L |
| Reset Port 4 $\overline{INT}_{P4}$ Flag | X | X | X | X | X | X | FFFC | H |

**Note**
52. During Master Reset the control signals will be set to a deselected read state: $\overline{CE}_{0I} = \overline{LB}_I = \overline{UB}_I = R/\overline{W}_I = \overline{MKLD}_I = \overline{MKRD}_I = \overline{CNTRD}_I = \overline{CNTRST}_I = \overline{CNTLD}_I = CNTINC_I = V_{IH}$; $CE_{1I} = V_{IL}$. The "I" suffix on all these signals denotes that these are the internal registered equivalent of the associated pin signals.

## Address Counter Control Operations

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for the fast interleaved memory applications. A port's burst counter is loaded with the port's Counter Load pin (CNTLD). When the port's Counter Increment (CNTINC) is asserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until CNTINC is deasserted. Depending on the mask register state, the counter can address the entire memory array and will loop back to start. Counter Reset (CNTRST) is used to reset the Burst Counter (the Mask Register value is unaffected). When using the counter in readback mode, the internal address value of the counter will be read back on the address lines when Counter Readback Signal

(CNTRD) is asserted. Figure 1 provides a block diagram of the readback operation. Table 2 lists control signals required for counter operations. The signals are listed based on their priority. For example, Master Reset takes precedence over Counter Reset, and Counter Load has lower priority than Mask Register Load (described below). All counter operations are independent of Chip Enables ($\overline{CE_0}$ and $CE_1$). When the address readback operation is performed the data I/Os are three-stated (if CEs are active) and one-clock cycle (no-operation cycle) latency is experienced. The address will be read at time $t_{CA2}$ from the rising edge of the clock following the no-operation cycle. The read back address can be either of the burst counter or the mask register based on the levels of Counter Read signal (CNTRD) and Mask Register Read signal (MKRD). Both signals are synchronized to the port's clock as shown in Table 2. Counter read has a higher priority than mask read.

**Figure 16. Counter and Mask Register Read Back on Address Lines**
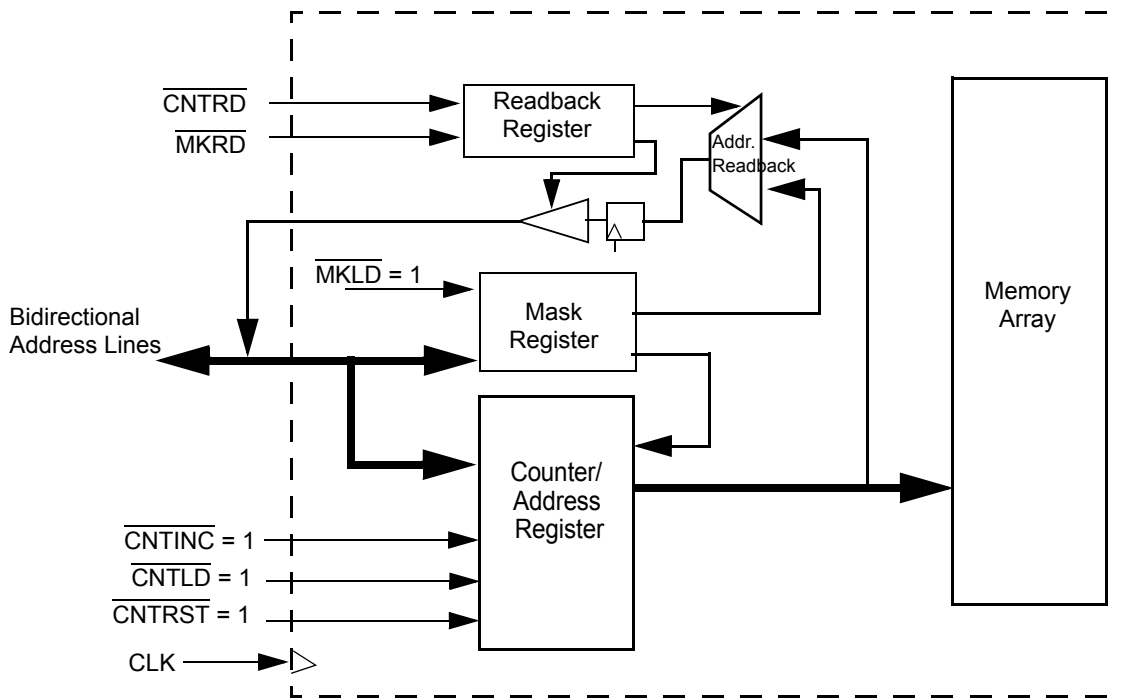
## Counter-Mask Register

**Figure 17. Programmable Counter-Mask Register Operation[53]**
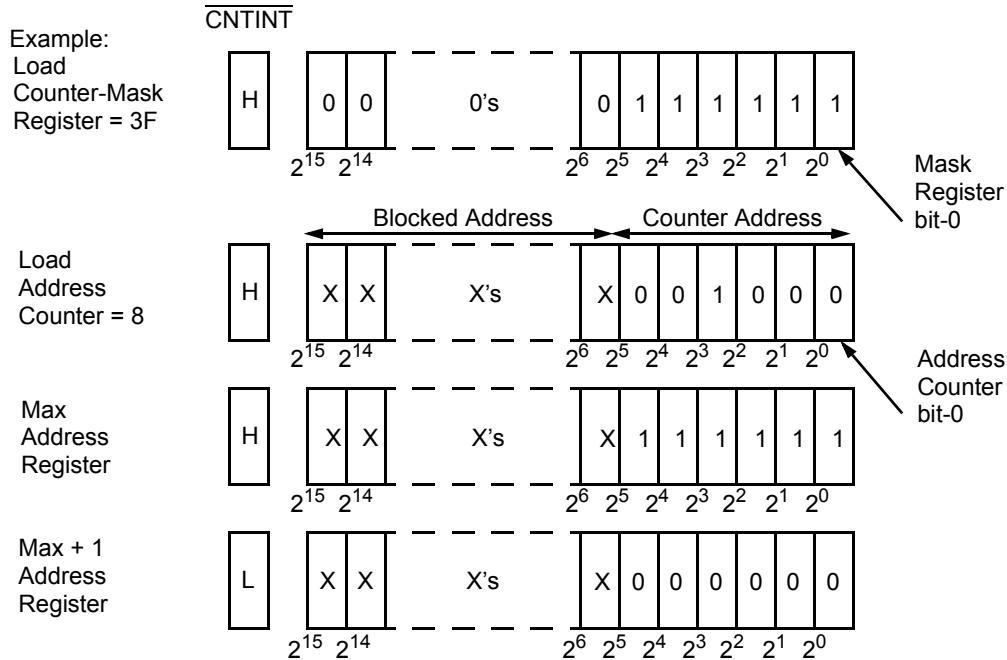


The burst counter has a mask register that controls when and where the counter wraps. An interrupt flag ($\overline{\text{CNTINT}}$) is asserted for one clock cycle when the unmasked portion of the counter address wraps around from all ones ($\overline{\text{CNTINC}}$ must be asserted) to all zeros. The example in Figure 16 shows the counter mask register loaded with a mask value of 003F unmasking the first 6 bits with bit "0" as the LSB and bit "15" as the MSB. The maximum value the mask register can be loaded with is FFFF. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of XXX8. The "blocked" addresses (in this case, the 6th address through the 15th address) are loaded with an address but do not increment once loaded. The counter address will start at address XXX8. With CNTINC asserted LOW, the counter will increment its internal address value till it reaches the mask register value of 3F and wraps around the memory block to location XXX0. Therefore, the counter uses the mask-register to define wrap-around point. The mask register of every port is loaded when MKLD (mask register load) for that port is LOW. When MKRD is LOW, the value of the mask register can be read out on address lines in a manner similar to counter read back operation (see Table 2 on page 26 for required conditions).

When the burst counter is loaded with an address higher than the mask register value, the higher addresses will form the masked portion of the counter address and are called blocked addresses. The blocked addresses will not be changed or affected by the counter increment operation. The only exception is mask register bit 0. It can be masked to allow the address

counter to increment by two. If the mask register bit 0 is loaded with a logic value of "0," then address counter bit 0 is masked and can not be changed during counter increment operation. If the loaded value for address counter bit 0 is "0," the counter will increment by two and the address values are even. If the loaded value for address counter bit 0 is "1," the counter will increment by two and the address values are odd. This operations allows the user to achieve a 36-bit interface using any two ports, where the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 36-bit word in even memory locations, and the other half in odd memory locations. $\overline{\text{CNTINT}}$ will be asserted when the unmasked portion of the counter wraps to all zeros. Loading mask register bit 0 with "1" allows the counter to increment the address value sequentially.

Table 2 on page 26 groups the operations of the mask register with the operations of the address counter. Address counter and mask register signals are all synchronized to the port's clock CLK. Master reset ($\overline{\text{MRST}}$) is the only asynchronous signal listed on Table 2 on page 26. Signals are listed based on their priority going from left column to right column with $\overline{\text{MRST}}$ being the highest. A LOW on $\overline{\text{MRST}}$ will reset both counter register to all zeros and mask register to all ones. On the other hand, a LOW on $\overline{\text{CNTRST}}$ will only clear the address counter register to zeros and the mask register will remain intact.

**Note**
53. The "X" in this diagram represents the counter upper-bits.

There are four operations for the counter and mask register:

1. Load operation: When $\overline{CNTLD}$ or $\overline{MKLD}$ is LOW, the address counter or the mask register is loaded with the address value presented at the address lines. This value ranges from 0 to FFFF (64K). The mask register load operation has a higher priority over the address counter load operation.

2. Increment: Once the address counter is loaded with an external address, the counter can internally increment the address value by asserting CNTINC LOW. The counter can address the entire memory array (depend on the value of the mask register) and loop back to location 0. The increment operation is second in priority to load operation.

3. Readback: the internal value of either the burst counter or the mask register can be read out on the address lines when $\overline{CNTRD}$ or $\overline{MKRD}$ is LOW. Counter readback has higher priority over mask register readback. A no-operation delay cycle is experienced when readback operation is performed. The address will be valid after $t_{CA2}$ (for counter readback) or $t_{CM2}$ (for mask readback) from the following port's clock rising edge. Address readback operation is independent of the port's chip enables ($\overline{CE}_0$ and $CE_1$). If address readback occurs while the port is enabled (chip enables active), the data lines (I/Os) will be three-stated.

4. Hold operation: In order to hold the value of the address counter at certain address, all signals in Table 2 on page 26 have to be HIGH. This operation has the least priority. This operation is useful in many applications where wait states are needed or when address is available few cycles ahead of data.

The counter and mask register operations are totally independent of port chip enables.

# IEEE 1149.1 Serial Boundary Scan (JTAG) and Memory Built-In-Self-Test (MBIST)

The CY7C0430CV incorporate a serial boundary scan test access port (TAP). This port is fully compatible with IEEE Standard 1149.1-2001[54]. The TAP operates using JEDEC standard 3.3 V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard. Memory BIST circuitry will also be controlled through the TAP interface. All MBIST instructions are compliant to the JTAG standard. An external clock (CLKBIST) is provided to allow the user to run BIST at speeds up to 50 MHz. CLKBIST is multiplexed internally with the ports clock during BIST operation.

## Disabling the JTAG Feature

It is possible to operate the QuadPort DSE device without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left unconnected. CLKBIST must be tied LOW to disable the MBIST. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

## Test Access Port (TAP)–Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

## Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

## Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

## Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram (FSM)). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

## Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the QuadPort DSE device and may be performed while the device is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

## TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the QuadPort DSE device test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

## Instruction Register

Four-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the following JTAG/BIST Controller diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

## Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain devices. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the QuadPort DSE device with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

## Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the QuadPort DSE device. The boundary scan register is loaded with the contents of the QuadPort DSE device Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, and SAMPLE/PRELOAD instructions can be used to capture the contents of the Input and Output ring.

## Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the QuadPort DSE device and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

**Note**
54. Master Reset will reset the JTAG controller.

## TAP Instruction Set

Sixteen different instructions are possible with the 4-bit instruction register. All combinations are listed in Table on page 37, Instruction Codes. Seven of these instructions (codes) are listed as RESERVED and should not be used. The other nine instructions are described in detail below.

The TAP controller used in this QuadPort DSE device is fully compatible[55] with the 1149.1 convention. The TAP controller can be used to load address, data or control signals into the QuadPort DSE device and can preload the Input or output buffers. The QuadPort DSE device implements all of the 1149.1 instructions except INTEST. Table lists all instructions.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

### EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST allows circuitry external to the QuadPort DSE device package to be tested. Boundary-scan register cells at output pins are used to apply test stimuli, while those at input pins capture test results.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the identification register. It also places the identification register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

### High-Z

The High-Z instruction causes the bypass register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all QuadPort DSE device outputs into a High-Z state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the QuadPort DSE device clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the QuadPort DSE device signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times. Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins. If the TAP controller goes into the Update-DR state, the sampled data will be updated.

### BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### CLAMP

The optional CLAMP instruction allows the state of the signals driven from QuadPort DSE device pins to be determined from the boundary-scan register while the BYPASS register is selected as the serial path between TDI and TDO. CLAMP controls boundary cells to 1 or 0.

### CYBIST

CYBIST instruction provides the user with a means of running a user-accessible self-test function within the QuadPort DSE device as a result of a single instruction. This permits all components on a board that offer the CYBIST instruction to execute their self-tests concurrently, providing a quick check for the board. The QuadPort DSE device MBIST provides two modes of operation once the TAP controller is loaded with the CYBIST instruction.

**Note**
55. Master Reset will reset the JTAG controller.

## Non Debug Mode (Go-NoGo)

The non-debug mode is a go-nogo test used simply to run BIST and obtain pass-fail information after the test is run. In addition to that, the total number of failures encountered can be obtained. This information is used to aid the debug mode (explained next) of operation. The pass-fail information and failure count is scanned out using the JTAG interface. An MBIST Result Register (MRR) will be used to store the pass-fail results. The MRR is a 25-bit register that will be connected between TDI and TDO during the internal scan (INT_SCAN) operation. The MRR will contain the total number of fail read cycles of the entire MBIST sequence. MRR[0] (bit 0) is the Pass/Fail bit. A "1" indicates some type of failure occurred, and a "0" indicates entire memory pass.

In order to run BIST in non-debug mode, the two-bit MBIST Control Register (MCR) is loaded with the default value "00", and the TAP controller's finite state machine (FSM), which is synchronous to TCK, transitions to Run Test/Idle state. The entire MBIST test will be performed with a deterministic number of TCK cycles depending on the TCK and CLKBIST frequency.

$$t_{CYC} = \frac{t_{CYC}[CLKBIST]}{t_{CYC}[TCK]} \times m + SPC$$

$t_{CYC}$ is total number of TCK cycles required to run MBIST.

*SPC* is the Synchronization Padding Cycles (4–6 cycles).

*m* is a constant represents the number of read and write operations required to run MBIST algorithms (31195136).

Once the entire MBIST sequence is completed, supplying extra TCK or CLKBIST cycles will have no effect on the MBIST controller state or the pass-fail status.

## Debug Mode

With the CYBIST instruction loaded and the MCR loaded with the value of "01," and the FSM transitions to RUN_TEST/IDLE state, the MBIST goes into CYBIST-debug mode. The debug mode will be used to provide complete failure analysis information at the board level. It is recommended that the user runs the non-debug mode first and then the debug mode in order to save test time and to set an upper bound on the number of scan outs that will be needed. The failure data will be scanned out automatically once a failure occurs using the JTAG TAP interface. The failure data will be represented by a 100-bit packet given below. The 100-bit Memory Debug Register (MDR) will be connected between TDI and TDO, and will be shifted out on TDO, which is synchronized to TCK.

Figure 18 on page 34 is a representation of the 100-bit MDR packet. The packet follows a two-bit header that has a logic "1" value, and represents two TCK cycles. MDR[97:26] represent the BIST comparator values of all four ports (each port has 18 data lines). A value of "1" indicates a bit failure. The scanned out data is from LSB to MSB. MDR[25:10] represent the failing address (MSB to LSB). The state of the BIST controller is scanned out using MDR[9:4]. Bit 2 is the Test Done bit. A "0" in bit 2 means test not complete. The user has to monitor this bit at every packet to determine if more failure packets need to be scanned out at the end of the BIST operations. If the value is "0" then BIST must be repeated to capture the next failing packet. If it is "1," it means that the last failing packets have been scanned out. A trailer similar to the header represents the end of a packet.

## MCR_SCAN

This instruction will connect the Memory BIST Control Register (MCR) between TDI and TDO. The default value (upon master reset) is "00." Shift_DR state will allow modifying the MCR to extend the MBIST functionality.

## MBIST Control States

Thirty-five states are listed in Table  on page 38. Four data algorithms are used in debug mode: moving inversion (MIA), march_2 (M2A), checkerboard (CBA), and unique address algorithm (UAA). Only Port 1 can write MIA, M2A, and CBA data to the memory. All four ports can read any algorithm data from the QuadPort DSE device memory. Ports 2, 3, and 4 will only write UAA data.

## Boundary Scan Cells (BSC)

Table  on page 40 lists all QuadPort DSE family I/Os with their associated BSC. Note that the cells have even numbers. Every I/O has two boundary scan cells. Bidirectional signals (address lines, datalines) require two cells so that one (the odd cell) is used to control a three-state buffer. Input only and output only signals have an extra dummy cell (odd cells) that are used to ease device layout.

**Figure 18.  MBIST Debug Register Packet**

```
99    98
┌───┬───┐
│ 1 │ 1 │
└───┴───┘

 97                                                              62
┌─────────────┬─────────────┬─────────────┬─────────────┐
│P4_IO(17-9)  │P3_IO(17-9)  │P2_IO(17-9)  │P1_IO(17-9)  │
└─────────────┴─────────────┴─────────────┴─────────────┘

 61                                                              26
┌─────────────┬─────────────┬─────────────┬─────────────┐
│P4_IO(8-0)   │P3_IO(8-0)   │P2_IO(8-0)   │P1_IO(8-0)   │
└─────────────┴─────────────┴─────────────┴─────────────┘

 25          10
┌─────────────┐
│ A(15-0)     │
└─────────────┘

 9           4
┌─────────────┐
│ MBIST_State │
└─────────────┘

 3
┌─────┐
│P/F  │
└─────┘

 2
┌─────┐
│TD   │
└─────┘

 1    0
┌───┬───┐
│ 1 │ 1 │
└───┴───┘
```
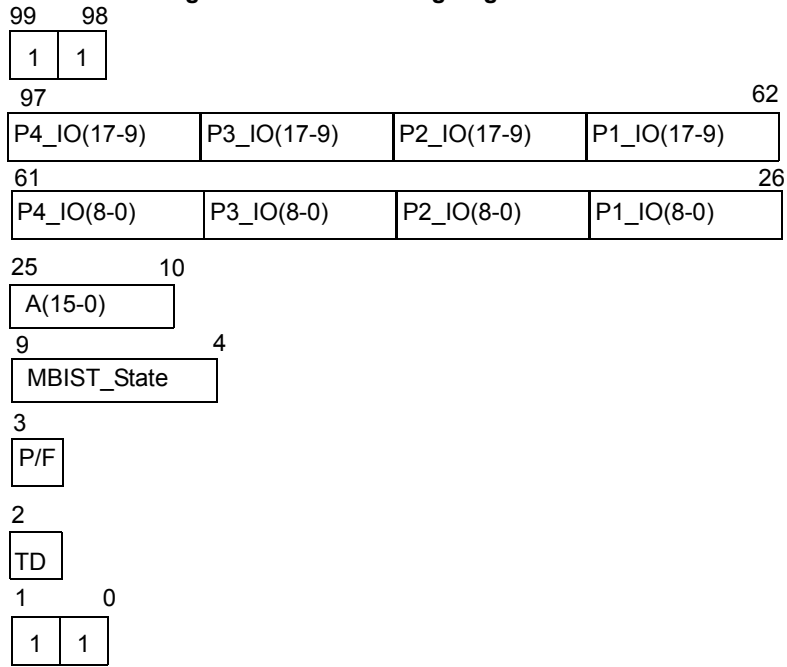
## TAP Controller State Diagram (FSM)[56]
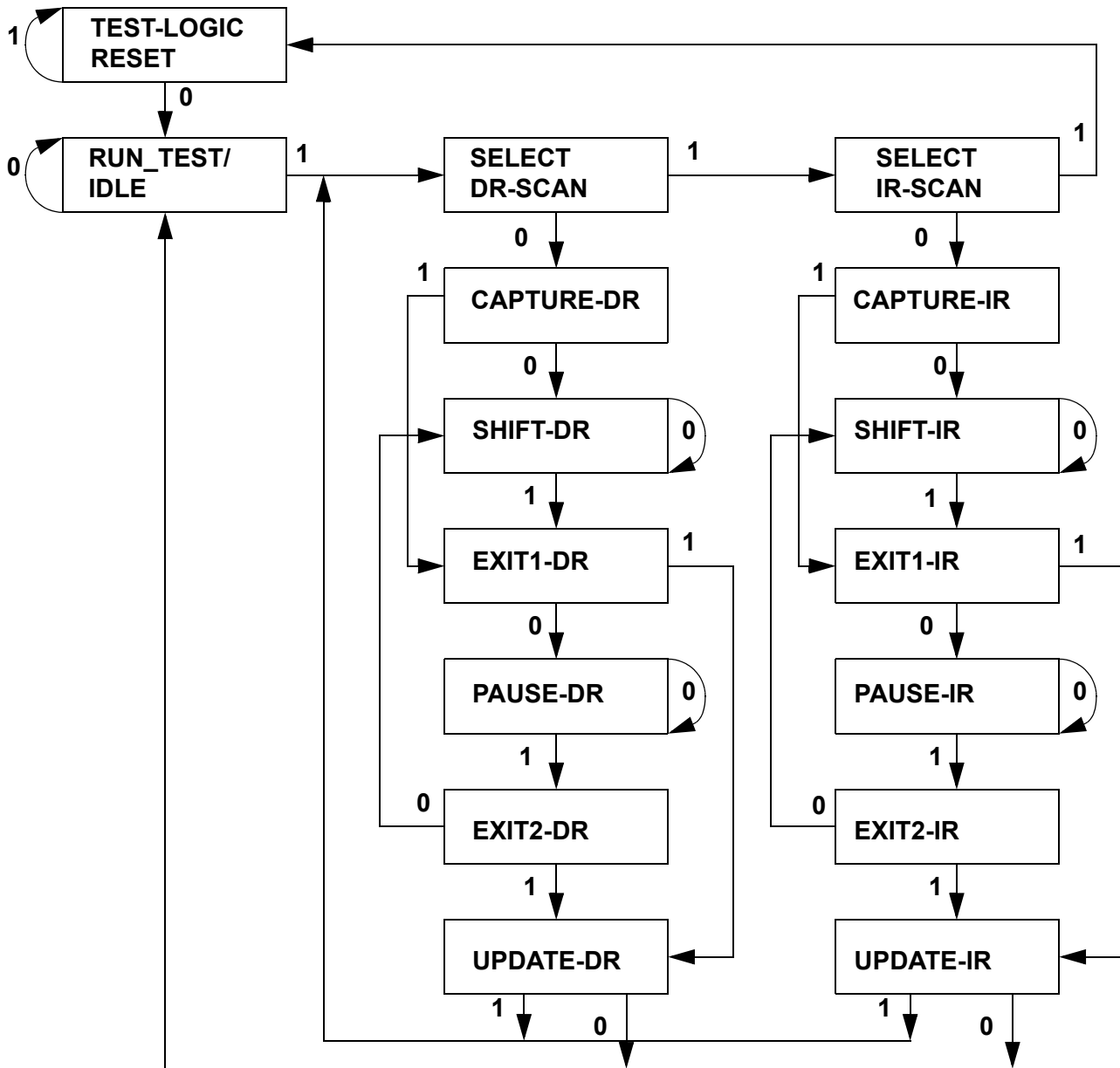


**Note**
56. The "0"/"1" next to each state represents the value at TMS at the rising edge of TCK.

## JTAG/BIST TAP Controller Block Diagram

## Identification Register Definitions

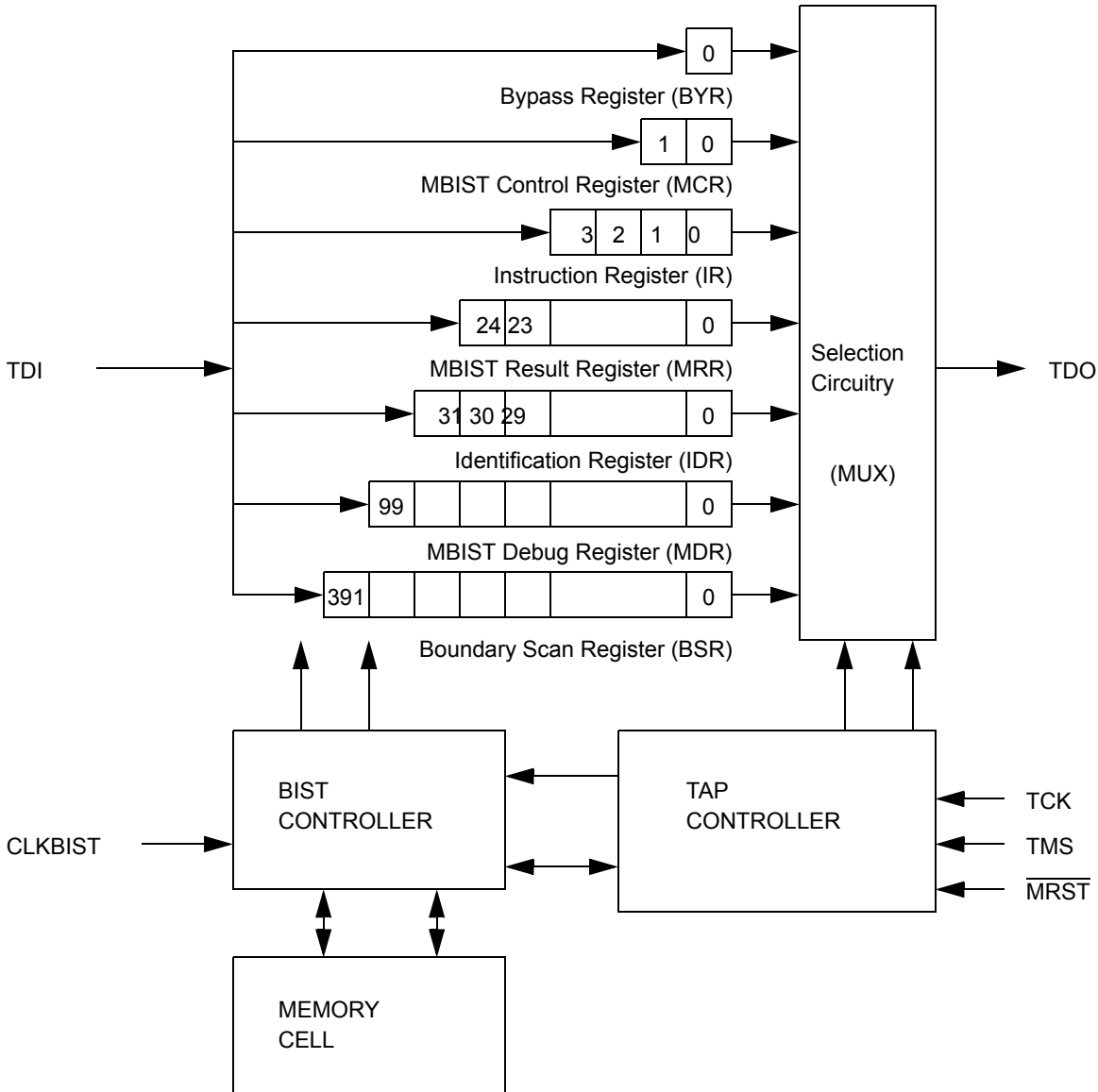| Instruction Field | Value | Description |
|---|---|---|
| Revision Number (31:28) | 1h | Reserved for version number |
| Cypress Device ID (27:12) | C000h | Defines Cypress part number |
| Cypress JEDEC ID (11:1) | 34h | Allows unique identification of QuadPort DSE device vendor |
| ID Register Presence (0) | 1 | Indicate the presence of an ID register |

## Scan Registers Sizes

| Register Name | Bit Size |
|---|---|
| Instruction (IR) | 4 |
| Bypass (BYR) | 1 |
| Identification (IDR) | 32 |
| MBIST Control (MCR) | 2 |
| MBIST Result (MRR) | 25 |
| MBIST Debug (MDR) | 100 |
| Boundary Scan (BSR) | 392 |

## Instruction Identification Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 0000 | **Captures the Input/Output ring contents**. Places the boundary scan register (BSR) between the TDI and TDO. |
| BYPASS | 1111 | **Places the bypass register (BYR) between TDI and TDO**. |
| IDCODE | 0111 | **Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO**. |
| HIGHZ | 0110 | **Places the BYR between TDI and TDO**. Forces all QuadPort DSE device output drivers to a High-Z state. |
| CLAMP | 0101 | **Controls boundary to 1/0**. Uses BYR. |
| SAMPLE/PRELOAD | 0001 | **Captures the Input/Output ring contents**. Places the boundary scan register (BSR) between TDI and TDO. |
| CYBIST | 1000 | **Invokes MBIST**. Places the MBIST Debug register (MDR) between TDI and TDO. |
| INT_SCAN | 0010 | **Scans out pass-fail information**. Places MBIST Result Register (MRR) between TDI and TDO. |
| MCR_SCAN | 0011 | **Presets CYBIST mode**. Places MBIST Control Register (MCR) between TDI and TDO. |
| RESERVED | All other codes | **Seven combinations are reserved**. Do not use other than the above. |

## MBIST Control States

| States Code | State Name | Description |
|---|---|---|
| 000001 | movi_zeros | Port 1 write all zeros to the QuadPort DSE device memory using Moving Inversion Algorithm (MIA). |
| 000011 | movi_1_upcnt | Up count from 0 to 64K (depth of QuadPort DSE device). All ports read 0s, then Port 1 writes 1s to all memory locations using MIA, then all ports read 1s. MIA read0_write1_read1 (MIA_r0w1r1). |
| 000010 | movi_0_upcnt | Up count from 0 to 64K. All ports read 1s, then Port 1 writes 0s, then all ports read 0s (MIA_r1w0r0). |
| 000110 | movi_1_downcnt | Down count from 64K to 0. MIA_r0w1r1. |
| 000111 | movi_0_downcnt | Down count MIA_r1w0r0. |
| 000101 | movi_read | Read all 0s. |
| | | |
| 000100 | mar2_zeros | Port 1 write all zeros to memory using March2 Algorithm (M2A). |
| 001100 | mar2_1_upcnt | Up count M2A_r0w1r1. |
| 001101 | mar2_0_upcnt | Up count M2A_r1w0r0. |
| 001111 | mar2_1_downcnt | Down count M2A_r0w1r1. |
| 001110 | mar2_0_downcnt | Down count M2A_r1w0r0. |
| 001010 | mar2_read | Read all 0s. |
| | | |
| 001011 | chkr_w | Port 1 writes topological checkerboard data to memory. |
| 001001 | chkr_r | All ports read topological checkerboard data. |
| 001000 | n_chkr_w | Port 1 write inverse topological checkerboard data. |
| 011000 | n_chkr_r | All ports read inverse topological checkerboard data. |
| | | |
| 011001 | uaddr_zeros2 | Port 2 write all zeros to memory using Unique Address Algorithm (UAA). |
| 011011 | uaddr_write2 | Port 2 writes every address value into its memory location (UAA). |
| 011010 | uaddr_read2 | All ports read UAA data. |
| 011110 | uaddr_ones2 | Port 2 writes all ones to memory. |
| 011111 | n_uaddr_write2 | Port 2 writes inverse address value into memory. |
| 011101 | n_uaddr_read2 | All ports read inverse UAA data. |
| | | |
| 011001 | uaddr_zeros3 | Port 3 write all zeros to memory using Unique Address Algorithm (UAA). |
| 011011 | uaddr_write3 | Port 3 writes every address value into its memory location (UAA). |
| 011010 | uaddr_read3 | All ports read UAA data. |
| 011110 | uaddr_ones3 | Port 3 writes all ones to memory. |
| 011111 | n_uaddr_write3 | Port 3 writes inverse address value into memory. |
| 011101 | n_uaddr_read3 | All ports read inverse UAA data. |
| | | |
| 011001 | uaddr_zeros4 | Port 4 write all zeros to memory using Unique Address Algorithm (UAA). |
| 011011 | uaddr_write4 | Port 4 writes every address value into its memory location (UAA). |
| 011010 | uaddr_read4 | All ports read UAA data. |
| 011110 | uaddr_ones4 | Port 4 writes all ones to memory. |
| 011111 | n_uaddr_write4 | Port 4 writes inverse address value into memory. |
| 011101 | n_uaddr_read4 | All ports read inverse UAA data. |
| | | |
| 110010 | complete | Test complete. |

## MBIST Control Register (MCR)

| MCR[1:0] | Mode |
|---|---|
| 00 | Non-Debug |
| 01 | Debug |
| 10 | Reserved |
| 11 | Reserved |

## Boundary Scan Order

| Cell # | Signal Name | Bump (Ball) ID |
|---|---|---|
| 2 | A0_P4 | K20 |
| 4 | A1_P4 | J19 |
| 6 | A2_P4 | J18 |
| 8 | A3_P4 | H20 |
| 10 | A4_P4 | H19 |
| 12 | A5_P4 | G19 |
| 14 | A6_P4 | G18 |
| 16 | A7_P4 | F20 |
| 18 | A8_P4 | F19 |
| 20 | A9_P4 | F18 |
| 22 | A10_P4 | E20 |
| 24 | A11_P4 | E19 |
| 26 | A12_P4 | D19 |
| 28 | A13_P4 | D18 |
| 30 | A14_P4 | C20 |
| 32 | A15_P4 | C19 |
| 34 | $\overline{\text{CNTINT}}$_P4 | F17 |
| 36 | CNTRST_P4 | K18 |
| 38 | $\overline{\text{MKLD}}$_P4 | H18 |
| 40 | $\overline{\text{CNTLD}}$_P4 | H17 |
| 42 | $\overline{\text{CNTINC}}$_P4 | G17 |
| 44 | $\overline{\text{CNTRD}}$_P4 | E17 |
| 46 | $\overline{\text{MKRD}}$_P4 | E18 |
| 48 | $\overline{\text{LB}}$_P4 | A20 |
| 50 | $\overline{\text{UB}}$_P4 | B19 |
| 52 | $\overline{\text{OE}}$_P4 | D17 |
| 54 | R/$\overline{\text{W}}$_P4 | C16 |
| 56 | $\overline{\text{CE1}}$_P4 | C18 |
| 58 | $\overline{\text{CE0}}$_P4 | C17 |
| 60 | $\overline{\text{INT}}$_P4 | K19 |
| 62 | CLK_P4 | K17 |
| 64 | A0_P3 | L20 |
| 66 | A1_P3 | M19 |
| 68 | A2_P3 | M18 |
| 70 | A3_P3 | N20 |
| 72 | A4_P3 | N19 |
| 74 | A5_P3 | P19 |
| 76 | A6_P3 | P18 |
| 78 | A7_P3 | R20 |
| 80 | A8_P3 | R19 |
| 82 | A9_P3 | R18 |

## Boundary Scan Order (continued)

| Cell # | Signal Name | Bump (Ball) ID |
|---|---|---|
| 84 | A10_P3 | T20 |
| 86 | A11_P3 | T19 |
| 88 | A12_P3 | U19 |
| 90 | A13_P3 | U18 |
| 92 | A14_P3 | V20 |
| 94 | A15_P3 | V19 |
| 96 | $\overline{\text{CNTINT}}$_P3 | R17 |
| 98 | $\overline{\text{CNTRST}}$_P3 | L18 |
| 100 | $\overline{\text{MKLD}}$_P3 | N18 |
| 102 | $\overline{\text{CNTLD}}$_P3 | N17 |
| 104 | $\overline{\text{CNTINC}}$_P3 | P17 |
| 106 | $\overline{\text{CNTRD}}$_P3 | T17 |
| 108 | $\overline{\text{MKRD}}$_P3 | T18 |
| 110 | $\overline{\text{LB}}$_P3 | Y20 |
| 112 | $\overline{\text{UB}}$_P3 | W19 |
| 114 | $\overline{\text{OE}}$_P3 | U17 |
| 116 | R/$\overline{\text{W}}$_P3 | V16 |
| 118 | $\overline{\text{CE1}}$_P3 | V18 |
| 120 | $\overline{\text{CE0}}$_P3 | V17 |
| 122 | $\overline{\text{INT}}$_P3 | L19 |
| 124 | CLK_P3 | M17 |
| 126 | IO0_P4 | Y15 |
| 128 | IO1_P4 | W15 |
| 130 | IO2_P4 | Y16 |
| 132 | IO3_P4 | W16 |
| 134 | IO4_P4 | Y17 |
| 136 | IO5_P4 | W17 |
| 138 | IO6_P4 | Y18 |
| 140 | IO7_P4 | W18 |
| 142 | IO8_P4 | Y19 |
| 144 | IO0_P3 | V12 |
| 146 | IO1_P3 | Y11 |
| 148 | IO2_P3 | W12 |
| 150 | IO3_P3 | Y12 |
| 152 | IO4_P3 | W13 |
| 154 | IO5_P3 | Y13 |
| 156 | IO6_P3 | V15 |
| 158 | IO7_P3 | Y14 |
| 160 | IO8_P3 | W14 |
| 162 | IO0_P1 | Y6 |
| 164 | IO1_P1 | W6 |
| 166 | IO2_P1 | Y5 |

## Boundary Scan Order (continued)

| Cell # | Signal Name | Bump (Ball) ID |
|--------|-------------|----------------|
| 168 | IO3_P1 | W5 |
| 170 | IO4_P1 | Y4 |
| 172 | IO5_P1 | W4 |
| 174 | IO6_P1 | Y3 |
| 176 | IO7_P1 | W3 |
| 178 | IO8_P1 | Y2 |
| 180 | IO0_P2 | V9 |
| 182 | IO1_P2 | Y10 |
| 184 | IO2_P2 | W9 |
| 186 | IO3_P2 | Y9 |
| 188 | IO4_P2 | W8 |
| 190 | IO5_P2 | Y8 |
| 192 | IO6_P2 | V6 |
| 194 | IO7_P2 | Y7 |
| 196 | IO8_P2 | W7 |
| 198 | A0_P2 | L1 |
| 200 | A1_P2 | M2 |
| 202 | A2_P2 | M3 |
| 204 | A3_P2 | N1 |
| 206 | A4_P2 | N2 |
| 208 | A5_P2 | P2 |
| 210 | A6_P2 | P3 |
| 212 | A7_P2 | R1 |
| 214 | A8_P2 | R2 |
| 216 | A9_P2 | R3 |
| 218 | A10_P2 | T1 |
| 220 | A11_P2 | T2 |
| 222 | A12_P2 | U2 |
| 224 | A13_P2 | U3 |
| 226 | A14_P2 | V1 |
| 228 | A15_P2 | V2 |
| 230 | $\overline{\text{CNTINT}}$_P2 | R4 |
| 232 | $\overline{\text{CNTRST}}$_P2 | L3 |
| 234 | $\overline{\text{MKLD}}$_P2 | N3 |
| 236 | $\overline{\text{CNTLD}}$_P2 | N4 |
| 238 | $\overline{\text{CNTINC}}$_P2 | P4 |
| 240 | $\overline{\text{CNTRD}}$_P2 | T4 |
| 242 | $\overline{\text{MKRD}}$_P2 | T3 |
| 244 | $\overline{\text{LB}}$_P2 | Y1 |
| 246 | $\overline{\text{UB}}$_P2 | W2 |
| 248 | $\overline{\text{OE}}$_P2 | U4 |
| 250 | R/$\overline{\text{W}}$_P2 | V5 |

## Boundary Scan Order (continued)

| Cell # | Signal Name | Bump (Ball) ID |
|--------|-------------|----------------|
| 252 | CE1_P2 | V3 |
| 254 | $\overline{\text{CE0}}$_P2 | V4 |
| 256 | $\overline{\text{INT}}$_P2 | L2 |
| 258 | CLK_P2 | M4 |
| 260 | A0_P1 | K1 |
| 262 | A1_P1 | J2 |
| 264 | A2_P1 | J3 |
| 266 | A3_P1 | H1 |
| 268 | A4_P1 | H2 |
| 270 | A5_P1 | G2 |
| 272 | A6_P1 | G3 |
| 274 | A7_P1 | F1 |
| 276 | A8_P1 | F2 |
| 278 | A9_P1 | F3 |
| 280 | A10_P1 | E1 |
| 282 | A11_P1 | E2 |
| 284 | A12_P1 | D2 |
| 286 | A13_P1 | D3 |
| 288 | A14_P1 | C1 |
| 290 | A15_P1 | C2 |
| 292 | $\overline{\text{CNTINT}}$_P1 | F4 |
| 294 | $\overline{\text{CNTRST}}$_P1 | K3 |
| 296 | $\overline{\text{MKLD}}$_P1 | H3 |
| 298 | $\overline{\text{CNTLD}}$_P1 | H4 |
| 300 | $\overline{\text{CNTINC}}$_P1 | G4 |
| 302 | $\overline{\text{CNTRD}}$_P1 | E4 |
| 304 | $\overline{\text{MKRD}}$_P1 | E3 |
| 306 | $\overline{\text{LB}}$_P1 | A1 |
| 308 | $\overline{\text{UB}}$_P1 | B2 |
| 310 | $\overline{\text{OE}}$_P1 | D4 |
| 312 | R/$\overline{\text{W}}$_P1 | C5 |
| 314 | CE1_P1 | C3 |
| 316 | $\overline{\text{CE0}}$_P1 | C4 |
| 318 | $\overline{\text{INT}}$_P1 | K2 |
| 320 | CLK_P1 | K4 |
| 322 | IO9_P2 | A6 |
| 324 | IO10_P2 | B6 |
| 326 | IO11_P2 | A5 |
| 328 | IO12_P2 | B5 |
| 330 | IO13_P2 | A4 |
| 332 | IO14_P2 | B4 |
| 334 | IO15_P2 | A3 |

## Boundary Scan Order (continued)

| Cell # | Signal Name | Bump (Ball) ID |
|--------|-------------|----------------|
| 336 | IO16_P2 | B3 |
| 338 | IO17_P2 | A2 |
| 340 | IO9_P1 | C9 |
| 342 | IO10_P1 | A10 |
| 344 | IO11_P1 | B9 |
| 346 | IO12_P1 | A9 |
| 348 | IO13_P1 | B8 |
| 350 | IO14_P1 | A8 |
| 352 | IO15_P1 | C6 |
| 354 | IO16_P1 | A7 |
| 356 | IO17_P1 | B7 |
| 358 | IO9_P3 | A15 |
| 360 | IO10_P3 | B15 |
| 362 | IO11_P3 | A16 |
| 364 | IO12_P3 | B16 |
| 366 | IO13_P3 | A17 |
| 368 | IO14_P3 | B17 |
| 370 | IO15_P3 | A18 |
| 372 | IO16_P3 | B18 |
| 374 | IO17_P3 | A19 |
| 376 | IO9_P4 | C12 |
| 378 | IO10_P4 | A11 |
| 380 | IO11_P4 | B12 |
| 382 | IO12_P4 | A12 |
| 384 | IO13_P4 | B13 |
| 386 | IO14_P4 | A13 |
| 388 | IO15_P4 | C15 |
| 390 | IO16_P4 | A14 |
| 392 | IO17_P4 | B14 |

## Ordering Information

**10 Gb/s 3.3 V QuadPort DSE Family 1 Mb (64K × 18)**

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 133 | CY7C0430CV-133BGI | BG272 | 272-ball BGA | Industrial |

### Ordering Code Definitions

CY 7 C 0430CV - 133 BG I

Temperature Range:
I = Industrial
Package Type:
BG = 272-ball BGA
Speed: 133 MHz
Part Identifier
Technology Code: C = CMOS
Marketing Code: 7 = SRAM
Company ID: CY = Cypress
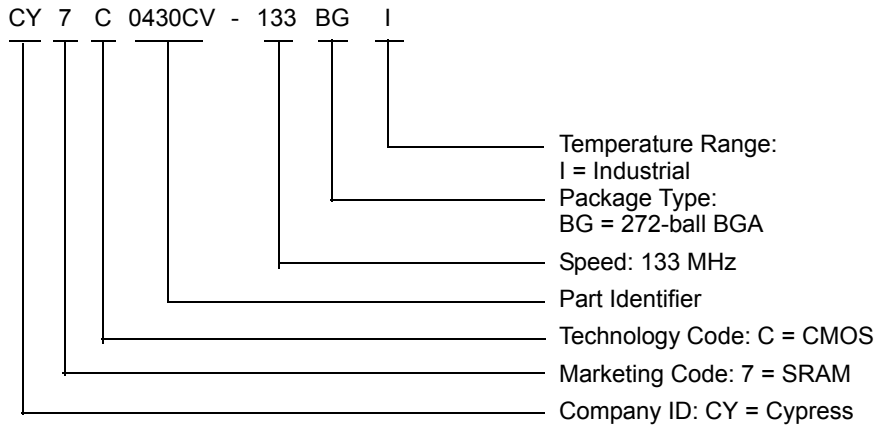
## Package Diagram

**Figure 19.  272-ball PBGA (27 × 27 × 2.33 mm) BG272**
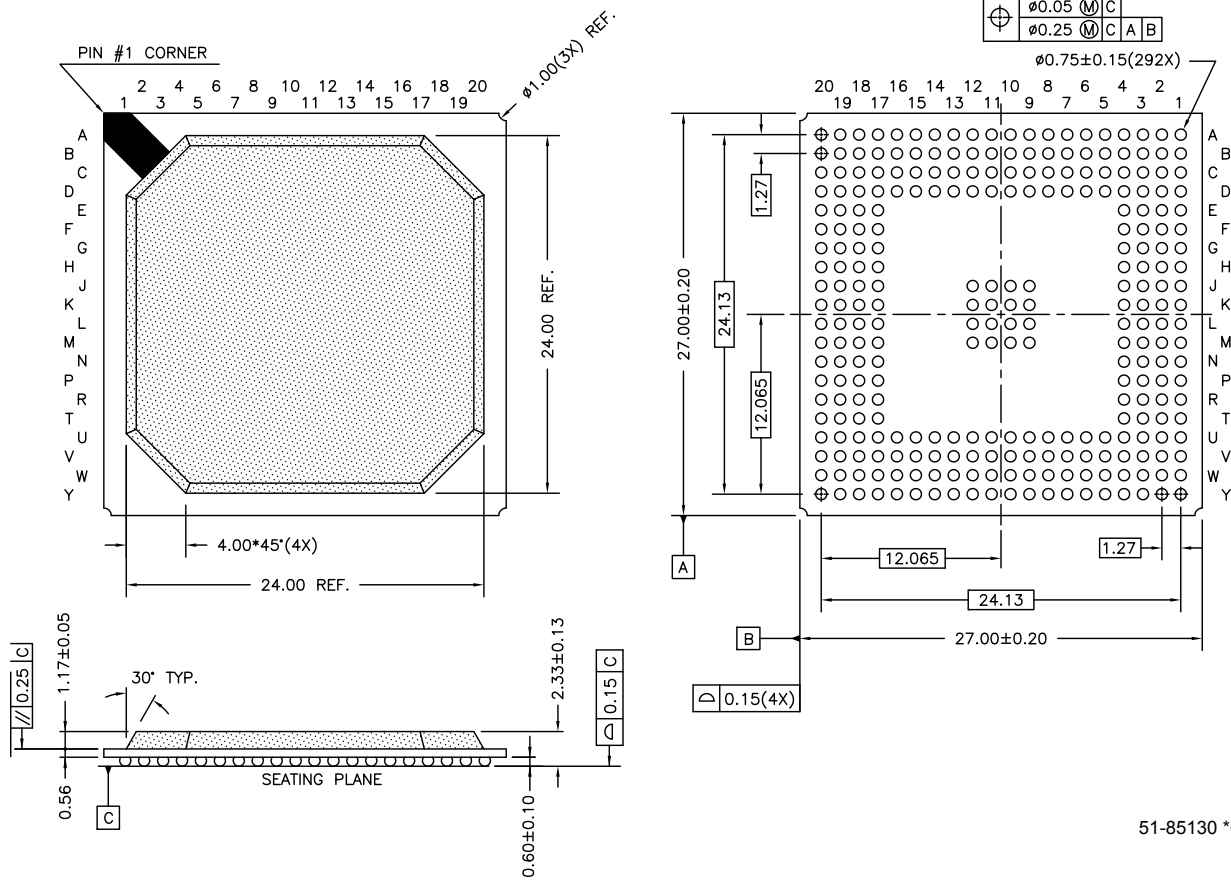


51-85130 *C

## Document History Page

**Document Title: CY7C0430CV, 10 Gb/s 3.3 V QuadPort™ DSE Family**
**Document Number: 38-06027**

| Revision | ECN | Submission Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| ** | 109906 | 09/10/01 | SZV | Change from Spec number: 38-01052 to 38-06027 |
| *A | 115042 | 05/23/02 | FSG | Remove Preliminary, TM from DSE<br>Change RUNBIST to CYBIST<br>Updated ISB values<br>Added notes 7 and 9<br>Increased commercial prime bin to 135 MHz |
| *B | 464083 | See ECN | YDT | Part numbers updated to reflect the recent die revisions<br>Removed 1/2M and 1/4M parts<br>Changed title of data sheet |
| *C | 2897887 | 03/23/2010 | RAME | Updated Ordering Information<br>Updated Package Diagram |
| *D | 3352352 | 08/23/2011 | ADMU | Updated template.<br>Removed CY7C0430BV and -100 speed bin information. |
| *E | 3724728 | 08/27/2012 | SMCH | Fixed minor grammar and typo errors.<br>Updated package diagram. |
| *F | 4083061 | 07/31/2013 | SMCH | Updated Features:<br>Updated dimension of 272-ball BGA package.<br>Removed COmmercial Temperature Range information.<br><br>Updated Pin Definitions:<br>Updated description of $CLK_{P1}$ pin.<br><br>Updated Operating Range:<br>Removed COmmercial Temperature Range information.<br><br>Updated Switching Waveforms:<br>Updated Figure 4, Figure 6, Figure 7.<br><br>Completing Sunset Review.<br><br>Updated in new template. |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc |
| | cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

### PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

### Cypress Developer Community

Community | Forums | Blogs | Video | Training

### Technical Support

cypress.com/go/support