1.1 Scope.

This specification covers the detail requirements for complete 8-bit and 10-bit resolution A/D converters with full microprocessor interface.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD673SD/883B
−2	AD573SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-20.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to Digital Common	+7V
V_{EE} to Digital Common	−16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V_{CC}
Digital Outputs (High Impedance State)	0 to V_{CC}
Power Dissipation	800mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10sec)	300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W
θ_{JA} = 85°C/W

AD573/AD673—SPECIFICATIONS

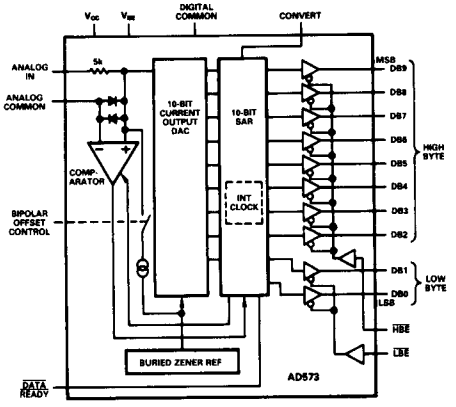
Table 1.

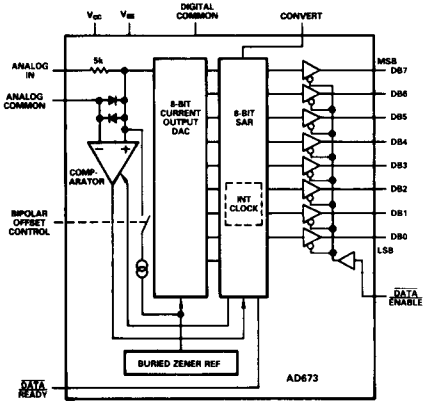
Test	Symbol	Device[2]	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Relative Accuracy	RA	−1	0.195	0.195	0.195		Unipolar and Bipolar Major Transitions ±3 Codes	±% of FS max
		−2	0.098	0.195	0.098	0.098		
Differential Nonlinearity[3]	DNL	−1	8	8	8		All codes test Unipolar and Bipolar	Bits min
		−2	10	8	10	10		
Full-Scale Error[4]	A_E	−1, 2	40	40			Unipolar	±mV max
		−1, 2	20	20			Bipolar	±mV max
Full-Scale Temperature Drift	TCA_E	−1	0.781		0.781			±% of FS max
		−2	0.488		0.488			
Offset Error	V_{OS}	−1	20	20			First Transition	±mV max
		−2	10	20		10		
Offset Temperature Drift	TCV_{OS}	−1	0.391		0.391			±% of FS max
		−2	0.195		0.195			
Bipolar Zero Error	B_{PZE}	−1	20	20			Low Side MSB Transition Bipolar	±mV max
		−2	10	20		10		
Bipolar Zero Temperature Drift	TCB_{PZE}	−1	0.391		0.391		Low Side MSB Transition Bipolar	±% of FS max
		−2	0.195		0.195			
Input Resistance	R_{IN}	−1, 2	3	3	3			kΩ min
			7	7	7			kΩ max
Conversion Time[5]	t_C	−1, 2	10	10	10			μs min
			30	30	30			μs max
Three-State Leakage Current	I_{OLT}	−1	40	40	40		V_{OH} = 5.0V V_{OL} = 0.0V, DB0-DB7	±μA max
		−2	40	40	40		V_{OH} = 5.0V V_{OL} = 0.0V, DB0-DB9	
Power Supply Rejection Ratio	PSRR	−1	78.1	78.1	78.1		V_{CC} = 5V, −15.75V≤V_{EE}≤−14.25V V_{CC} = 5V, −12.6V≤V_{EE}≤−11.4V	±mV max
		−2	19.5	78.1	78.1	19.5	V_{EE} = −15V, 4.5V≤V_{CC}≤5.5V	
Power Supply Current	I_{CC}	−1, 2	15	15			$\overline{DR}$ LOW	+mA max
			15	15			$\overline{DR}$ HIGH (During Conversion)	
	I_{EE}	−1, 2	15	15				−mA max
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0	2.0		Convert, $\overline{HBE}$, $\overline{LBE}$, $\overline{DE}$	+V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8		Convert, $\overline{HBE}$, $\overline{LBE}$, $\overline{DE}$	+V max
Digital Input High Current	I_{IH}	−1, 2	100	100	100		Convert, $\overline{HBE}$, $\overline{LBE}$, $\overline{DE}$ V_{IH} = 5.0V	±μA max
Digital Input Low Current	I_{IL}	−1, 2	100	100	100		Convert, $\overline{HBE}$, $\overline{LBE}$, $\overline{DE}$ V_{IL} = 0.0V	±μA max
Digital Output Low Voltage	V_{OL}	−1	0.4	0.4	0.4		I_{OL} = +3.2mA, $\overline{DR}$, DB0-DB7	+V max
		−2	0.4	0.4	0.4		I_{OL} = +3.2mA $\overline{DR}$, DB0-DB9	
Digital Output High Voltage	V_{OH}	−1	2.4	2.4	2.4		I_{OH} = −0.5mA, DB0-DB7	+V min
		−2	2.4	2.4	2.4		I_{OH} = −0.5mA, DB0-DB9	

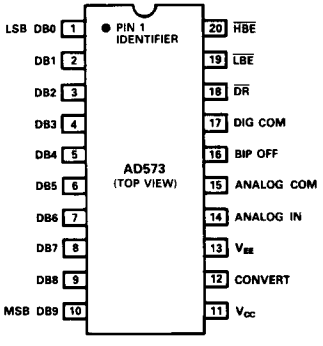
Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Convert Pulse Width[5]	t_{CS}	−1, 2	500		500	500		ns min
DR Delay Convert[5]	t_{DSC}	−1, 2	1.5			1.5		µs max
Data Valid After $\overline{DE}$, $\overline{HBE}$ or $\overline{LBE}$ High[6]	t_{HD}	−1, 2	50					ns min
Output Float Delay[6]	t_{HL}	−1, 2	200			200		ns max
Data Access Time[6]	t_{DD}	−1, 2	250			250		ns max

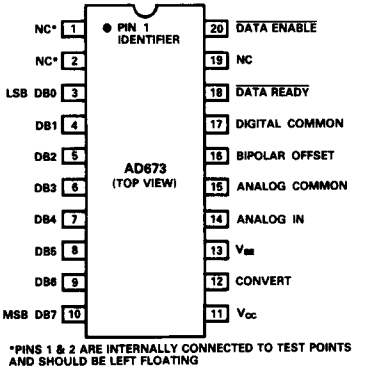
NOTES
[1]V_{CC} = + 5V, V_{EE} = − 15V, analog input through 15Ω resistor to Pin 13, Unipolar configuration.
T_A = 25°C unless otherwise indicated.
Unipolar configuration Pin 16 (Bipolar Offset Control) is grounded.
Bipolar configuration Pin 16 is not connected.
[2]For − 1 (8-Bit resolution Device), 0.391% of full scale = 1 LSB (least significant bit). For − 2 (10-Bit resolution device), 0.098% of full scale = 1 LSB.
[3]Minimum resolution for which no missing codes are guaranteed.
[4]− 1 device full scale error guaranteed trimmable with 50Ω potentiometer.
− 2 device full scale error guaranteed trimmable with 200Ω potentiometer.
[5]See Figure 1.
[6]See Figures 2 and 3.

3.2.1 Functional Block Diagram and Terminal Assignments.









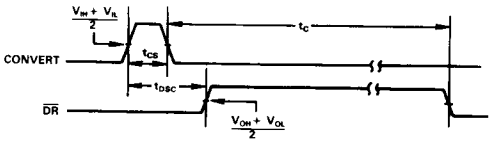


Figure 1. AD573 and AD673 CONVERT Timing

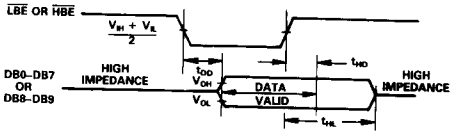


Figure 2. AD573 READ Timing

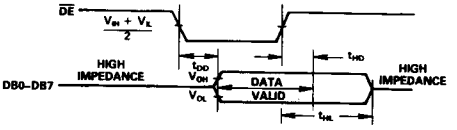


Figure 3. AD673 READ Timing

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).