CRYSTAL
A Cirrus Logic Company

CS6158A

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, and Clock and Data Recovery Functions
- Internal Generation of Transmitted Pulse Width and Pulse Shape
- Low Power Consumption (typically 175 mW)
- Minimum External Components (no external crystal required)
- 14 dB of Transmitter Return Loss

General Description

The CS6158A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply.

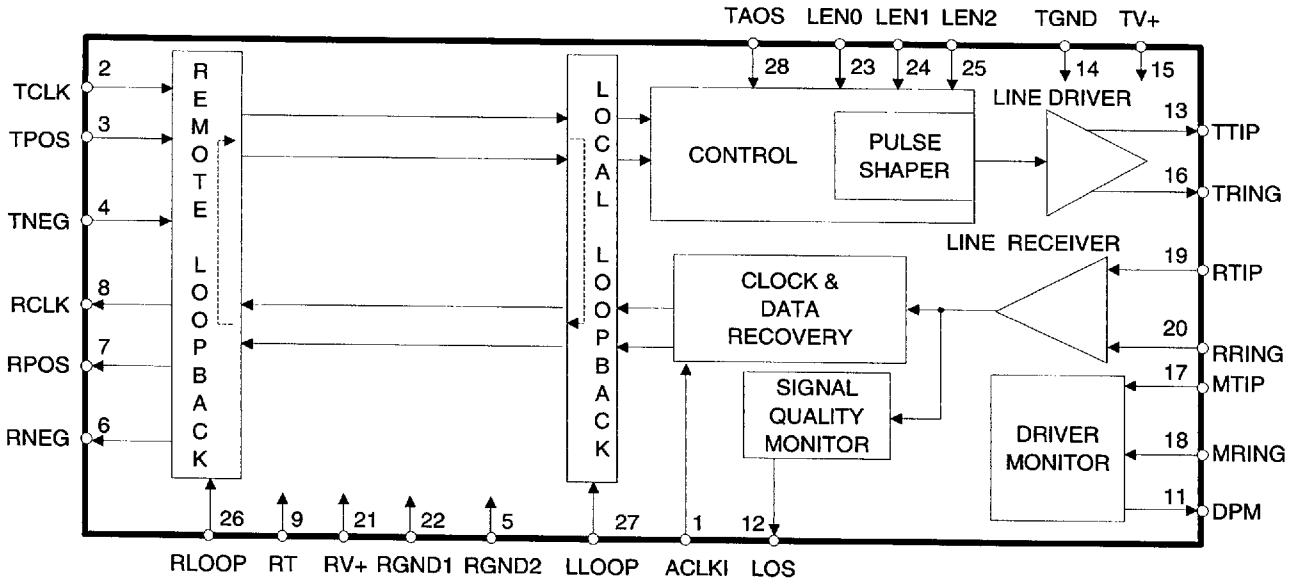
The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from an external reference to provide excellent stability and jitter tolerance. The transmitter features internal pulse shaping. The CS6158A provides a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Applications

- Central Office Exchnges
- Digital Access and Cross Connect Systems
- Large PABX's

ORDERING INFORMATION

CS6158A-IP1	28 Pin Plastic DIP
CS6158A-IL1	28 Pin Plastic PLCC



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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (referenced to GND)		RV+	-	6.0	V
		TV+	-	(RV+) + 0.3	V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND - 0.3	(RV+) + 0.3	
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 4, 5)	P_C	-	290	350	mW
Power Consumption	(Notes 4, 6)	P_C	-	175	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving the load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Note 7) PINS 1-4, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	(Note 7) PINS 1-4, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA	(Notes 7, 8) PINS 6-8, 11, 12	V_{OH}	4.0	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA	(Notes 7, 8) PINS 6-8, 11, 12	V_{OL}	-	-	0.4	V
Input Leakage Current	Except Pin 5		-	-	±10	µA

Notes:
7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
8. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 9)				
E1, 75 Ω	(Note 10)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 11)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 12)	2.7	3.0	3.3	V
T1, DSX-1	(Note 13)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
75Ω application	(Note 10)	-0.237	-	0.237	V
120Ω application	(Note 11)	-0.3	-	0.3	V
Load Presented To Transmitter Output	(Note 9)	-	75	-	Ω
Jitter Added by the Transmitter	(Note 14)				
10Hz - 8kHz		-	0.005	0.02	UI
8kHz - 40kHz		-	0.008	0.025	UI
10Hz - 40kHz		-	0.010	0.025	UI
Broad Band		-	0.015	0.05	UI
Power in 2kHz band about 772kHz	(Notes 9, 15)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 9, 15)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 9, 15)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
Transmitter Return Loss	(Notes 9, 15, 16)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB
Transmitter Short Circuit Current	(Notes 9, 17)	-	-	50	mA RMS

Notes:
9. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.
10. Amplitude measured at the transformer (CS6158A-1:1 or 1:1.26) output across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.
11. Amplitude measured at the transformer (CS6158A-1:1.26) output across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
12. Amplitude measured at the transformer (CS6158A-1:1.15) output across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
13. Amplitude measured across a 100 Ω load at the DSX-1 Cross-Connect for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0 and 1/1/1 after the length of #22 AWG ABAM equivalent cable specified in Table 1. The CS6158A requires a 1:1.15 transformer.
14. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
15. Not production tested. Parameters guaranteed by design and characterization.
16. Return loss = 20 $\log_{10}$ ABS($(z_1 + z_0)/(z_1 - z_0)$) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
17. Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6	-	-	dB
Data Decision Threshold					
T1, DSX-1	(Note 18)	60	65	70	% of peak
T1, DSX-1	(Note 19)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 20)	45	50	55	% of peak
Allowable Consecutive Zeros before LOS	(Note 21)	160	175	190	bits
Receiver Input Jitter Tolerance	(Note 22)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold	(Note 21)	0.25	0.30	0.50	V
Driver Performance Monitor					
MTIP/MRING Sensitivity: Differential Voltage Required for Detection		-	0.6	-	V

Notes:
18. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
19. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
20. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
21. LOS goes high after 160 to 190 consecutive zeros are received. A zero is output on RPOS and RNEG for each bit period where the input signal amplitude remains below the data decision threshold. The analog input squelch circuit operates when the input signal amplitude above ground on the RTIP and RRING pins falls within the range of 0.25V to 0.50V long enough for the internal slicing threshold to decay within this range. Operation of the squelch causes zeros to be output on RPOS and RNEG as long as the input amplitude remains below 0.25V. During receive LOS, pulses greater than 0.25V in amplitude may be output on RPOS and RNEG. LOS returns low after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.
22. Jitter tolerance increases at lower frequencies. See Figure 7.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	(Note 23)	t_{pwh2}	150	-	500	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 24)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Notes 25, 26, 27)	t_{pwh1}/t_{pw1}	-	29	-	%
RCLK Cycle Width	(Notes 25, 26, 27)	t_{pw1}	320	648	980	ns
RCLK High Time	(Notes 25, 26, 27)	t_{pwh1}	130	190	240	ns
RCLK Low Time	(Notes 25, 26, 27)	t_{pwl1}	100	458	850	ns
Rise Time, All Digital Outputs	(Note 28)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 28)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Notes 26, 27)	t_{su1}	50	-	-	ns
RPOS/RNEG Valid After RCLK Rising	(Notes 26, 27)	t_{h1}	50	-	-	ns

Notes:
23. The transmitted pulse width does not depend on the TCLK duty cycle.
24. ACLKI may be provided by an external source or TCLK, but *not* RCLK.
25. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
26. Max and Min RCLK duty cycles and pulse widths are for worst case jitter conditions: i.e. 0.4 UI AMI data displacement for T1 or 0.2 UI AMI data displacement for E1. See text section on *Jitter and Recovered Clock*.
27. Not production tested. Guaranteed by design and/or characterization.
28. At max load of 1.6 mA and 50 pF.

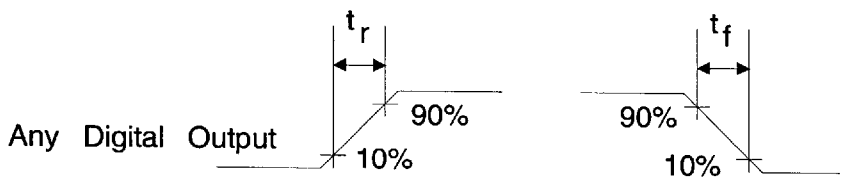


Figure 1. Signal Rise and Fall Characteristics

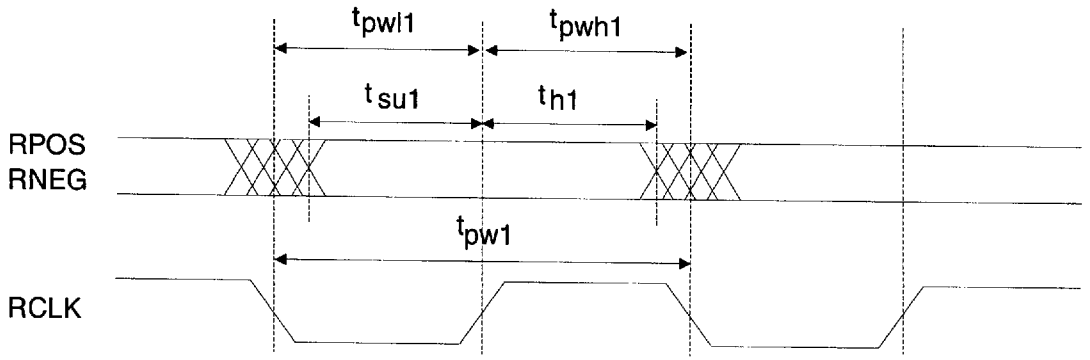


Figure 2. Recovered Clock and Data Switching Characteristics

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	(Note 23)	t_{pwh2}	150	-	340	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 24)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Notes 25, 26, 27)	t_{pwh1}/t_{pw1}	-	29	-	%
RCLK Cycle Width	(Notes 25, 26, 27)	t_{pw1}	310	488	670	ns
RCLK High Time	(Notes 25, 26, 27)	t_{pwh1}	90	140	190	ns
RCLK Low Time	(Notes 25, 26, 27)	t_{pwl1}	120	348	500	ns
Rise Time, All Digital Outputs	(Note 28)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 28)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Notes 26, 27)	t_{su1}	50	-	-	ns
RPOS/RNEG Valid After RCLK Rising	(Notes 26, 27)	t_{h1}	50	-	-	ns

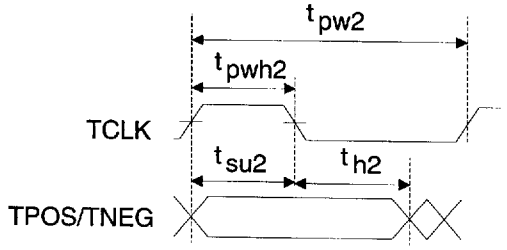


Figure 3a. Transmit Clock and Data Switching Characteristics

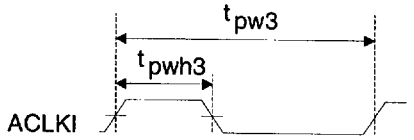


Figure 3b. Alternate External Clock Characteristics

THEORY OF OPERATION

Enhancements in CS6158A

The CS6158A provides higher performance and more features than the CS6158 including:

- 50% reduction in power consumption
- 14 dB of transmitter return loss (during marks and spaces) improves signal quality.
- The E1 transmitted pulse width is set internally by the CS6158A (and not by the TCLK input duty cycle).
- Upon power up, RCLK immediately starts and LOS (loss of signal) is set high.
- When the transmitter senses the absence of a signal on TCLK, TTIP and TRING are forced to zero.
- ANSI T1.231-1993 compliant receiver LOS (Loss Of Signal) handling.
- The driver performance monitor operates over a wider range of input signal levels.

CS6158 designs can be converted to the higher performance, pin-compatible CS6158A if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio and the 4.4 Ω resistor used in 75 Ω E1 applications is shorted.

Transmitter

The transmitter takes data from a T1 (or E1) terminal and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 (DSX-1 or Network Interface) or CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 1. The CS6158A line driver is designed to drive a 75 Ω equivalent load.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	
1	0	0	133-266 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		RESERVED
0	0	0	75Ω and 120Ω	E1 CCITT G.703
0	1	0	FCC PART 68, OPT. A	T1 NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1. Line Length Selection

For E1 applications, the CS6158A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the IC to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 4. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

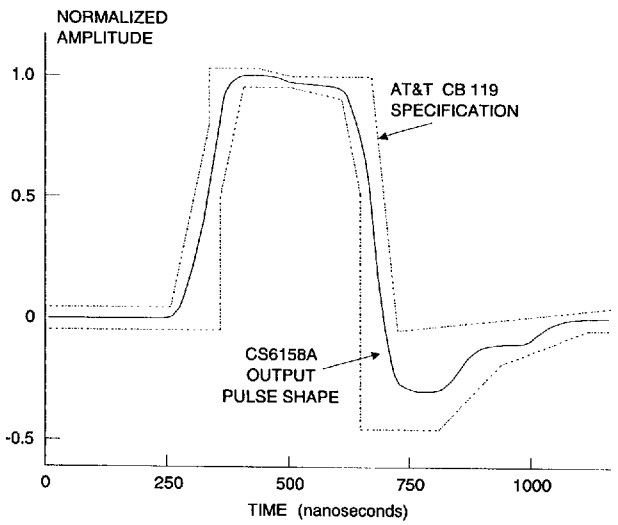


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figure A1.

Table 2. CCITT G.703 Specifications

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS6158A automatically adjusts the pulse width based upon the "line length " selection made.

The E1 CCITT G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 5, and specified in Table 2.

The CS6158A transmitter will detect a failed TCLK, and will insure that neither TTIP nor TRING gets stuck high.

When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals down to approximately 300 mV in amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The

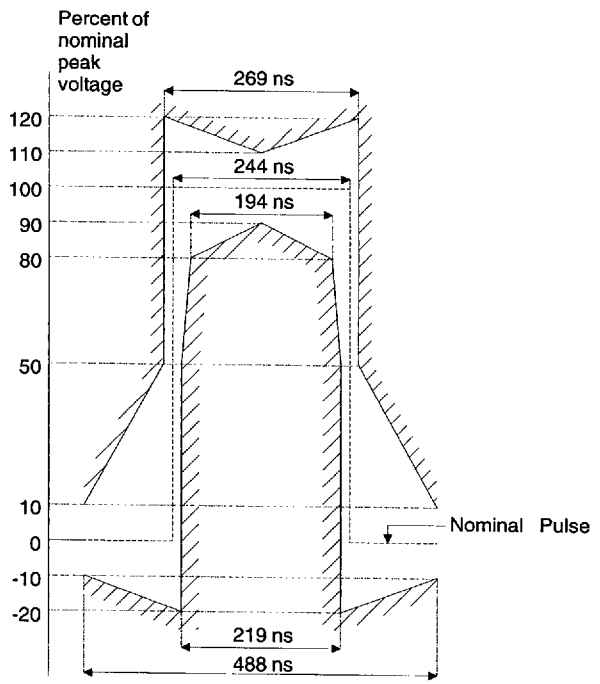


Figure 5 - Mask of the Pulse at the 2048 kbps Interface

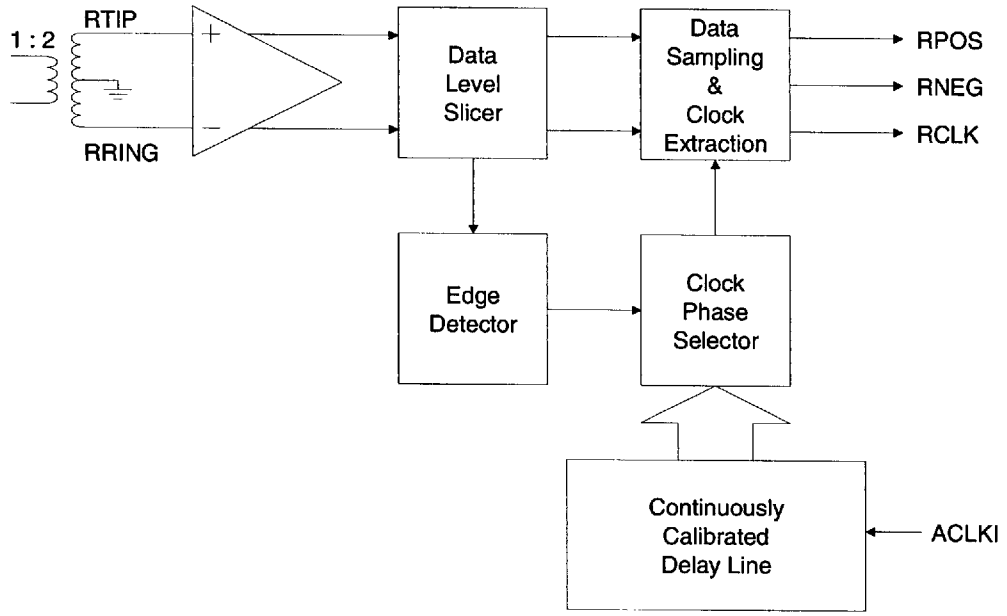


Figure 6. - Receiver Block Diagram

transformer is center tapped on the CS6158A side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI, into 13 equal divisions of phases. Continuous calibration ensures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that plot shown in Figure 7.

The CS6158A outputs a clock on RCLK immediately upon power-up. The clock recovery circuit is calibrated, and the device will lock onto the

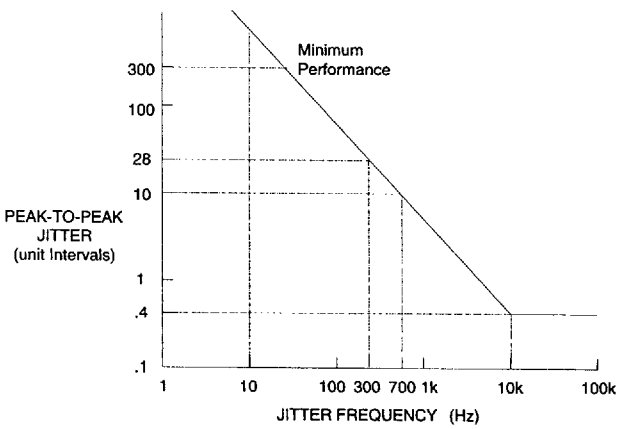


Figure 7. - Input Jitter Tolerance of Receiver

AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

Data on RPOS and RNEG is stable and may be sampled on the rising edge of RCLK, the recovered clock.

Jitter and Recovered Clock

The CS6158A is designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UI. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS6158A, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similar calculations hold for the 2.048 MHz rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS6158A, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS6158A is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. In the CS6158A, LOS returns to logic zero

after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993. A power-up or manual reset will also set LOS high.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line. Because RCLK cycle times vary, selecting RLOOP will result in adding jitter to the transmitted data. *Therefore selection of the RLOOP function on a functioning link is not recommended.* Rather, it is recommended that remote loopbacks be implemented external to the CS6158A, for example, by using a frame buffer in the data path between the CS6158A receiver and transmitter.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6158A is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance.

Power On Reset / Reset

Upon power-up, the CS6158A is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear the internal logic.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset

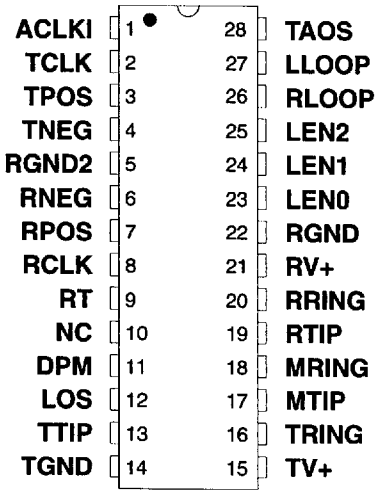
request (falling edge of RLOOP or LLOOP). A reset will also set LOS high.

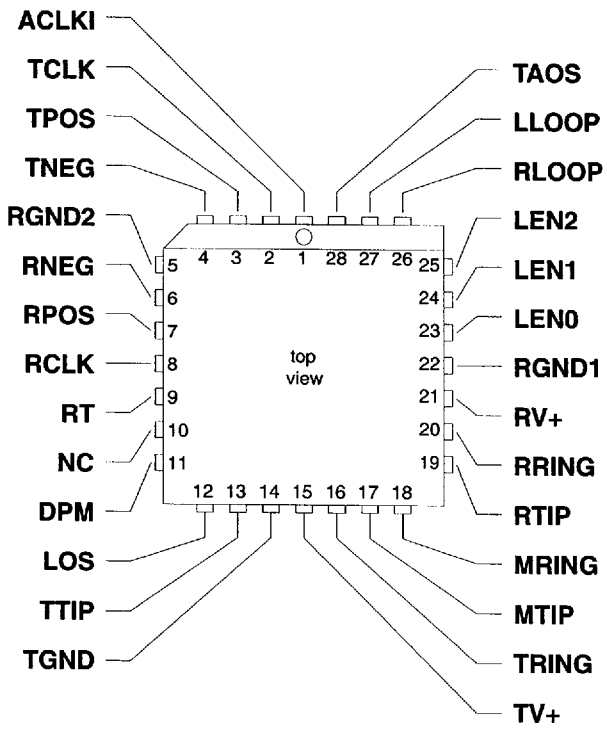
Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS





Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 Volts.

RV+ - Positive Power Supply, Pin 21.
Positive power supply for the device, except transmit drivers; typically +5 Volts.

RGND1, RGND2 - Ground, Pins 22 and 5
Power supply grounds for the device, except transmit drivers; typically 0 Volts.

Control

LLOOP - Local Loopback, Pin 27.
Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.
Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.
Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TAOS - Transmit All Ones select, Pin 28.
Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency selected by TCLK.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.
Either a 1.544 MHz (or 2.048 MHz for E1) clock must be input to ACLKI, which is used to calibrate the receiver delay line. Since ACLKI is used to calibrate the receiver, RCLK will equal ACLKI upon loss of signal.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.
Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

RT - Resistor Termination, Pin 9.

This pin should be connected to the RV+ power supply through a 1kΩ resistor.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the transmitter output. If the monitor is not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. When in the loss of signal state, received ones are output at RPOS/RNEG. In the CS6158A, LOS returns to a logic 0 after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING, DPM goes to a logic 1.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

The receiver recovered clock and NRZ digital data is output on these pins. RPOS and RNEG are stable and valid on the rising edge of RCLK. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

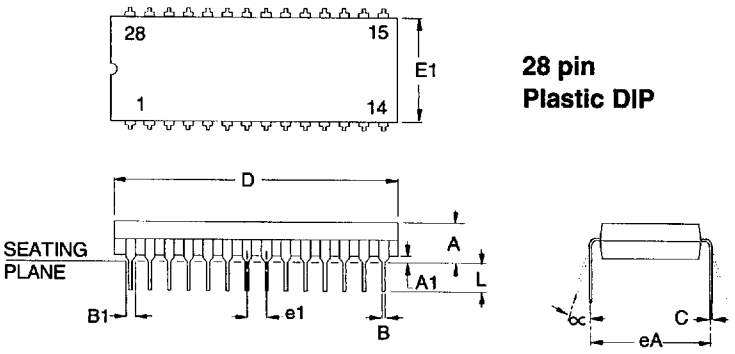
The AMI signal is driven to the line through these pins.

For the CS6158A, this output is designed to drive a 75 Ω ohm load. A transformer is required as shown in Figure A1.

Miscellaneous

NC - No Connect, Pin 10

Pin 10 may be left floating (recommended for new designs), or may be tied to ground.

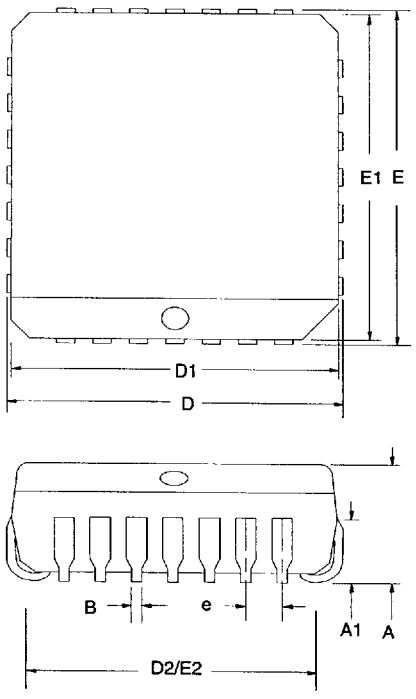


28 pin
Plastic DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	5.08	0.155	0.170	0.200
A1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	36.45	36.83	37.21	1.435	1.450	1.465
E1	13.72	13.97	14.22	0.540	0.550	0.560
e1	2.41	2.54	2.67	0.095	0.100	0.105
eA	15.24	-	15.87	0.600	-	0.625
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:

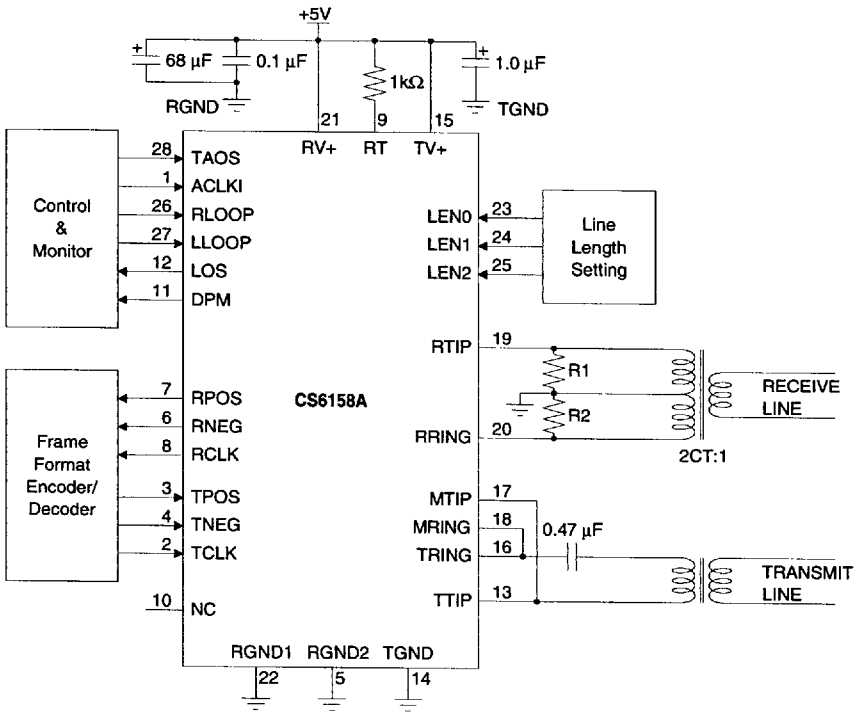
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.



28-pin PLCC

DIM	28					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180
A1	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021
D/E	12.32	12.45	12.57	0.485	0.490	0.495
D1/E1	11.43	11.51	11.58	0.450	0.453	0.456
D2/E2	9.91	10.41	10.92	0.390	0.410	0.430
e	1.19	1.27	1.35	0.047	0.050	0.053

APPLICATIONS



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	Transmit Transformer
CS6158A	1.544	100	200	1:1.15
	2.048	120	240	1:1.26
	2.048	75	150	1:1

Figure A1. - Typical Connection Diagram

Line Interface

Figure A1 shows the typical configuration for the CS6158A.

For T1 applications, the receiver transformer is center-tapped and center-grounded with 200 Ω resistors between the center tap and each leg on the IC side. These resistors provide the 100 Ω termination for the T1 line. When terminating 2.048 MHz twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load. For transmitting data at 2.048 MHz onto a 75 Ω coax cable, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Figure A1 shows a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

Transformers

Recommended transmitter and receiver transformer specifications for the CS6158A are shown in Table A1. The transformers in Table A2 have been tested and recommended for use with the CS6158A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

In applications with the CS6158A where it is advantageous to use a single transmitter transformer for both 75Ω and 120Ω E1 applications, a 1:1.26 transformer may be used. Although transmitter return loss will be reduced for 75Ω applications, the pulse amplitude will be correct.

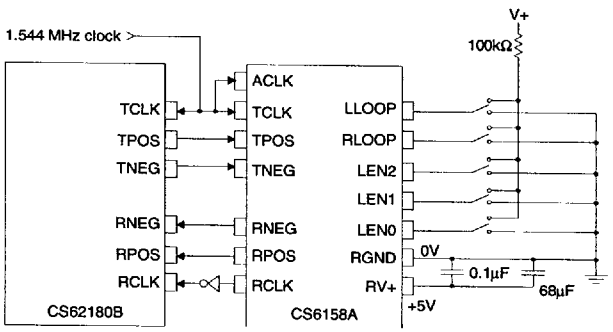


Figure A2. - Interfacing the CS6158A with a CS62180B

Interfacing the CS6158A with CS62180B T1 Transceiver

To interface with the CS62180B, connect the devices as shown in Figure A2.

Parameter	CS6158A Receiver	CS6158A Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 75 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 120 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A1. Transformer Specifications

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A2. Recommended Transformers For The CS6158A

• Notes •

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A Cirrus Logic Company

CDB61534, CDB61535, CDB61535A, CDB6158, CDB6158A, CDB61574, CDB61574A, CDB61575, CDB61577, CDB615304A, & CDB61305A

Line Interface Evaluation Board

Features

- Socketed Line Interface Device
- All Required Components for Complete Line Interface Evaluation
- Configuration by DIP Switch or Serial Interface
- LED Status Indicators for Alarm Conditions
- Support for Host, Hardware, and Extended Hardware Modes

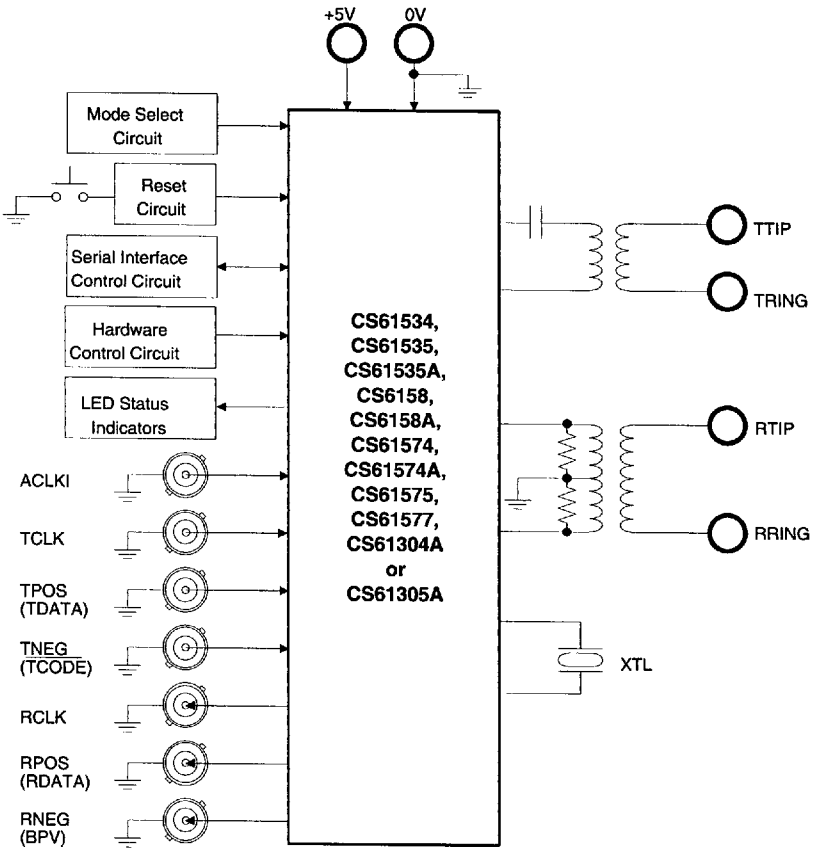
General Description

The evaluation board includes a socketed line interface device and all support components necessary for evaluation. The board is powered by an external 5 Volt supply.

The board may be configured for 100 Ω twisted-pair T1, 75 Ω coax E1, or 120 Ω twisted-pair E1 operation. Binding posts are provided for line connections. Several BNC connectors are available to provide system clocks and data I/O. Two LED indicators monitor device alarm conditions. The board supports all line interface operating modes.

ORDERING INFORMATION:

CDB61534, CDB61535. CDB61535A,
CDB6158, CDB6158A, CDB61574,
CDB61574A, CDB61575, CDB61577,
CDB61304A, CDB61305A



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

POWER SUPPLY

As shown on the evaluation board schematic in Figure 1, power is supplied to the evaluation board from an external +5 Volt supply connected to the two binding posts labeled +5V and GND. Transient suppressor D10 protects the components on the board from over-voltage damage and reversed supply connections. The recommended power supply decoupling is provided by C1, C2 and C3. Ceramic capacitor C1 and electrolytic capacitor C2 are used to decouple RV+ to RGND. Capacitor C3 decouples TV+ to TGND. The TV+ and RV+ power supply traces are connected at the device socket U1. A ground plane on the component side of the evaluation board insures optimum performance.

BOARD CONFIGURATION

Pins on line interface device U1 with more than one pin name have different functions depending on the operating mode selected. Pin names not enclosed in parenthesis or square brackets describe the Hardware mode pin function. Pin names enclosed in parenthesis describe the Extended Hardware mode pin function. Pin names enclosed in square brackets describe the Host mode pin function.

Table 1 explains how to configure the evaluation board jumpers depending on the device installed and the desired operating mode. Mode selection is accomplished with slide switch SW1 and jumpers JP2, JP6, and JP7. The CS61535A, CS61574A, CS61575, CS61577, CS61304A, and CS61305A support the Hardware, Extended Hardware, and Host operating modes. The CS61534, CS61535, and CS61574 support the Hardware and Host operating modes. The CS6158 and CS6158A only support the Hardware operating mode.

Hardware Mode

In the Hardware operating mode, the line interface is configured using DIP switch S2. The digital control inputs to the device selected by S2 include: transmit all ones (TAOS), local loopback (LLOOP), remote loopback (RLOOP), and transmit line length selection (LEN2,LEN1,LEN0). Closing a DIP switch on S2 towards the label sets the device control pin of the same name to logic 1 (+5 Volts). Note that S2 switch positions $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ have no function in Hardware mode. In addition, the host processor interface connector JP1 should not be used in the Hardware mode.

Two LED status indicators are provided in Hardware mode. The LED labeled DPM (AIS) illuminates when the line interface asserts the Driver

JUMPER	POSITION	FUNCTION SELECTED
JP1	-	Connector for external processor in Host operating mode.
JP2, JP6, JP7	A-A	Extended Hardware operating mode.
	B-B	Hardware or Host operating modes.
JP3	IN	Hardware or Extended Hardware operating modes.
	OUT	Host operating mode.
JP4	C-C	Connects the ACLKI BNC input to pin 1 of device.
	D-D	Grounds the ACLKI BNC input through 51Ω resistor R1.
JP5	E-E	Transmit line connection for all applications except those listed for "F-F" on the next line.
	F-F	75Ω coax E1 applications using the Schott 12932/12532 or PE-65389/65566 at transformer T1.
JP8	IN	Shorts resistor R2 for all applications except those listed for "OUT" on the next line.
	OUT	Inserts resistor R2 for 75Ω coax E1 applications using the CS61534, 35, 58, 74, or 77.

Table 1. Evaluation Board Jumper Settings

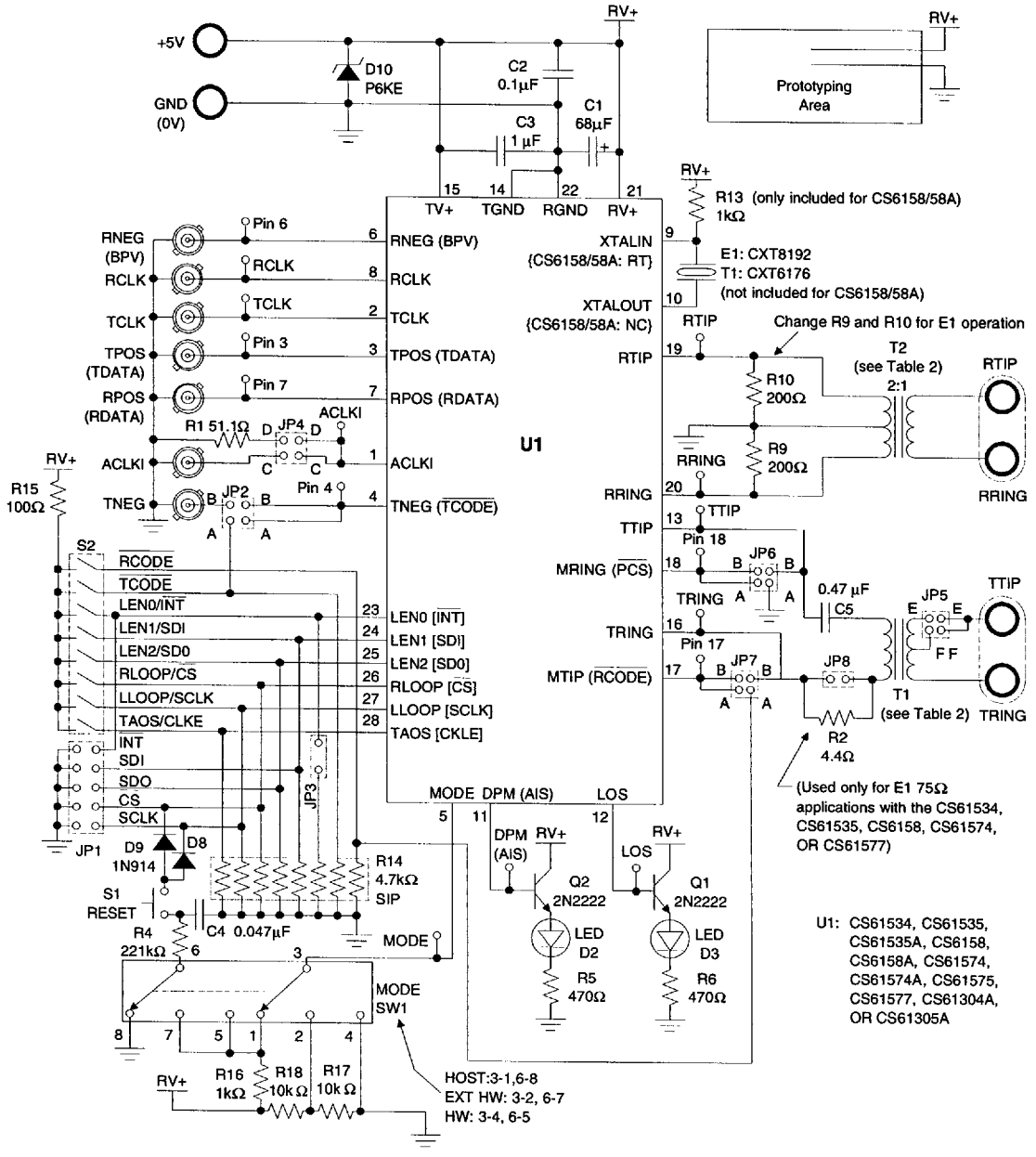


Figure 1. Evaluation Board Schematic

Performance Monitor alarm. The LED labeled LOS illuminates when the line interface receiver has detected a loss of signal.

Extended Hardware Mode

In the Extended Hardware operating mode, the line interface is configured using DIP switch S2. The digital control inputs to the device selected by S2 include: transmit all ones (TAOS), local loopback (LLOOP), remote loopback (RLOOP), transmit line length selection (LEN2, LEN1, LEN0), transmit line code ($\overline{\text{TCODE}}$), and receive line code ($\overline{\text{RCODE}}$). Closing a DIP switch (moving it towards the S2 label) sets the device control pin of the same name to logic 1 (+5 Volts). Note that the $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ options are active low and are enabled when the switch is moved away from the S2 label. The parallel chip select input $\overline{\text{PCS}}$ is tied to ground in Extended Hardware mode to enable the device to be reconfigured when S2 is changed. In addition, the host processor interface connector JP1 should not be used in Extended Hardware mode.

Two LED status indicators are provided in Extended Hardware mode. The LED labeled DPM (AIS) illuminates when the line interface detects the receive blue alarm (AIS). The LED labeled LOS illuminates when the line interface receiver has detected a loss of signal.

Host Mode

In the Host operating mode, the line interface is configured using a host processor connected to the serial interface port JP1. The S2 switch position labeled CLKE selects the active edge of SCLK and RCLK. Closing the CLKE switch selects RPOS and RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK as required by the CS2180B T1 framer.

All other DIP switch positions on S2 should be open (logic 0) to prevent shorting of the serial interface signals. Resistor R15 is a current limiting resistor that prevents the serial interface signals from being shorted directly to the +5 Volt supply if any S2 switch, other than CLKE, is closed. Jumper JP3 should be out so the $\overline{\text{INT}}$ pin may be externally pulled-up at the host processor interrupt pin.

Two LED status indicators are provided in Host mode. The LED labeled DPM (AIS) illuminates when the line interface asserts the Driver Performance Monitor alarm. The LED labeled LOS illuminates when the line interface receiver has detected a loss of signal.

Manual Reset

A manual reset circuit is provided that can be used in Hardware and Extended Hardware modes. The reset circuit consists of S1, R4, R16, C4, D8, and D9. Pressing switch S1 forces both LLOOP and RLOOP to a logic 1 and causes a reset. A reset is only necessary for the CS61534 device to calibrate the center frequency of the receiver clock recovery circuit. All other line interface units use a continuously calibrated clock recovery circuit that eliminates the reset requirement.

TRANSMIT CIRCUIT

The transmit clock and data signals are supplied on BNC inputs labeled TCLK, TPOS(TDATA), and TNEG. In the Hardware and Host operating modes, data is supplied on the TPOS(TDATA) and TNEG connectors in dual NRZ format. In the Extended Hardware operating mode, data is supplied in NRZ format on the TPOS(TDATA) connector and TNEG is not used.

The transmitter output is transformer coupled to the line through a transformer denoted as T1 in Figure 1. The signal is available at the TTIP and TRING binding posts. Capacitor C5 is the recommended 0.47 µF DC blocking capacitor.

The evaluation board supports 100Ω twisted-pair T1, 75Ω coax E1, and 120Ω twisted-pair E1 operation. The CDB61534, CDB61535, CDB6158, CDB61574, and CDB61577 are supplied from the factory with a 1:2 transmit transformer that may be used for all T1 and E1 applications. The CDB61535A, CDB6158A, CDB61574A, CDB61575, CDB61304A, and CDB61305A are supplied with a 1:1.15 transmit transformer installed for T1 applications. An additional 1:1:1.26 transformer for E1 applications is provided with the board. This transformer requires JP5 to be jumpered across F-F for 75Ω coax E1 applications.

The CDB61534, CDB61535, CDB6158, CDB61574, and CDB61577 require the JP8 jumper to be out for 75Ω coax E1 applications. This inserts resistor R2 to reduce the transmit pulse amplitude and meet the 2.37 V nominal pulse amplitude requirement in CCITT G.703. In addition, R2 increases the equivalent load impedance across TTIP and TRING.

RECEIVE CIRCUIT

The receive line interface signal is input at the RTIP and RRING binding posts. The receive signal is transformer coupled to the line interface device through a center-tapped 1:2 transformer. The transformer produces ground referenced pulses of equal amplitude and opposite polarity on RTIP and RRING.

The receive line interface is terminated by resistors R9 and R10. The evaluation boards are supplied from the factory with 200Ω resistors for terminating 100Ω T1 twisted-pair lines. Resistors R9 and R10 should be replaced with 240Ω resistors for terminating 120Ω E1 twisted-pair lines or 150Ω resistors for terminating 75Ω E1 coaxial lines. Two 243Ω resistors and two 150Ω resistors are included with the evaluation board for this purpose.

The recovered clock and data signals are available on BNC outputs labeled RCLK, RPOS(RDATA), and RNEG(BPV). In the Hardware and Host operating modes, data is output on the RPOS(RDATA) and RNEG(BPV) connectors in dual NRZ format. In the Extended Hardware operating mode, data is output in NRZ format on the RPOS(RDATA) connector and bipolar violations are reported on the RNEG(BPV) connector.

QUARTZ CRYSTAL

A quartz crystal must be installed in socket Y1 for all devices except the CS6158 and CS6158A. A Crystal Semiconductor CXT6176 crystal is recommended for T1 operation and a CXT8192 is recommended for E1 operation. The evaluation board has a CXT6176 installed at the factory and a CXT8192 is also provided with the board.

The CDB6158 and CDB6158A have resistor R13 installed instead of a crystal. This connects the RT pin of the device to the +5 Volt supply.

ALTERNATE CLOCK INPUT

The ACLKI BNC input provides the alternate clock reference for the line interface device (ACLK for the CS61534) when JP4 is jumpered across C-C. This clock is required for the CS61534, CS61535, CS6158, and CS6158A operation but is optional for all other line interface devices. If ACLKI is provided, it may be desirable to connect both C-C and D-D positions on JP4 to terminate the external clock source providing ACLKI with the 51Ω resistor R1. If ACLKI is optional and not used, connector JP4 should be jumpered across D-D to ground pin 1 of the device through resistor R1.

TRANSFORMER SELECTION

To permit the evaluation of other transformers, Table 2 lists the transformer and line interface device combinations that can be used in T1 and E1

applications. A letter at the intersection of a row and column in Table 2 indicates that the selected transformer is supported for use with the device. The transformer is installed in the evaluation board with pin 1 positioned to match the letter illustrated on the drawing in Table 2. For example, the Pulse Engineering PE-65388 transformer may be used with the transmitter of the CS61575 device for 100Ω T1 applications only (as indicated by note 3) when installed in transformer socket T1 with pin 1 at position D (upper right).

PROTOTYPING AREA

A prototyping area with power supply and ground connections is provided on the evaluation board. This area can be used to develop and test a variety of additional circuits like a data pattern generator, CS2180B framer, system synchronizer PLL, or specialized interface logic.

EVALUATION HINTS

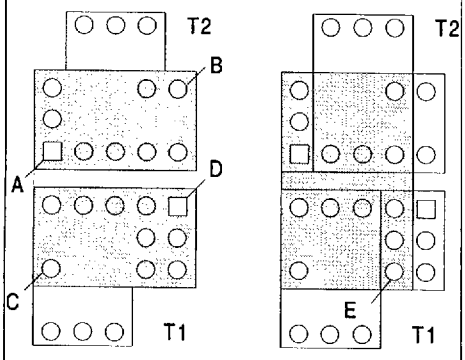
1. Properly terminate TTIP/TRING when evaluating the transmit output signal. For more information concerning pulse shape evaluation, refer to the Crystal application note entitled "Measurement and Evaluation of Pulse Shapes in T1/E1 Transmission Systems."

2. Change the receiver terminating resistors R9 and R10 when evaluating E1 applications. Resistors R9 and R10 should be replaced with 240Ω resistors for terminating 120Ω E1 twisted-pair lines or 150Ω resistors for terminating 75Ω E1 coaxial lines. Two 243Ω resistors and two 150Ω resistors are included with the evaluation board for this purpose.

3. Closing a DIP switch on S2 towards the label sets the device control pin of the same name to logic 1 (+5 Volts).

4. To avoid damage to the external host controller connected to JP1, all S2 switch positions (except CLKE) should be open. In the Host operating mode, the CLKE switch selects the active edge of SCLK and RCLK.

TRANSFORMER (Turns Ratio)[1,2]	LINE INTERFACE UNIT																	
	'34		'35		'35A		'58		'58A		'74,'77		'74A		'75		'304A, '305A	
	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX
PE-65351 (1:2CT)	A	D	A	D	A		A	D	A		A	D	A		A		A	
Schott 12930 (1:2CT)	B	C	B	C	B		B	C	B		B	C	B		B		B	
PE-65388 (1:1.15)						D[3]				D[3]				D[3]		D[3]		D[3,5]
Schott 12931 (1:1.15)						C[3]				C[3]				C[3]		C[3]		C[3,5]
PE-65389 (1:1:1.26)						D[4]				D[4]				D[4]		D[4]		D[4,5]
Schott 12932 (1:1:1.26)						C[4]				C[4]				C[4]		C[4]		C[4,5]
PE-64951 (dual 1:2CT)	E		E				E				E							
Schott 11509 (dual 1:2CT)	E		E				E				E							
PE-65565 (dual 1:1.15 & 1:2CT)					E[3]				E[3]				E[3]		E[3]		E[3,5]	
Schott 12531 (dual 1:1.15 & 1:2CT)					E[3]				E[3]				E[3]		E[3]		E[3,5]	
PE-65566 (dual 1:1:1.26 & 1:2CT)					E[4]				E[4]				E[4]		E[4]		E[4,5]	
Schott 12532 (dual 1:1:1.26 & 1:2CT)					E[4]				E[4]				E[4]		E[4]		E[4,5]	



NOTES:

1. A letter at the intersection of a row and column in Table 2 indicates that the selected transformer is supported for use with the device. The transformer is installed in the evaluation board with pin 1 positioned to match the letter illustrated in the drawing to the left.
2. The receive transformer (RX) is soldered at location T2 on the evaluation board and is used for all applications. The transmit transformer (TX) is socketed at location T1 on the evaluation board and may be changed according to the application.
3. For use in 100Ω T1 twisted-pair applications only.
4. For use in 75Ω and 120Ω E1 applications only. Place jumper JP5 in position F-F for 75Ω E1 applications requiring a 1:1 turns ratio.
5. Transmitter return loss improves when using a 1:2 turns ratio transformer with the appropriate transmit resistors.

Table 2. Transformer Applications

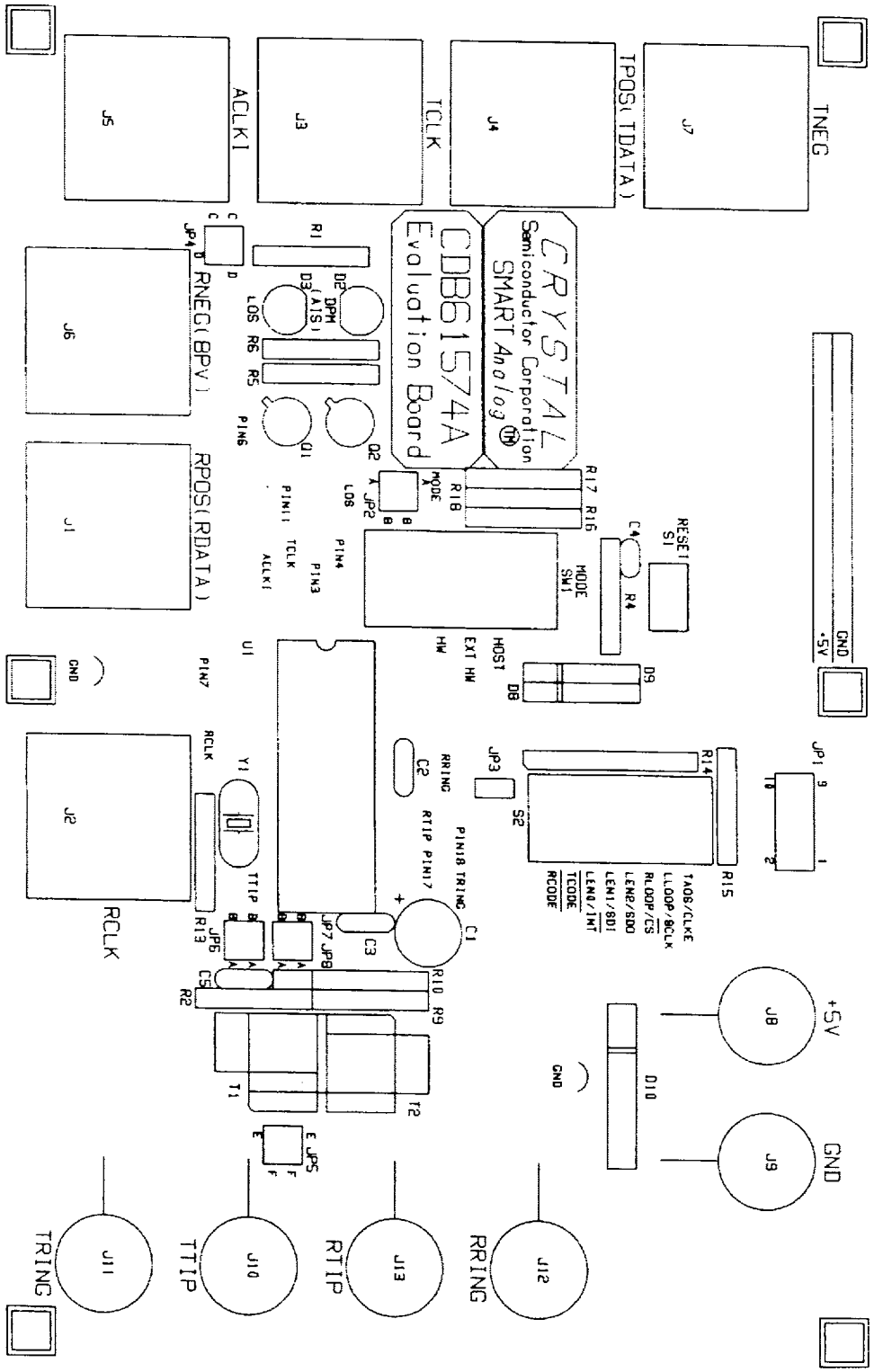


Figure 2. Silk Screen Layer (NOT TO SCALE)

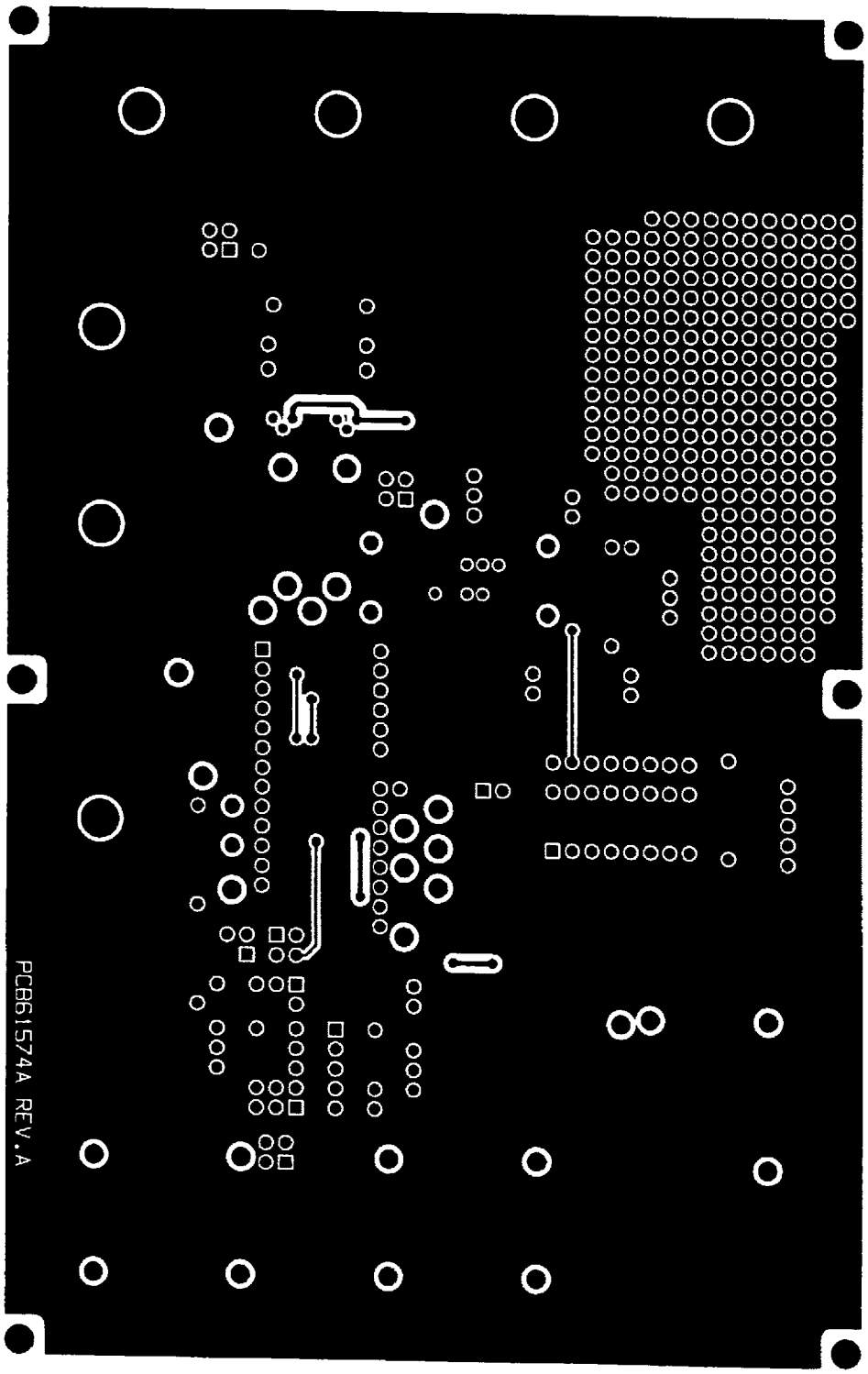


Figure 3. Top Ground Plane Layer (NOT TO SCALE)

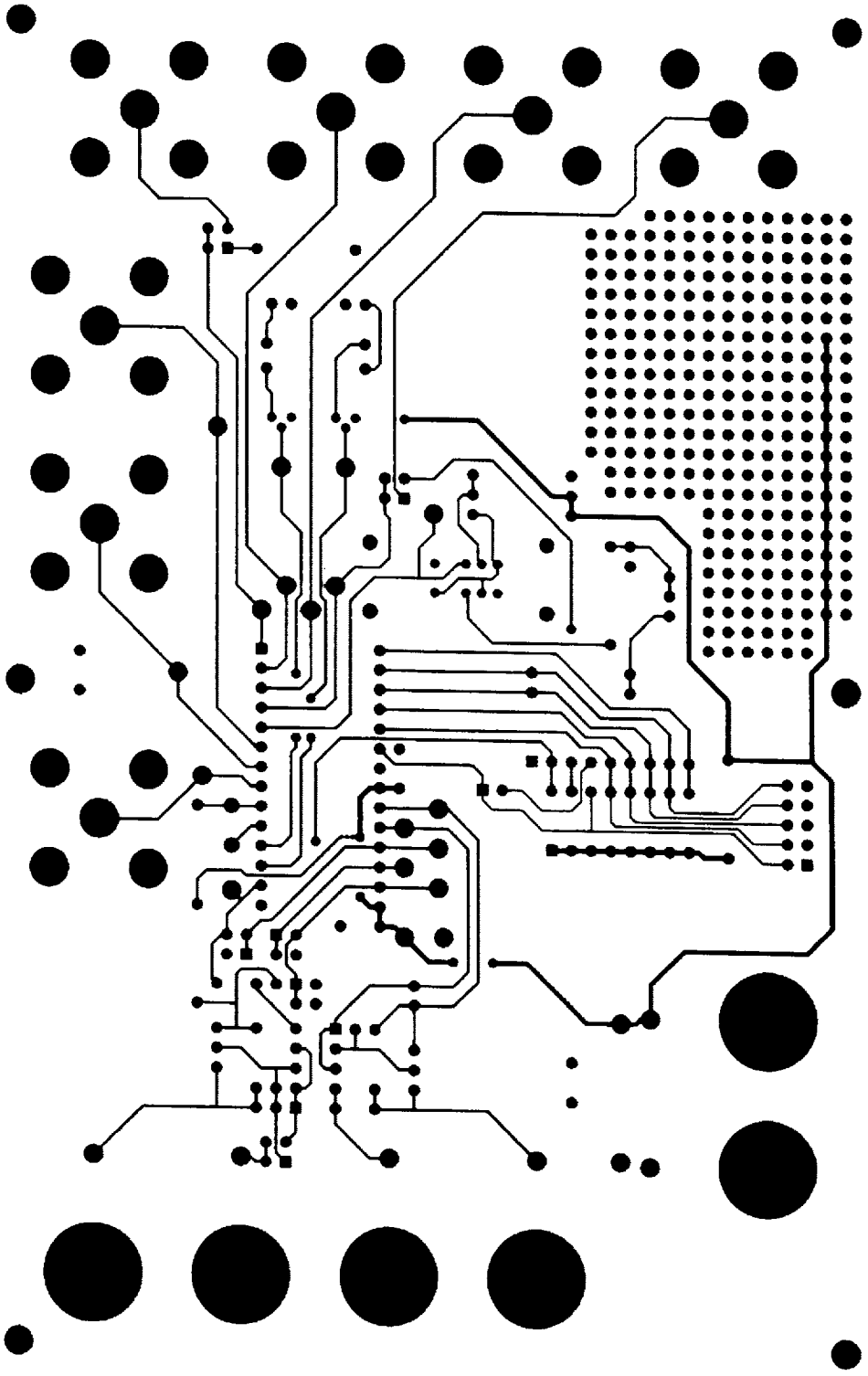


Figure 4. Bottom Trace Layer (NOT TO SCALE)