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February 24, 2009

DS25MB100

2.5 Gbps 2:1/1:2 CML Mux/Buffer with Transmit Pre-Emphasis and Receive Equalization

General Description

The DS25MB100 is a signal conditioning 2:1 multiplexer and 1:2 fan-out buffer designed for use in backplane redundancy or cable driving applications. Signal conditioning features include input equalization and programmable output Pre-emphasis that enable data communication in FR4 backplane up to 2.5 Gbps. Each input stage has a fixed equalizer to reduce ISI distortion from board traces. All output drivers have four selectable levels of Pre-emphasis to compensate for transmission losses from long FR4 backplane or cable attenuation reducing deterministic jitter. The Pre-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs are internally terminated with 100Ω differential terminating resistors. All driver outputs are internally terminated with 50Ω to V_{CC}.

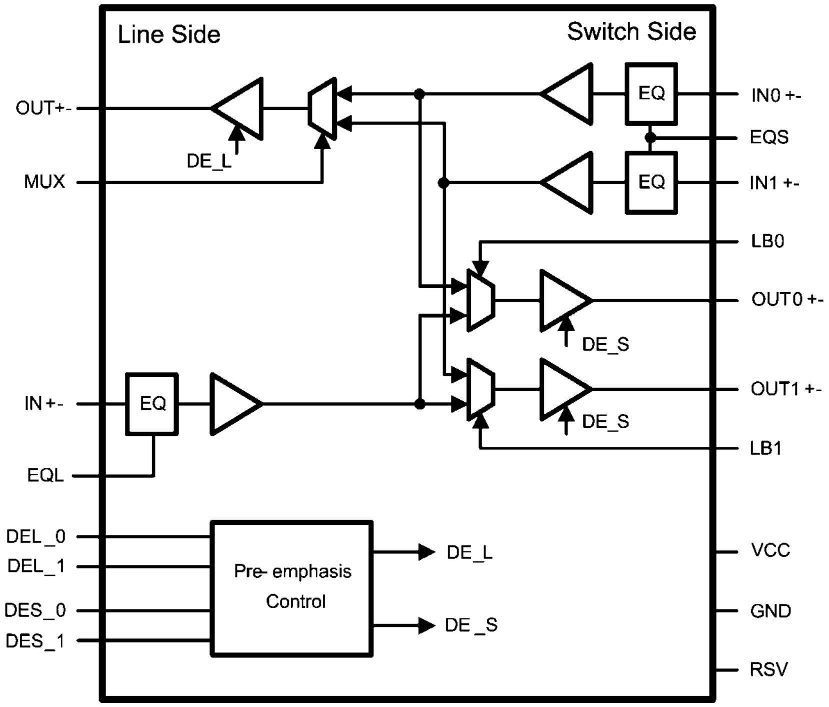
Features

- 2:1 multiplexer and 1:2 buffer
- 0.25–2.5 Gbps fully differential data paths
- Fixed input equalization
- Programmable output Pre-emphasis
- Independent Pre-emphasis controls
- Programmable loopback modes
- On-chip terminations
- HBM ESD rating 6 kV on all pins
- +3.3V supply
- Low power, 0.45 W typical
- Lead-less LLP-36 package
- −40°C to +85°C operating temperature range

Applications

- Backplane or cable driver
- Redundancy and signal conditioning applications
- CPRI/OBSAI

Functional Block Diagram



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Note: All CML inputs and outputs must be AC coupled for optimal performance.

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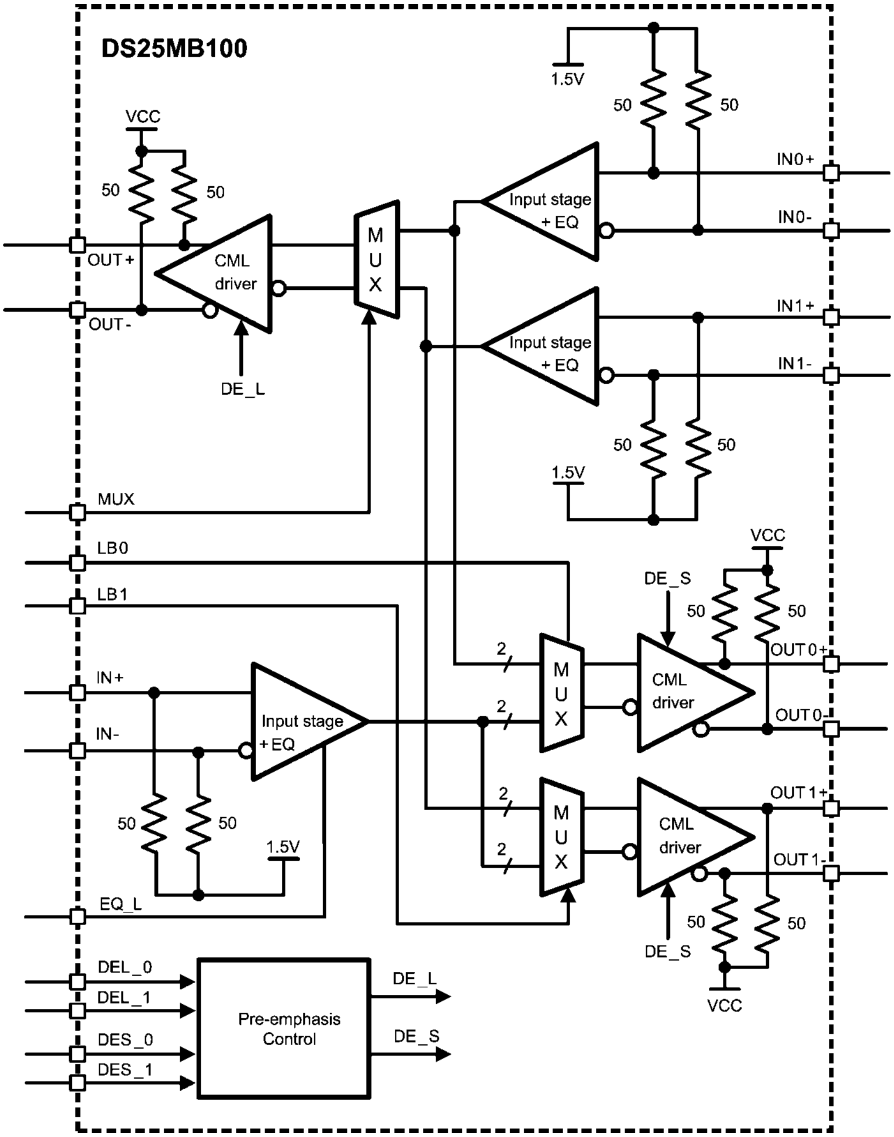
Simplified Block Diagram


DS25MB100
1.5V
50
50
IN0+
IN0-
Input stage
+EQ
VCC
50
50
OUT+
OUT-
CML
driver
DE_L
M
U
X
IN1+
IN1-
Input stage
+EQ
50
50
1.5V
MUX
LB0
LB1
VCC
DE_S
50
50
OUT0+
OUT0-
CML
driver
IN+
IN-
Input stage
+EQ
2
2
2
2
M
U
X
M
U
X
OUT1+
OUT1-
CML
driver
50
50
1.5V
EQ_L
50
50
DE_S
VCC
DEL_0
DEL_1
DES_0
DES_1
Pre-emphasis
Control
DE_L
DE_S

20208902

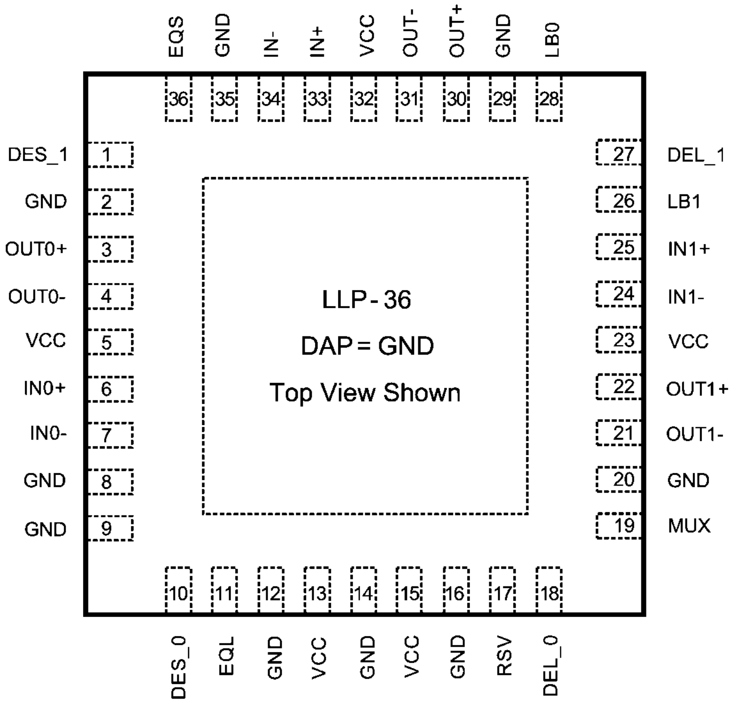
Pin Descriptions

Pin Name	Pin Number	I/O	Description
LINE SIDE HIGH SPEED DIFFERENTIAL IO's			
IN+ IN–	33 34	I	Inverting and non-inverting differential inputs at the line side. IN+ and IN– have an internal 50Ω connected to an internal reference voltage. See *Figure 6*.
OUT+ OUT–	30 31	O	Inverting and non-inverting differential outputs at the line side. OUT+ and OUT– have an internal 50Ω connected to V_{CC}.
SWITCH SIDE HIGH SPEED DIFFERENTIAL IO's			
OUT0+ OUT0–	3 4	O	Inverting and non-inverting differential outputs at the switch side. OUT0+ and OUT0– have an internal 50Ω connected to V_{CC}.
OUT1+ OUT1–	22 21	O	Inverting and non-inverting differential outputs at the switch side. OUT1+ and OUT1– have an internal 50Ω connected to V_{CC}.
IN0+ IN0–	6 7	I	Inverting and non-inverting differential inputs to the mux at the switch side. IN0+ and IN0– have an internal 50Ω connected to an internal reference voltage. See *Figure 6*.
IN1+ IN1–	25 24	I	Inverting and non-inverting differential inputs to the mux at the switch side. IN1+ and IN1– have an internal 50Ω connected to an internal reference voltage. See *Figure 6*.
CONTROL (3.3V LVCMOS)			
MUX	19	I	A logic low at MUX selects IN1±. MUX is internally pulled high. Default state for MUX is IN0±.
EQL	11	I	A logic low enables the input equalizer on the line side. EQL is internally pulled high. Default is with EQ disabled.
EQS	36	I	A logic low enables the input equalizer on the switch side. EQS is internally pulled high. Default is with EQ disabled.
DEL_0 DEL_1	18 27	I	DEL_0 and DEL_1 select the output Pre-emphasis of the line side drivers (OUT±). DEL_0 and DEL_1 are internally pulled high.
DES_0 DES_1	10 1	I	DES_0 and DES_1 select the output Pre-emphasis of the switch side drivers (OUT0±, OUT1±). DES_0 and DES_1 are internally pulled high.
LB0	28		A logic low at LB0 enables the internal loopback path from IN0± to OUT0±. LB0 is internally pulled high.
LB1	26	I	A logic low at LB1 enables the internal loopback path from IN1± to OUT1±. LB1 is internally pulled high.
RSV	17	I	Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor.
POWER			
V_{CC}	5, 13, 15, 23, 32	P	V_{CC} = 3.3V ± 5%. Each V_{CC} pin should be connected to the V_{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V_{CC} pin. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each V_{CC} pin to ground plane.
GND	2, 8, 9, 12, 14, 16, 20, 29, 35	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	DAP is the metal contact at the bottom side, located at the center of the LLP package. It should be connected to the GND plane with at least 16 via to lower the ground impedance and improve the thermal performance of the package.

Note: I = Input, O = Output, P = Power

Note: All CML Inputs or Outputs must be AC coupled.

Connection Diagram



20208903

Order Number DS25MB100TSQ
See NS Package Number SQA36A

Functional Description

The DS25MB100 is a signal conditioning 2:1 multiplexer and a 1:2 buffer designed to support port redundancy up to 2.5 Gbps. The high speed inputs are self-biased to about 1.3V and are designed for AC coupling. The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL and CML. The DS25MB100 is not designed to operate with data rates below 250 Mbps or with a DC bias applied to the CML inputs or outputs. Most high speed links are encoded for DC balance and have been defined to include AC coupling capacitors allowing the DS25MB100 to be directly inserted into the datapath without any limitation. The ideal AC coupling capacitor value is often based on the lowest frequency component embedded within the serial link. A typical AC coupling capacitor value ranges between 100 and 1000nF, some specifications with scrambled data may require a larger capacitor for optimal performance. To reduce unwanted parasitics around and within the AC coupling capacitor, a body size of 0402 is recommended. *Figure 5* shows the AC coupling capacitor placement in an AC test circuit.

Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB of transmission loss from a short backplane trace (about 10 inches backplane). The output driver has Pre-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane, and minimize the deterministic jitter caused by the amplitude disparity. The DS25MB100 provides four steps of user-selectable Pre-emphasis ranging from 0, -3, -6 and –9 dB to handle different lengths of backplane. *Figure 1* shows a driver Pre-emphasis waveform. The Pre-emphasis duration is 188ps nominal, corresponds to 0.47 bit-width at 2.5 Gbps. The Pre-emphasis levels of switch-side and line-side can be individually programmed.

TABLE 1. Logic Table For Multiplex Controls

MUX	Mux Function
0	MUX select switch input, IN1±.
1 (default)	MUX select switch input, IN0±.

TABLE 2. Logic Table For Loopback Controls

LB0	Loopback Function
0	Enable loopback from IN0± to OUT0±.
1 (default)	Normal mode. Loopback disabled.
LB1	**Loopback Function**
0	Enable loopback from IN1± to OUT1±.
1 (default)	Normal mode. Loopback disabled.

TABLE 3. Line-Side Pre-Emphasis Controls

DEL_[1:0]	Pre-Emphasis Level in mV$_{PP}$ (VODB)	Pre-Emphasis Level in mV$_{PP}$ (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 Board Trace
0 0	1300	1300	0	10 inches
0 1	1300	920	–3	20 inches
1 0	1300	650	–6	30 inches
1 1 (default)	1300	461	–9	40 inches

TABLE 4. Switch-Side Pre-Emphasis Controls

DES_[1:0]	Pre-Emphasis Level in mV$_{PP}$ (VODB)	Pre-Emphasis Level in mV$_{PP}$ (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 Board Trace
0 0	1300	1300	0	10 inches
0 1	1300	920	–3	20 inches
1 0	1300	650	–6	30 inches
1 1 (default)	1300	461	–9	40 inches

TABLE 5. EQ Controls For Line And Switch Sides

EQL or EQS	Equalizer Function
0	Enable equalization.
1 (default)	Normal mode. Equalization disabled.

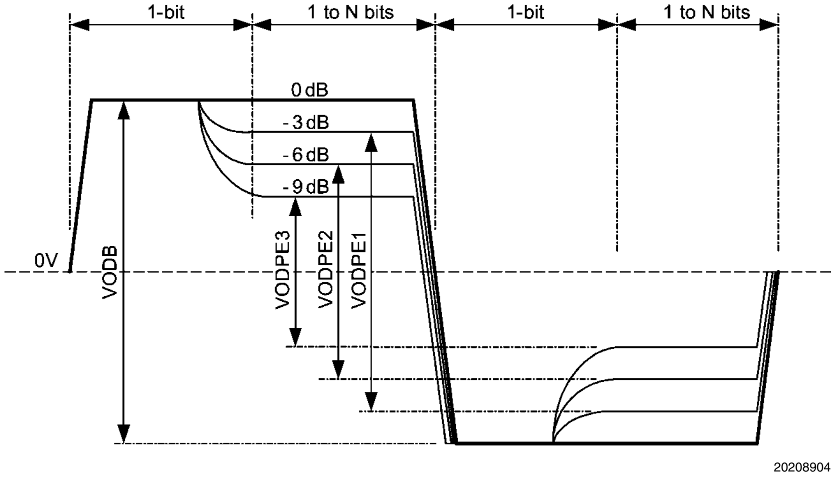


FIGURE 1. Driver Pre-Emphasis Differential Waveform (Showing All 4 Pre-Emphasis Steps)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.3V to 4V
CMOS/TTL Input Voltage	-0.3V to (V_{CC} +0.3V)
CML Input/Output Voltage	-0.3V to (V_{CC} +0.3V)
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature	
Soldering, 4 seconds	+260°C
Thermal Resistance, θ_{JA} (Note 8)	26.2°C/W
Thermal Resistance, θ_{JC}	3.3°C/W
Thermal Resistance, Φ_{JB}	11.1°C/W
ESD Rating (Note 10)	
HBM, 1.5 kΩ, 100 pF	6 kV
CDM	1.25 kV
MM	350V

Recommended Operating Ratings

	Min	Typ	Max	Units
Supply Voltage (V_{CC}-GND)	3.135	3.3	3.465	V
Supply Noise Amplitude 10 Hz to 2 GHz			100	mV_{PP}
Ambient Temperature	−40		85	°C
Case Temperature			100	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC} +0.3	V
V_{IL}	Low Level Input Voltage		-0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	-10		10	μA
I_{IL}	Low Level Input Current	V_{IN} = GND	75	94	124	μA
R_{PU}	Pull-High Resistance			35		kΩ
RECEIVER SPECIFICATIONS						
V_{ID}	Differential Input Voltage Range (Note 9)	AC Coupled Differential Signal Below 1.25 Gbps Above 1.25 Gbps This parameter is not tested at production	 100 100		 1750 1560	 mV_{P-P} mV_{P-P}
V_{ICM}	Common Mode Voltage at Receiver Inputs	Measured at receiver inputs reference to ground		1.3		V
R_{ITD}	Input Differential Termination (Note 3)	On-chip differential termination between IN+ or IN−	84	100	116	Ω
DRIVER SPECIFICATIONS						
V_{ODB}	Output Differential Voltage Swing without Pre-Emphasis (Note 4)	R_L = 100Ω ±1% DES_1=DES_0=0 DEL_1=DEL_0=0 Driver Pre-emphasis disabled Running K28.7 pattern at 2.5 Gbps See *Figure 5* for test circuit.	1100	1300	1500	mV_{P-P}
V_{PE}	Output Pre-Emphasis Voltage Ratio 20*log(VODPE/VODB)	R_L = 100Ω ±1% Running K28.7 pattern at 2.5 Gbps DEx_[1:0]=00 DEx_[1:0]=01 DEx_[1:0]=10 DEx_[1:0]=11 x=S for switch side Pre-emphasis control x=L for line side Pre-emphasis control See *Figure 1* on waveform. See *Figure 5* for test circuit.		 0 -3 -6 -9		 dB dB dB dB

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
T_{PE}	Pre-Emphasis Width	Tested at –9 dB Pre-emphasis level, DEx[1:0]=11 x=S for switch side Pre-emphasis control x=L for line side Pre-emphasis control See *Figure 4* on measurement condition.	125	188	250	ps
R_{OTSE}	Output Termination (Note 3)	On-chip termination from OUT+ or OUT– to V_{CC}	42	50	58	Ω
R_{OTD}	Output Differential Termination	On-chip differential termination between OUT+ and OUT–		100		Ω
ΔR_{OTSE}	Mis-Match in Output Termination Resistors	Mis-match in output terminations at OUT+ and OUT–			5	%
V_{OCM}	Output Common Mode Voltage			2.7		V
POWER DISSIPATION						
P_D	Power Dissipation	V_{DD} = 3.3V @ 25°C All outputs terminated by 100Ω ±1%. DEL_[1:0]=0, DES_[1:0]=0 Running PRBS 2^7-1 pattern at 2.5 Gbps		0.45		W
AC CHARACTERISTICS						
t_R	Differential Low to High Transition Time	Measured with a clock-like pattern at 2.5 Gbps, between 20% and 80% of the differential output voltage. Pre-emphasis disabled Transition time is measured with fixture as shown in *Figure 5*, adjusted to reflect the transition time at the output pins		100		ps
t_F	Differential High to Low Transition Time			100		ps
t_{PLH}	Differential Low to High Propagation Delay	Measured at 50% differential voltage from input to output			1	ns
t_{PHL}	Differential High to Low Propagation Delay				1	ns
t_{SKP}	Pulse Skew	$\lvert t_{PHL}–t_{PLH}\rvert$			20	ps
t_{SKO}	Output Skew (Note 7)	Difference in propagation delay between two outputs in the same device			100	ps
t_{SKPP}	Part-to-Part Skew	Difference in propagation delay between the same output from devices operating under identical conditions			100	ps
t_{SM}	Mux Switch Time	Measured from V_{IH} or V_{IL} of the mux-control or loopback control to 50% of the valid differential output		1.8	6	ns
RJ	Device Random Jitter (Note 5)	See *Figure 5* for test circuit. Alternating-1-0 pattern EQ and Pre-emphasis disabled. At 0.25 Gbps At 1.25 Gbps At 2.5 Gbps			2 2 2	psrms psrms psrms
DJ	Device Deterministic Jitter (Note 6)	See *Figure 5* for test circuit. EQ and Pre-emphasis disabled Between 0.25 and 2.5 Gbps with PRBS7 pattern for DS25MB100 @ –40°C to 85°C			35	Pspp
DR	Data Rate (Note 9)	Tested with alternating-1-0 pattern	0.25		2.5	Gbps

Note 1: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters measured at V_{CC} = 3.3V, T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 3: IN+ and IN– are generic names refer to one of the many pairs of complimentary inputs of the DS25MB100. OUT+ and OUT– are generic names refer to one of the many pairs of the complimentary outputs of the DS25MB100. Differential input voltage V_{ID} is defined as |IN+–IN–|. Differential output voltage V_{OD} is defined as |OUT+–OUT–|.

Note 4: K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000}

K28.5 pattern is a 20-bit repeating pattern of +K28.5 and –K28.5 code groups {110000 0101 001111 1010}

Note 5: Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation sqrt($RJ_{OUT}^2 – RJ_{IN}^2$), where RJ_{OUT} is the total random jitter measured at the output of the device in psrms, RJ_{IN} is the random jitter of the pattern generator driving the device.

Note 6: Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation ($DJ_{OUT}–DJ_{IN}$), where DJ_{OUT} is the total peak-to-peak deterministic jitter measured at the output of the device in pspp, DJ_{IN} is the peak-to-peak deterministic jitter of the pattern generator driving the device.

Note 7: t_{SKO} is the magnitude difference in the propagation delays among data paths. An example is the output skew among data paths from IN0± to OUT± and IN1± to OUT±. Another example is the output skew among data paths from IN± to OUT0± and IN± to OUT1±. t_{SKO} also refers to the delay skew of the loopback paths of the same port and between similar data paths. An example is the output skew among data paths IN0± to OUT0± and IN1± to OUT1±.

Note 8: Thermal resistances are based on having 16 thermal relief vias on the DAP pad under the 0 airflow condition.

Note 9: This parameter is guaranteed by design and/or characterization. It is not tested in production.

Note 10: ESD tests conform to the following standards:

Human Body Model applicable standard: MIL-STD-883, Method 3015.7
Machine Model applicable standard: JESD22-A115-A (ESD MM standard of JEDEC)
Field-induced Charge Device Model: Applicable standard JESD22-C101-C (ESD FICDM standard of JEDEC)

Timing Diagrams

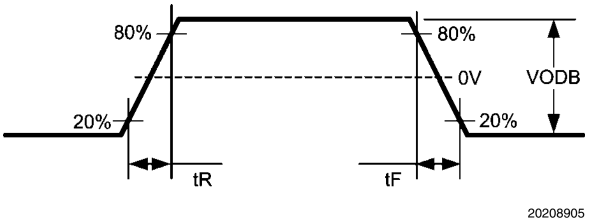


FIGURE 2. Driver Output Transition Time

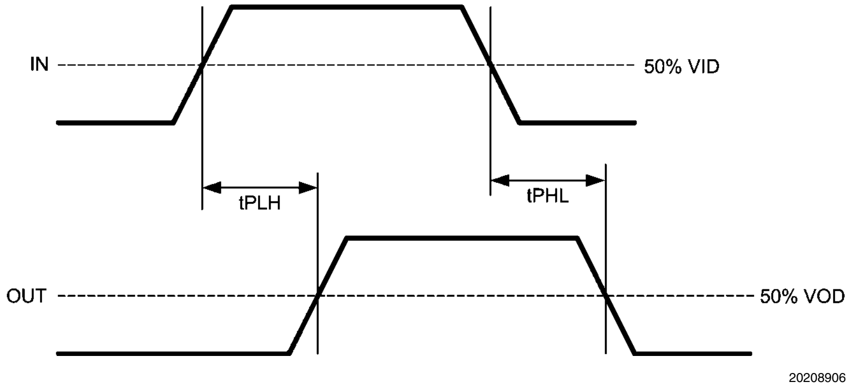


FIGURE 3. Propagation Delay from Input to Output

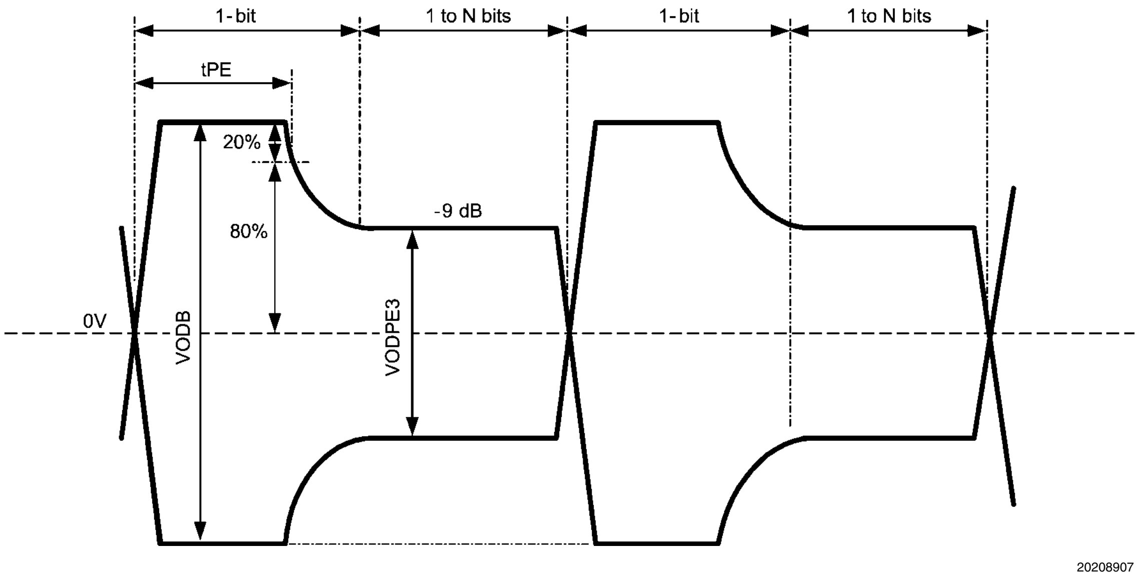

1-bit
1 to N bits
1-bit
1 to N bits
tPE
20%
80%
-9 dB
0V
VODB
VODPE3
20208907

FIGURE 4. Test Condition for Output Pre-Emphasis Duration

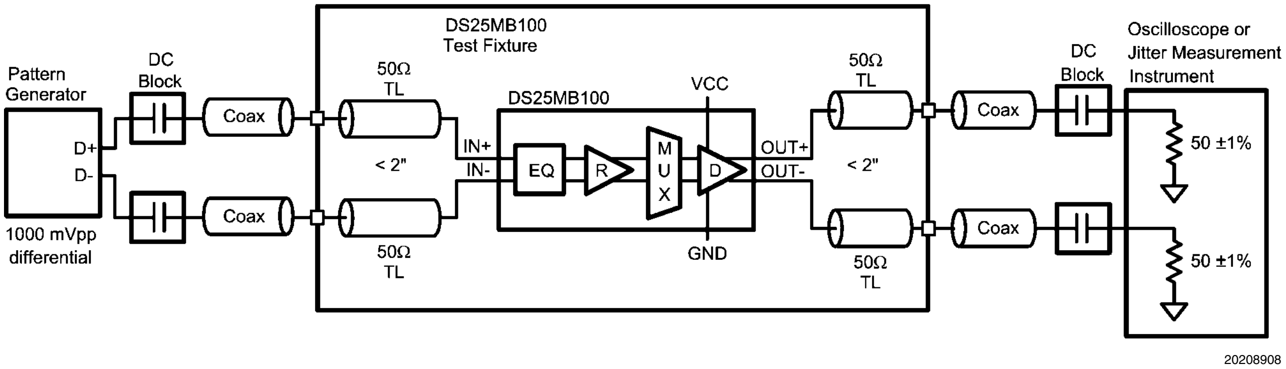

Pattern Generator
D+
D-
1000 mVpp differential
DC Block
Coax
DS25MB100 Test Fixture
50Ω TL
< 2"
DS25MB100
IN+
IN-
EQ
R
M U X
D
VCC
GND
OUT+
OUT-
Oscilloscope or Jitter Measurement Instrument
50 ±1%
20208908

FIGURE 5. AC Test Circuit

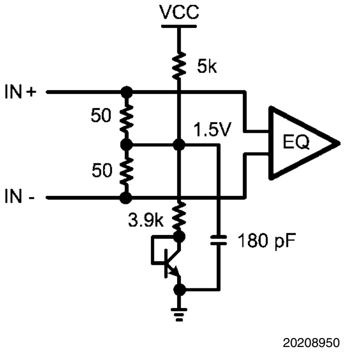

VCC
5k
IN+
50
1.5V
EQ
50
IN -
3.9k
180 pF
20208950

FIGURE 6. Receiver Input Termination and Bias Circuit

Application Information

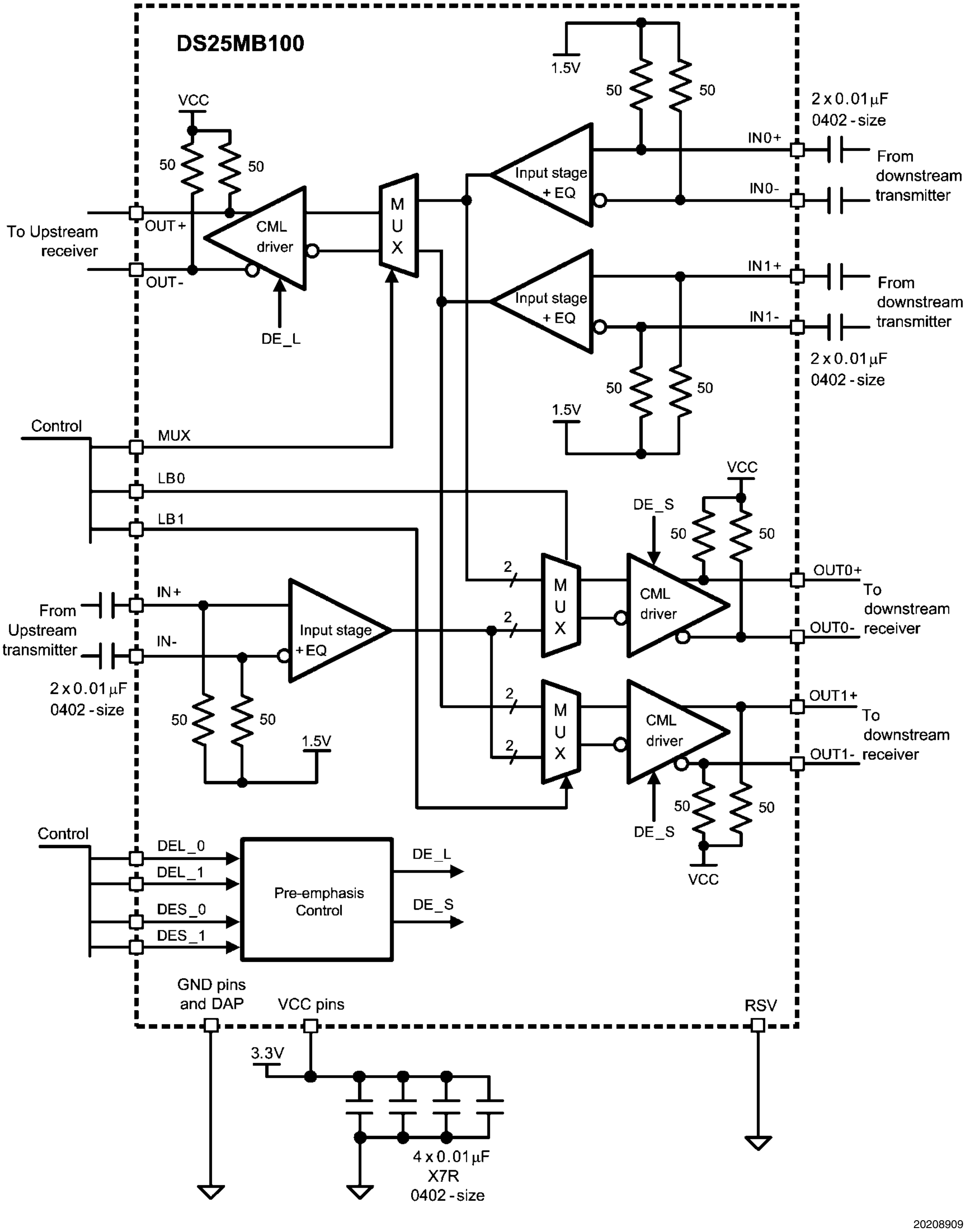

DS25MB100
1.5V
50
50
2 x 0.01 µF
0402 - size
IN0+
IN0-
From downstream transmitter
VCC
50
50
Input stage + EQ
M U X
CML driver
To Upstream receiver
OUT+
OUT-
DE_L
IN1+
IN1-
From downstream transmitter
2 x 0.01 µF
0402 - size
50
50
1.5V
Control
MUX
LB0
LB1
VCC
DE_S
50
50
2
M U X
CML driver
OUT0+
OUT0-
To downstream receiver
From Upstream transmitter
IN+
IN-
Input stage + EQ
2 x 0.01 µF
0402 - size
50
50
1.5V
OUT1+
OUT1-
To downstream receiver
DE_S
VCC
Control
DEL_0
DEL_1
DES_0
DES_1
Pre-emphasis Control
DE_L
DE_S
GND pins and DAP
VCC pins
RSV
3.3V
4 x 0.01 µF
X7R
0402 - size
20208909

FIGURE 7. Application Diagram

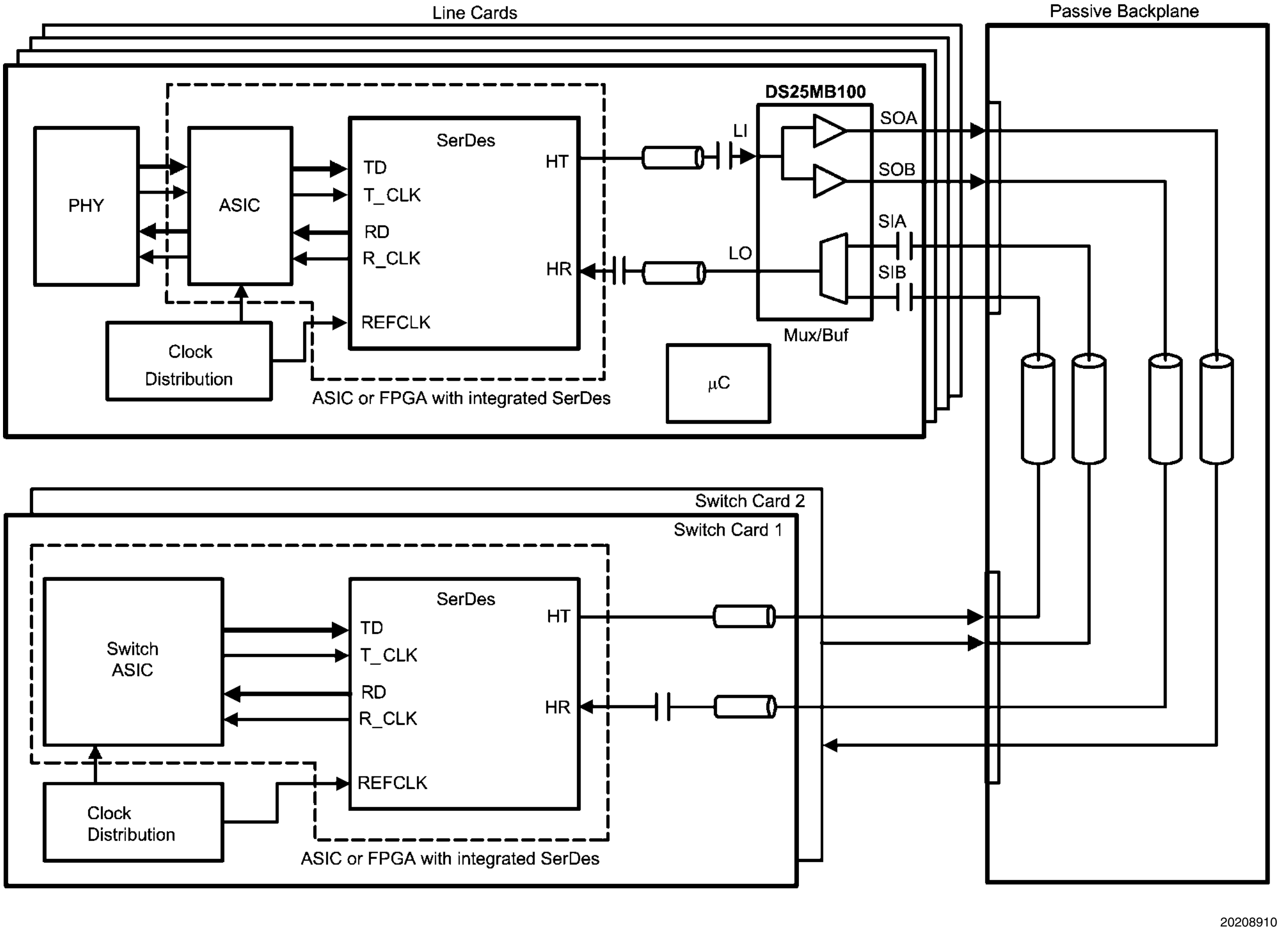
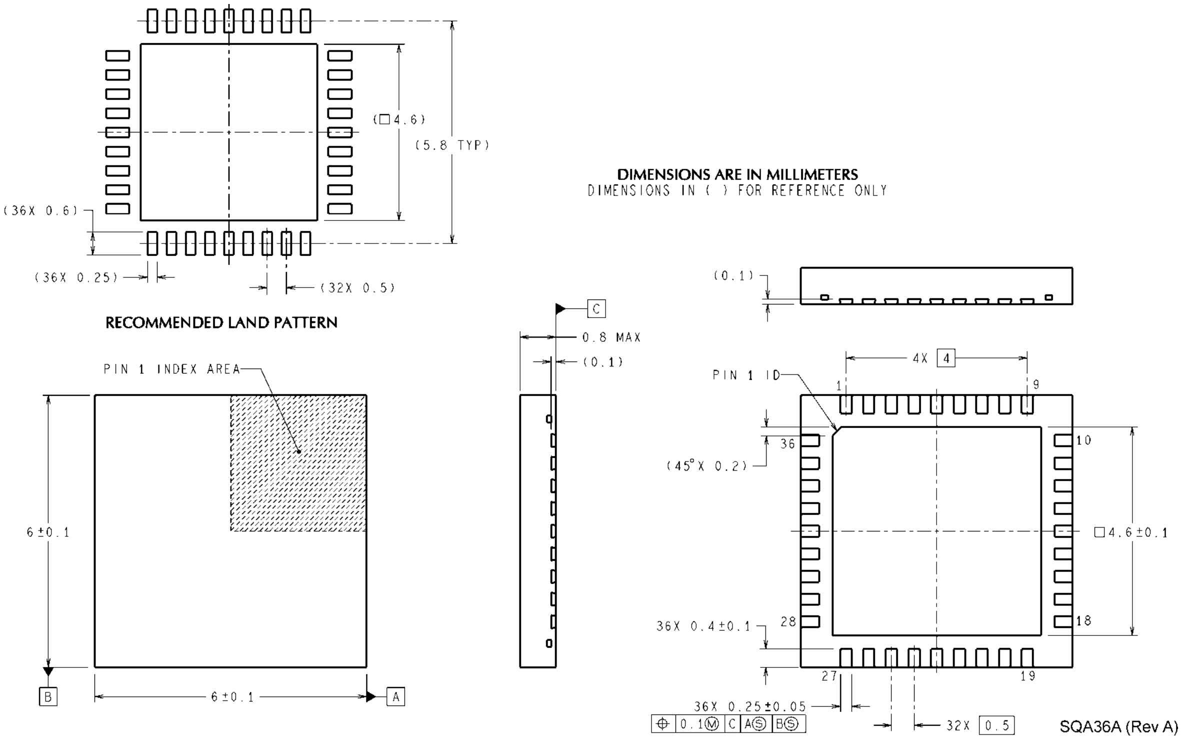

Line Cards
Passive Backplane
DS25MB100
PHY
ASIC
SerDes
TD
T_CLK
RD
R_CLK
HT
HR
REFCLK
LI
LO
SOA
SOB
SIA
SIB
Mux/Buf
Clock Distribution
ASIC or FPGA with integrated SerDes
µC
Switch Card 2
Switch Card 1
Switch ASIC
SerDes
TD
T_CLK
RD
R_CLK
HT
HR
REFCLK
Clock Distribution
ASIC or FPGA with integrated SerDes
20208910

FIGURE 8. Network Switch System With Redundancy

Physical Dimensions inches (millimeters) unless otherwise noted


(□4.6)
(5.8 TYP)
(36X 0.6)
(36X 0.25)
(32X 0.5)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
C
0.8 MAX
(0.1)
PIN 1 INDEX AREA
6 ±0.1
B
6 ±0.1
A
PIN 1 ID
4X 4
1
9
36
10
(45° X 0.2)
□4.6 ±0.1
36X 0.4±0.1
28
18
27
19
36X 0.25±0.05
⌖ 0.1Ⓜ C AⓈ BⓈ
32X 0.5
SQA36A (Rev A)

LLP-36 Package
Order Number DS25MB100TSQ
NS Package Number SQA36A

Notes

Notes

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Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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