

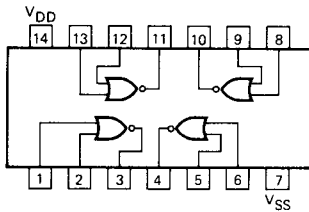
# 4001B

# 4002B

## QUAD 2-INPUT NOR GATE • DUAL 4-INPUT NOR GATE

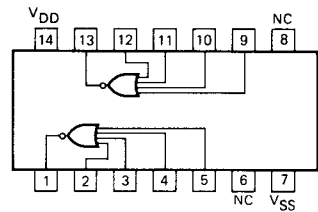
**DESCRIPTION** – These CMOS logic elements provide the positive input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

**4001B**  
LOGIC AND CONNECTION DIAGRAM  
DIP (TOP VIEW)



**NOTE:**  
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

**4002B**  
LOGIC AND CONNECTION DIAGRAM  
DIP (TOP VIEW)



**DC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0$  V

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS See Note 1		
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V							
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX					
$I_{DD}$	Quiescent Power	XC			1			2			4	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$	
					7.5			15			30		MAX		
	Supply Current	XM			0.25			0.5			1		$\mu$ A		MIN, 25°C
					7.5			15			30				MAX

**AC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$  C, 4001B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS See Note 2
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay		60	110		25	60		20	48	ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$
$t_{PHL}$			60	110		25	60		20	48	ns	
$t_{TLH}$	Output Transition Time		60	135		30	70		20	45	ns	Input Transition Times $\leq 20$ ns
$t_{THL}$			60	135		30	70		20	45	ns	

**AC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$  C, 4002B only

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS See Note 2
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay		65	110		30	60		20	48	ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$
$t_{PHL}$			70	110		30	60		23	48	ns	
$t_{TLH}$	Output Transition Time		75	135		40	70		30	45	ns	Input Transition Times $\leq 20$ ns
$t_{THL}$			60	135		23	70		15	45	ns	

**NOTES:**

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

