HARRIS SEMICONDUCTOR

HC-5524

SLIC
Subscriber Line Interface Circuit

March 1993

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and DLC Performance Requirements
- Controlled Supply of Battery Feed Current With Programmable Current Limit
- Operates with 5V Positive Supply ($V_{B}+$)
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On Chip Op-Amp for 2 Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBX's
- 2W/4W, 4W/2W Hybrid

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-5524-5	0°C to +75°C	28 Lead Ceramic DIP
HC1-5524-9	-40°C to +85°C	28 Lead Ceramic DIP
HC3-5524-5	0°C to +75°C	28 Lead Plastic DIP
HC3-5524-9	-40°C to +85°C	28 Lead Plastic DIP
HC4P5524-5	0°C to +75°C	44 Lead PLCC
HC4P5524-9	-40°C to +85°C	44 Lead PLCC
HC9P5524-5	0°C to +75°C	28 Lead SOIC
HC9P5524-9	-40°C to +85°C	28 Lead SOIC

Description

The HC-5524 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a 24V interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge, the device will withstand 500V induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

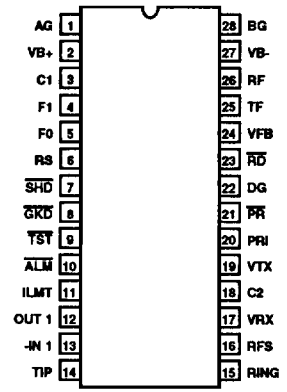
- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5524 SLIC is ideally suited for line card designs in PBX and DLC systems, replacing traditional transformer solutions.

Pinouts

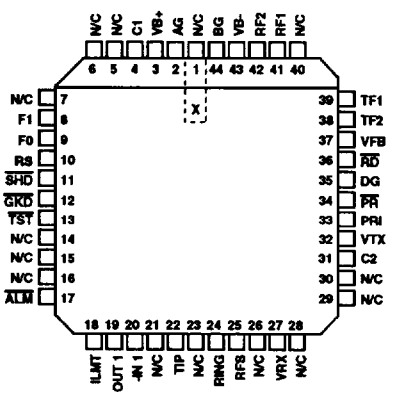
HC-5524 (PDIP, CDIP, SOIC)
TOP VIEW



TRUTH TABLE

F1	F0	Action
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active
1	0	Power Down Latch RESET
1	0	Power on RESET
1	1	Loop Power Denial Active

HC-5524 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2798.2**

Absolute Maximum Ratings (Note 1)

Maximum Supply Voltages (V_B+) ..... -0.5V to +7V
(V_B+) - (V_B-) ..... +40V
Relay Drive Voltage ..... -0.5V to +15V
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
HC-5524-5 ..... 0°C ≤ T_A ≤ +75°C
HC-5524-9 ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Relay Driver Voltage ..... +5V to +12V
Positive Power Supply (V_B+) ..... +5V ± 5%
Negative Power Supply (V_B-) ..... -20V to -28V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Typical Parameters are at T_A = +25°C, V_B+ = +5V, V_B- = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance, Unless Otherwise Specified.

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 2)	-	100	-	kΩ
TX Output Impedance		-	-	20	Ω
4W Input Overload Level	300Hz to 3.4kHz, 600Ω Reference	+1.0	-	-	V_{PEAK}
2W Return Loss	Matched for 600Ω (Note 2)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2W Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 2), 300Hz to 3400Hz	58	63	-	dB
4W Longitudinal Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 2), 300Hz to 3400Hz (Note 2)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-80	-67	dBmp
	I_{LINE} = 40mA, T_A = +25°C (Note 2)	-	10	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA, T_A = +25°C (Note 2)	-	-	40	mArms
Insertion Loss					
2W/4W	-1.58dBm at 1kHz, Referenced 600Ω	-	±0.05	±0.2	dB
4W/2W	0dBm at 1kHz, Referenced 600Ω	-	±0.05	±0.2	dB
4W/4W	-1.58dBm at 1kHz, Referenced 600Ω	-	-	±0.2	dB
Frequency Response	300Hz to 3400Hz (Note 2), Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.06	dB
Level Linearity 2W to 4W and 4W to 2W	Referenced to -10dBm (Note 2)				
	+3 to -40dBm	-	-	±0.08	dB
	-40 to -50dBm	-	-	±0.12	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 2)				
2W/4W	300Hz to 3400Hz	-	-	1	µs
4W/2W	300Hz to 3400Hz	-	-	1	µs
4W/4W	300Hz to 3400Hz	-	0.95	1.5	µs
Total Harmonic Distortion 2W/4W, 4W/2W, 4W/4W	Reference Level 0dBm at 600Ω, 300Hz to 3400Hz (Note 2)	-	-	-50	dB

Electrical Specifications Typical Parameters are at T_A = +25°C, V_{B+} = +5V, V_{B-} = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance, Unless Otherwise Specified. **(Continued)**

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
AC TRANSMISSION PARAMETERS (Continued)					
Idle Channel Noise 2W and 4W	(Note 2) C-Message	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	16	dBrn
Open Loop Voltage (V_{TIP} - V_{RING})	V_{B+} = +5V, V_{B-} = -24V	-	15.8	-	V
Power Supply Rejection Ratio	(Note 2)				
V_{B+} to 2W	30Hz to 200Hz, R_L = 600Ω	20	40	-	dB
V_{B+} to 4W		20	40	-	dB
V_{B-} to 2W		20	40	-	dB
V_{B-} to 4W		20	50	-	dB
V_{B+} to 2W	200Hz to 16kHz, R_L = 600Ω	30	40	-	dB
V_{B+} to 4W		20	28	-	dB
V_{B-} to 2W		20	50	-	dB
V_{B-} to 4W		20	50	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming Limit Range		20	40	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±4	±7	mA
Fault Currents					
TIP to Ground		-	30	-	mA
RING to Ground		-	120	-	mA
TIP and RING to Ground		-	150	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		-	10	-	mA
Thermal $\overline{ALM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	°C
Ring Trip Detection Threshold	V_{RING} = 105V_{RMS}, f_{RING} = 20Hz	-	10	-	mA
Ring Trip Detection Period		-	100	150	ms
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TST}$, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V

Electrical Specifications Typical Parameters are at T_A = +25°C, V_{B+} = +5V, V_{B-} = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance, Unless Otherwise Specified. **(Continued)**

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DC PARAMETERS (Continued)					
Input Current (F0, F1, RS, $\overline{TST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	60	-	mW
I_{B+}	V_{B+} = +5.25V, V_{B-} = -28V, $R_{LOOP} = \infty$	-	-	4	mA
I_{B-}	V_{B+} = +5.25V, V_{B-} = -28V, $R_{LOOP} = \infty$	-4	-	-	mA
I_{B+}	V_{B+} = +5V, V_{B-} = -24V, R_{LOOP} = 600Ω	-	3	6	mA
I_{B-}	V_{B+} = +5V, V_{B-} = -24V, R_{LOOP} = 600Ω	-28	-24	-	mA
UNCOMMITED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW	(Note 2)	-	1	-	MHz

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	VB+	Positive Voltage Source - Most Positive Supply.
3	4	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page.
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.

Pin Descriptions (Continued)

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
7	11	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table on front page.
10	17	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on front page. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduce component life.
11	18	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purposes.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	VRX	Receive Input, Four Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
19	32	VTX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	33	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	34	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	35	DG	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	36	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2 wire line.
24	37	VFB (Note 2)	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching. (This is not used in the typical applications circuit).
25	38	TF2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.
NA	39	TF1	Tie directly to TF2 in the PLCC application.
26	41	RF1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.

Pin Descriptions (Continued)

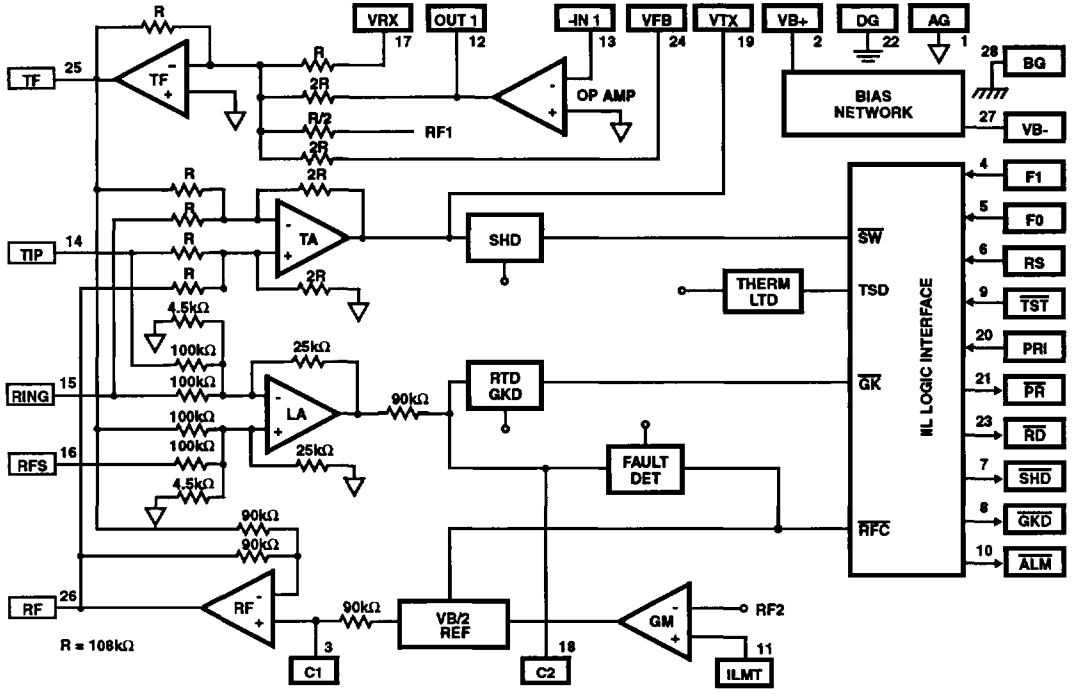
DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
NA	42	RF2	Tie directly to RF1 in the PLCC application.
27	43	VB-	The battery voltage source. The most negative supply.
28	44	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
	1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40	NC	No internal connection.

NOTES:

1. All grounds (AG, BG, DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Although not used in the typical applications circuit, V_{FB} may be used in matching complex 2-Wire impedances.

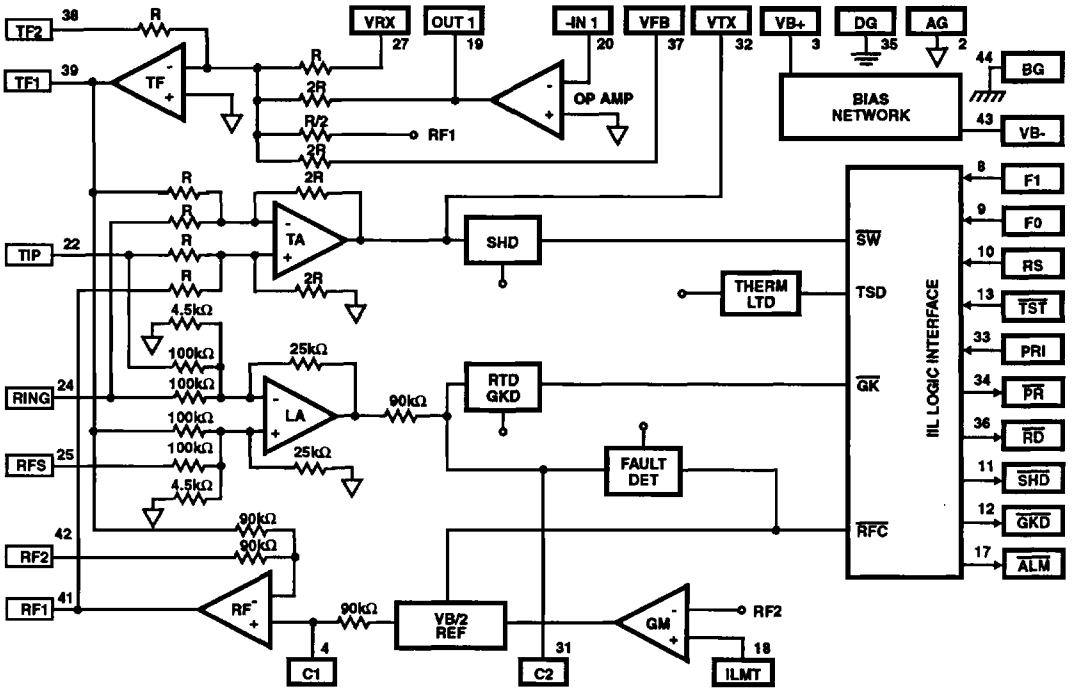
Functional Diagram

DIP OR SOIC



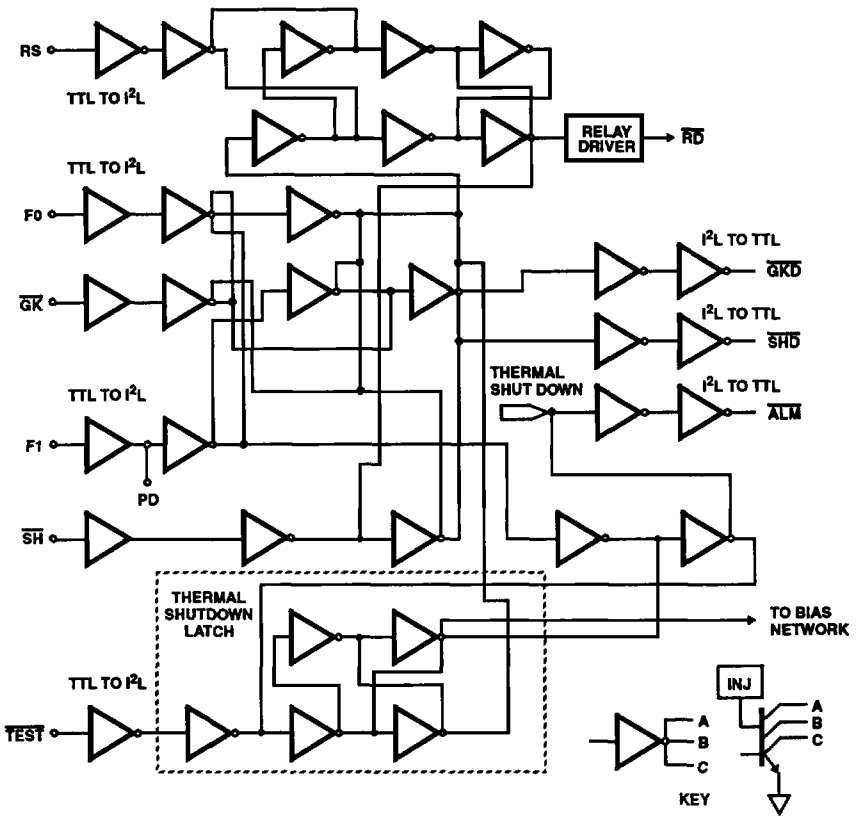
Functional Diagram (Continued)

PLCC



NOTE:
R = 108kΩ
NC = 1, 5, 6, 7, 14, 15, 16, 21
23, 26, 28, 29, 30, 40

Logic Diagram



Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions . . . . . 174 x 120 mils
Substrate Potential . . . . . Connected
Process . . . . . Bipolar-DI

Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	48	12
Plastic DIP	51	21
PLCC	47	17
SOIC	72	22

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 40mArms, 20mArms per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
T/GND	10µs Rise/	±1000 (Plastic)	V_{PEAK}
R/GND	1000µs Fall	±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to 10Arms	350 (Ceramic)	V_{RMS}

Applications Diagram

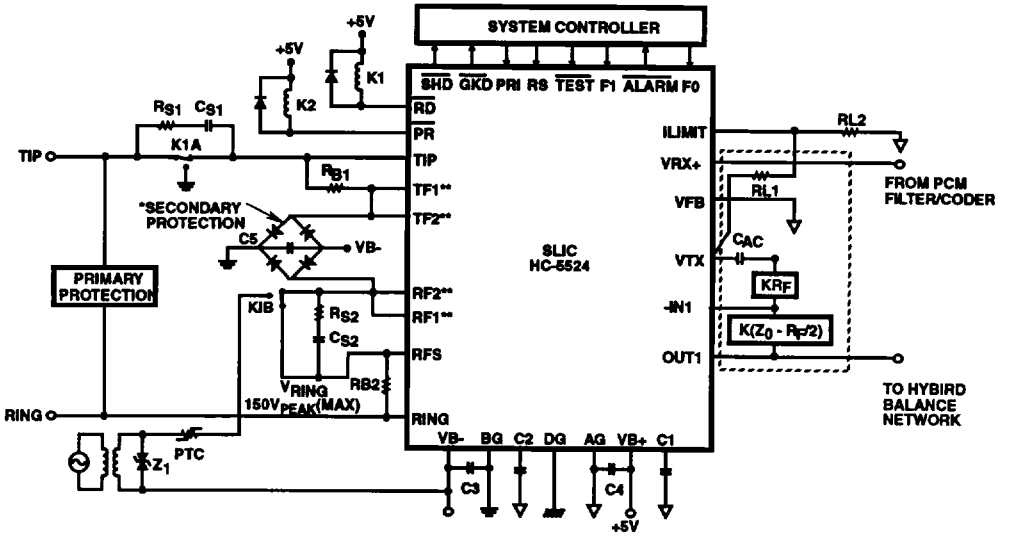


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C1 = 0.5µF, 20V

C2 = 0.5µF-1.0µF ±10%, 20V (Should be nonpolarized)

C3 = 0.01µF, 50V ±20%

C4 = 0.01µF, 50V ±20%

C5 = 0.01µF, 50V ±20%

C_{AC} = 0.5µF, 20V

$K(Z_0 - R_F/2)$ = 50kΩ, (Z_0 = 600Ω, K = Scaling Factor = 100)

RL1, RL2; Current Limit Setting Resistors

RL1+RL2 > 90kΩ

I_{LIMIT} = (.6) (RL1+RL2)/(200xRL2), RL1 typically 100kΩ

KR_F = 20kΩ, $R_F = 2(R_{B1}+R_{B2})$, K = Scaling Factor = 100)

$RB_1 = RB_2$ = 50Ω (1% absolute, matching requirements covered in a Tech Brief)

$R_{S1} = R_{S2}$ = 1kΩ typically

CS1 = CS2 = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

* Secondary protection diode bridge recommended is 3A, 200V type.

** TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

NOTES:

1. All grounds (AG, BG, & DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
2. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips