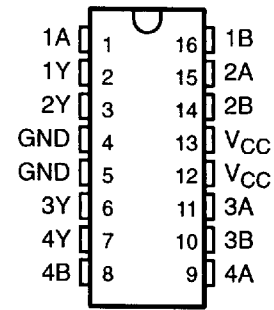


# 74ACT11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCAS008C – JULY 1987 – REVISED APRIL 1996

- Inputs Are TTL-Voltage Compatible
- Center-Pin  $V_{CC}$  and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages (D), Plastic Shrink Small-Outline Packages (DB), Plastic Thin Shrink Small-Outline Packages (PW), and Standard Plastic 300-mil DIPs (N)

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

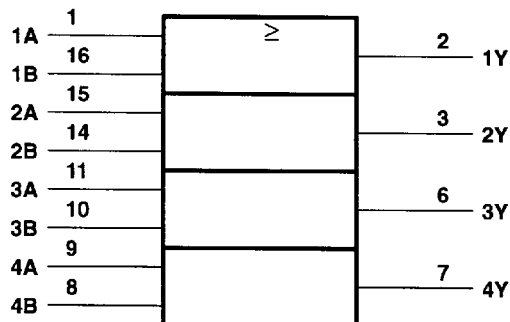
This device contains four independent 2-input OR gates. It performs the Boolean function  $Y = A + B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

The 74ACT11032 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

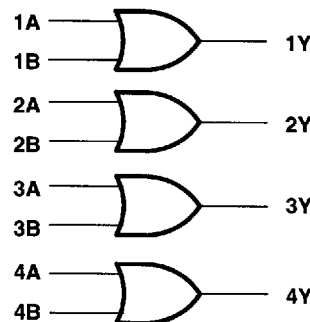
FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

■ 8961723 0105457 898 ■

# 74ACT11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCAS008C – JULY 1987 – REVISED APRIL 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 6V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–24	mA
$I_{OL}$ Low-level output current		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	ns/V
$T_A$ Operating free-air temperature	–40	85	°C



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**74ACT11032**  
**QUADRUPLE 2-INPUT POSITIVE-OR GATES**

SCAS008C - JULY 1987 - REVISED APRIL 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I <sub>OH</sub> = -75 mA†	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	0.1			0.1		V
		5.5 V	0.1			0.1		
	I <sub>OL</sub> = 24 mA	4.5 V	0.36			0.44		
		5.5 V	0.36			0.44		
I <sub>OL</sub> = 75 mA†	5.5 V				1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	4			40		μA
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V	0.9			1		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	3.5					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	1.5	6.2	8.1	1.5	9	ns
t <sub>PHL</sub>			1.5	4.9	7.4	1.5	8	

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	C <sub>L</sub> = 50 pF, f = 1 MHz	29	pF



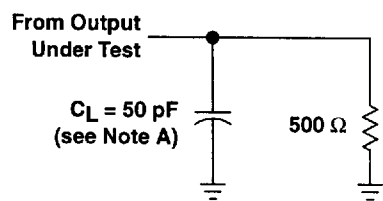
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

8961723 0105459 660

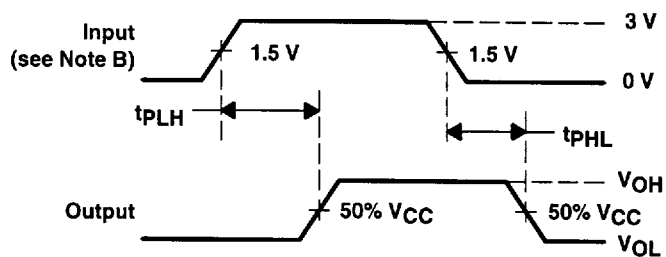
# 74ACT11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCAS008C – JULY 1987 – REVISED APRIL 1996

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms