4721B/4721BX

1024-BIT (256 x 4) RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

FAIRCHILD CMOS LSI

DESCRIPTION — The 4721B/4721BX is a 1024-Bit Random Access Memory, organized 256 words x 4 bits, with 3-state outputs. It has four Data Inputs (D_0-D_3), eight Address Inputs (A_0-A_7), an active LOW Write Enable Input ($\overline{WE}$), two Chip Select Inputs, one active LOW ($\overline{CS}_0$) and one active HIGH (CS_1), four 3-State Data Outputs (Q_0-Q_3) and an active LOW Output Enable Input ($\overline{EO}$).

Information on the Data Inputs (D_0-D_3) is written into the memory location selected by the Address Inputs (A_0-A_7) when $\overline{CS}_0$ and $\overline{WE}$ are LOW and CS_1 is HIGH. Under these conditions the Outputs (Q_0-Q_3) are held in a high impedance OFF state. Information is read from the memory location selected by the Address Inputs (A_0-A_7) while $\overline{CS}_0$ is LOW and CS_1 and $\overline{WE}$ are HIGH. When $\overline{CS}_0$ is HIGH or CS_1 is LOW all Outputs (Q_0-Q_3) are held in the high impedance OFF state. This allows other 3-state outputs to be wired together in a bus arrangement.

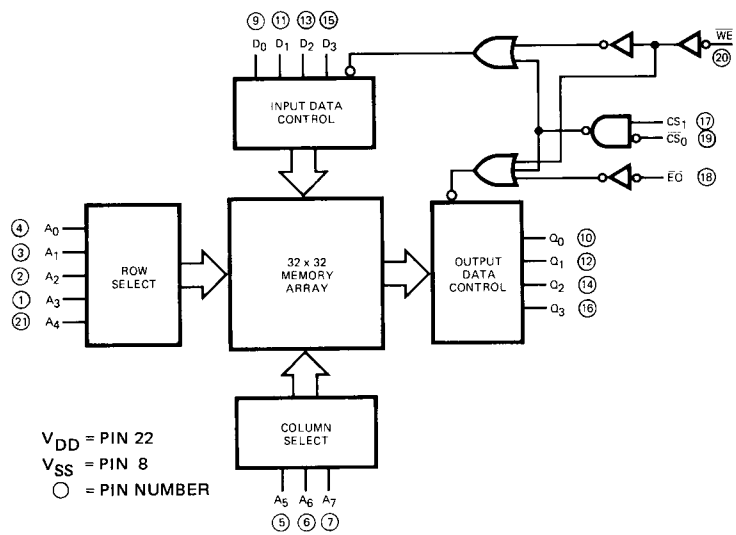
A HIGH on the active LOW Output Enable Input ($\overline{EO}$) forces all Data Outputs (Q_0-Q_3) to a high impedance OFF status regardless of all other input conditions. The 4721B/4721BX offers fully static operation. The 4721B is specified to operate over a power supply voltage range of 5 ± 0.5 V. The 4721BX is specified to operate over a power supply voltage range of 4.5 V to 12.5 V.

- **TYPICAL HOLDING VOLTAGE OF 1.5 V**
- **3-STATE OUTPUTS**
- **ORGANIZATION — 256 WORDS X 4 BITS**
- **ON-CHIP DECODING**
- **FULLY STATIC OPERATION**
- **LOW POWER DISSIPATION**
- **HIGH SPEED**
- **TWO CHIP SELECT INPUTS FOR EASY MEMORY EXPANSION**
- **ACTIVE LOW OUTPUT ENABLE INPUT**

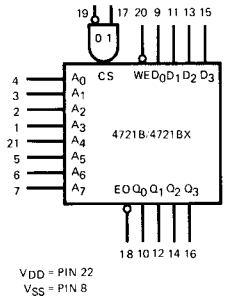
PIN NAMES

$A_0 - A_7$	Address Inputs
$D_0 - D_3$	Data Inputs
$\overline{CS}_0$, CS_1	Chip Select (Active LOW and Active HIGH) Inputs
$\overline{WE}$	Write Enable (Active LOW) Input
$Q_0 - Q_3$	Data Outputs
$\overline{EO}$	Output Enable (Active LOW) Input

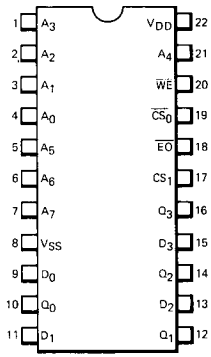
BLOCK DIAGRAM



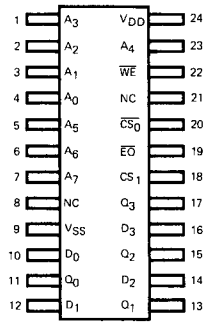
LOGIC SYMBOL



CONNECTION DIAGRAM DIP (TOP VIEW)



CONNECTION DIAGRAM FLATPAK (TOP VIEW)



MODE SELECTION

INPUTS				OUTPUTS	MODE
$\overline{EO}$	$\overline{CS_0}$	CS_1	$\overline{WE}$	Q_n	
H	X	X	X	High Impedance	Output Disabled
H	L	H	L	High Impedance	Write — Output Disabled
H	L	H	H	High Impedance	Output Disabled
L	H	X	X	High Impedance	Inhibit
L	X	L	X	High Impedance	Inhibit
L	L	H	L	Data Written Into Memory	Write — Transparent
L	L	H	H	Data Written Into Memory	READ

L = LOW Level
H = HIGH Level
X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

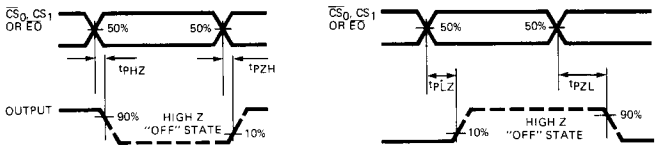
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 12.5 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	$\overline{CS_0}$ = V_{DD}, CS_1 = V_{SS} All inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35		MIN, 25°C	
					250			500			1000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

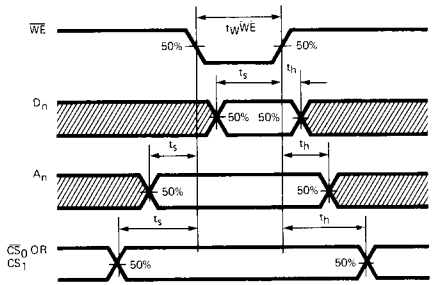
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 12.5 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PLH}	Propagation Delay,		420			240			180		ns	
t_{PHL}	Address to Output		420			240			180			
t_{PZH}	Enable Time, $\overline{CS_0}$, CS_1 or		150			70			50		ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}	$\overline{EO}$ to Output		150			70			50			(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Disable Time, $\overline{CS_0}$, CS_1 or		150			70			50		ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}	$\overline{EO}$ to Output		150			70			50			(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		75			35			25		ns	
t_{THL}			75			35			25			
	WRITE MODE											
$t_w\overline{WE}$	Minimum $\overline{WE}$ Pulse Width		180			100			80		ns	
t_s	Set-Up Time, D_n to $\overline{WE}$		150			120			115		ns	
t_h	Hold Time, D_n to $\overline{WE}$		40			20			15			
t_s	Set-Up Time, Address to $\overline{WE}$		150			120			115		ns	
t_h	Hold Time, Address to $\overline{WE}$		40			20			15			
t_s	Set-Up Time, $\overline{CS_0}$ or CS_1 to $\overline{WE}$		150			120			115		ns	
t_h	Hold Time, $\overline{CS_0}$ or CS_1 to $\overline{WE}$		40			20			15			

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

AC WAVEFORMS



OUTPUT ENABLE AND DISABLE TIMES



MINIMUM $\overline{WE}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{WE}$, A_n TO $\overline{WE}$, AND $\overline{CS}_0$ OR CS_1 TO $\overline{WE}$

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.