application INFO available

UC1714/5
UC2714/5
UC3714/5

Complementary Switch FET Drivers

FEATURES

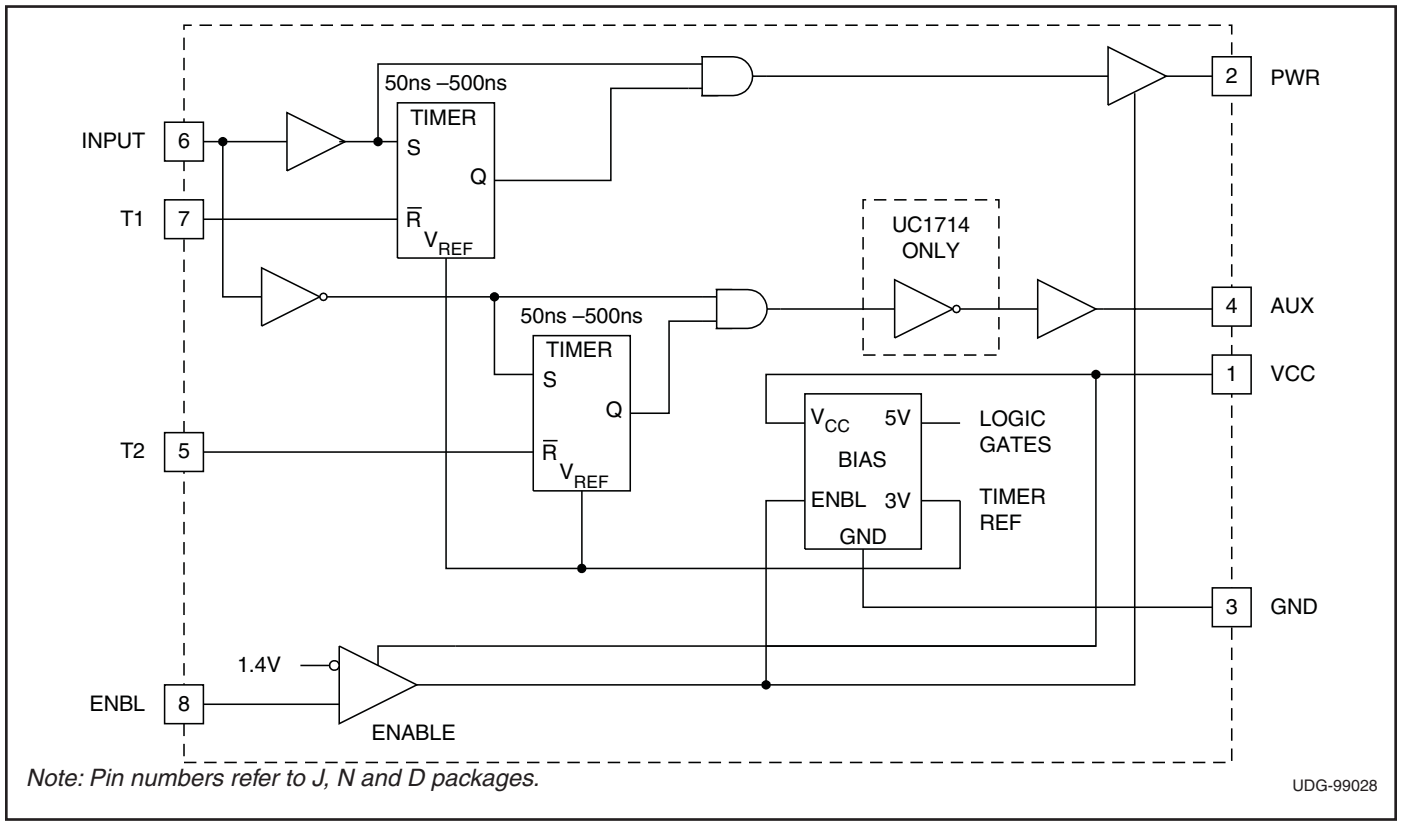
- Single Input (PWM and TTL Compatible)
- High Current Power FET Driver, 1.0A Source/2A Sink
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50ns to 500ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- Switching Frequency to 1MHz
- Typical 50ns Propagation Delays
- ENBL Pin Activates 220µA Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

DESCRIPTION

These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and can be interfaced with commonly available PWM controllers.

In the UC1714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC1715 series, the two outputs are configured in a true complementary fashion.

BLOCK DIAGRAM



Note: Pin numbers refer to J, N and D packages.

UDG-99028

ABSOLUTE MAXIMUM RATINGS

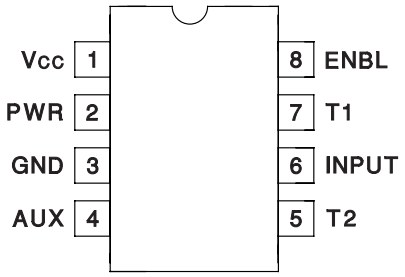
Supply Voltage V_{CC} 20V
Power Driver IOH
  continuous . . . . . –200mA
  peak . . . . . –1A
Power Driver IOL
  continuous 400mA
  peak 2A
Auxiliary Driver IOH
  continuous . . . . . –100mA
  peak . . . . . –500mA
Auxiliary Driver IOL
  continuous 200mA
  peak 1A

Input Voltage Range (INPUT, ENBL) . . . . . –0.3V to 20V
Storage Temperature Range . . . . . –65°C to 150°C
Operating Junction Temperature (Note 1) . . . . . 150°C
Lead Temperature (Soldering 10 seconds) . . . . . 300°C

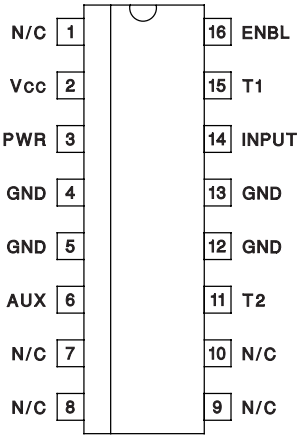
Note 1: *Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.*
Note 2*: Consult Packaging Section of databook for thermal limitations and specifications of packages.*

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J or N, D Packages



SOIC-16 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V, ENBL ≥ 2V, R_T1 = 100kΩ from T1 to GND, R_T2 = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
V_{CC}		7		20	V
I_{CC}, nominal	ENBL = 2.0V		18	24	mA
I_{CC}, sleep mode	ENBL = 0.8V		200	300	µA
Power Driver (PWR)					
Pre Turn-on PWR Output, Low	V_{CC} = 0V, I_{OUT} = 10mA, ENBL ® 0.8V		0.3	1.6	V
PWR Output Low, Sat. (V_{PWR})	INPUT = 0.8V, I_{OUT} = 40mA		0.3	0.8	V
	INPUT = 0.8V, I_{OUT} = 400mA		2.1	2.8	V
PWR Output High, Sat. (V_{CC} – V_{PWR})	INPUT = 2.0V, I_{OUT} = –20mA		2.1	3	V
	INPUT = 2.0V, I_{OUT} = –200mA		2.3	3	V
Rise Time	C_L = 2200pF		30	60	ns
Fall Time	C_L = 2200pF		25	60	ns
T1 Delay, AUX to PWR	INPUT rising edge, R_T1 = 10kΩ (Note 4)	20	35	80	ns
T1 Delay, AUX to PWR	INPUT rising edge, R_T1 = 100kΩ (Note 4)	350	500	700	ns
PWR Prop Delay	INPUT falling edge, 50% (Note 3)		35	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V, ENBL ≥ 2V, R_T1 = 100kΩ from T1 to GND, R_T2 = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Driver (AUX)					
AUX Output Low, Sat (V_{AUX})	V_{IN} = 2.0V, I_{OUT} = 20mA		0.3	0.8	V
	V_{IN} = 2.0V, I_{OUT} = 200mA		1.8	2.6	V
AUX Output High, Sat ($V_{CC} – V_{AUX}$)	V_{IN} = 0.8V, I_{OUT} = -10mA		2.1	3.0	V
	V_{IN} = 0.8V, I_{OUT} = -100mA		2.3	3.0	V
Rise Time	C_L = 1000pF		45	60	ns
Fall Time	C_L = 1000pF		30	60	ns
T2 Delay, PWR to AUX	INPUT falling edge, R_T2 = 10kΩ (Note 4)	20	50	80	ns
T2 Delay, PWR to AUX	INPUT falling edge, R_T2 = 100kΩ (Note 4)	250	350	550	ns
AUX Prop Delay	INPUT rising edge, 50% (Note 3)		35	80	ns
Enable (ENBL)					
Input Threshold		0.8	1.2	2.0	V
Input Current, I_{IH}	ENBL = 15V		1	10	µA
Input Current, I_{IL}	ENBL = 0V		–1	–10	µA
T1					
Current Limit	T1 = 0V		–1.6	–2	mA
Nominal Voltage at T1		2.7	3	3.3	V
Minimum T1 Delay	T1 = 2.5V, (Note 4)		40	70	ns
T2					
Current Limit	T2 = 0V		–1.2	–2	mA
Nominal Voltage at T2		2.7	3	3.3	V
Minumum T2 Delay	T2 = 2.5V, (Note 4)		50	100	ns
Input (INPUT)					
Input Threshold		0.8	1.4	2.0	V
Input Current, I_{IH}	INPUT = 15V		1	10	µA
Input Current, I_{IL}	INPUT = 0V		–5	–20	µA

Note 3: *Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.*

Note 4: *T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.*

PIN DESCRIPTIONS

AUX: The AUX switches immediately at INPUT's rising edge but waits through the T2 delay after INPUT's falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. See the Time Relationships diagram below for the difference between the UC1714 and UC1715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.

ENBL: The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into V_{CC} during the sleep mode is typically 220µA.

GND: This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.

PIN DESCRIPTIONS (cont.)

INPUT: The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0V to 20V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.

It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.

PWR: The PWR output waits for the T1 delay after the INPUT's rising edge before switching on, but switches off immediately at INPUT's falling edge (neglecting propagation delays). This output is capable of sourcing 1A and sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≥ 0.8V regardless of VCC's voltage.

T1: A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.

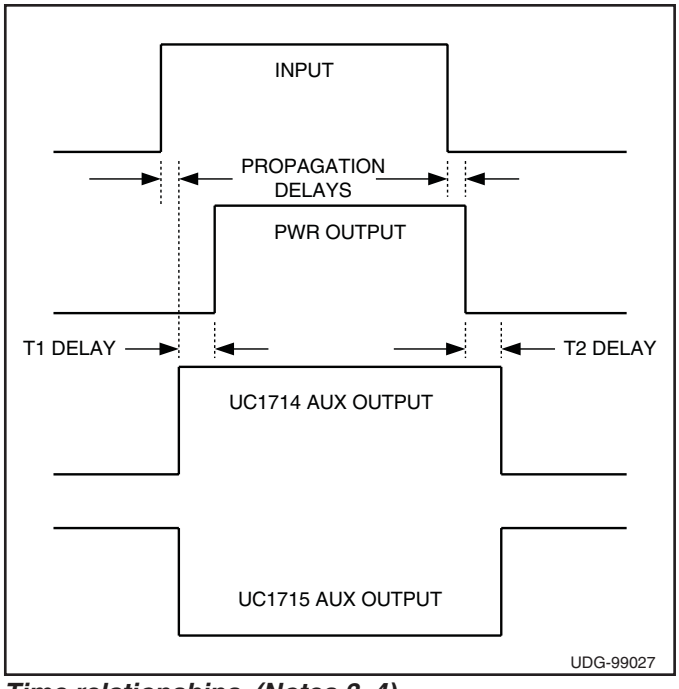
T2: This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch.

T1, T2: The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves.

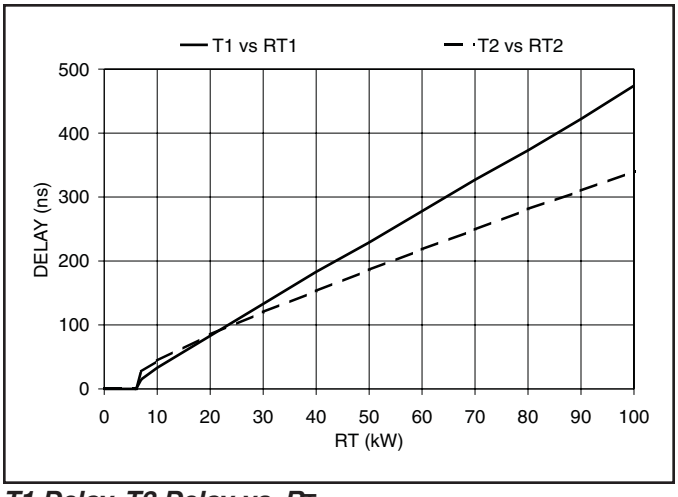
Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.

VCC: The V_{CC} input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

TYPICAL CHARACTERISTICS

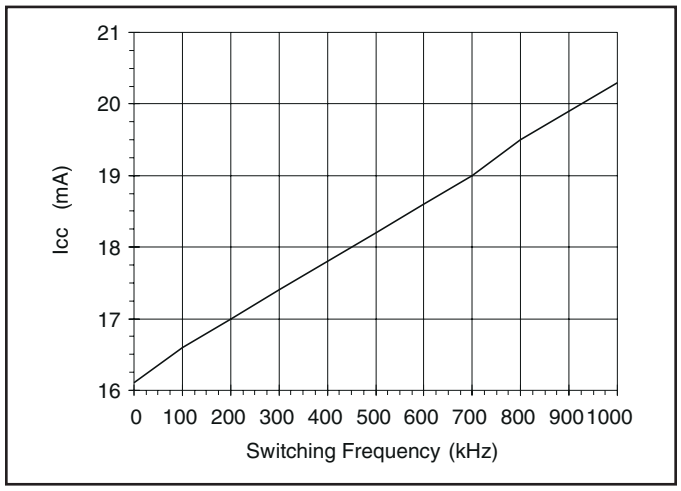


Time relationships. (Notes 3, 4)

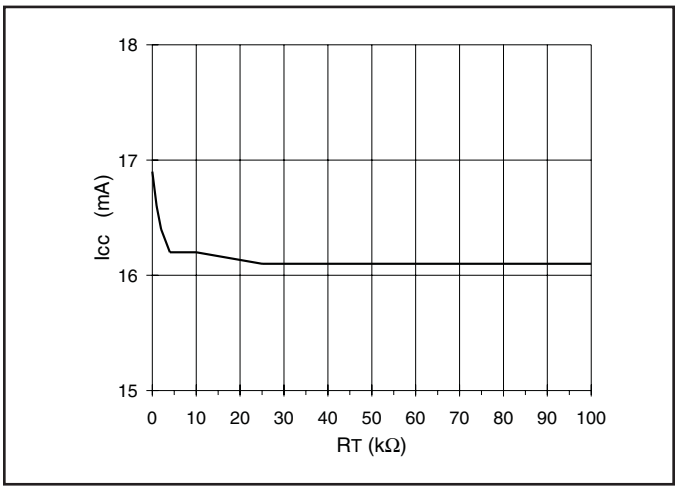


T1 Delay, T2 Delay vs. RT

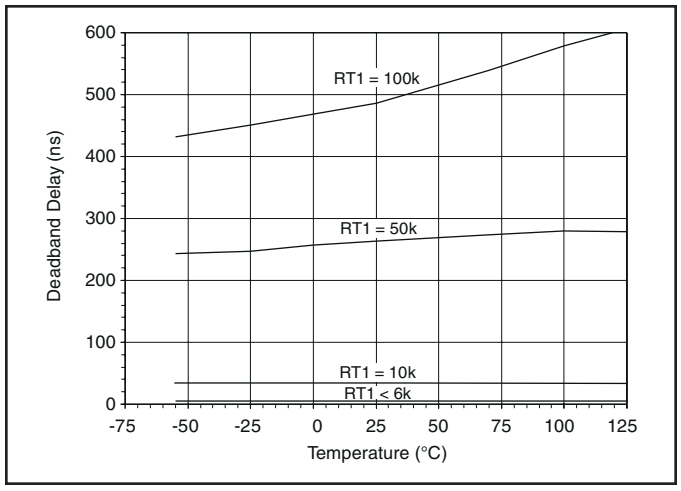
TYPICAL CHARACTERISTICS (cont.)



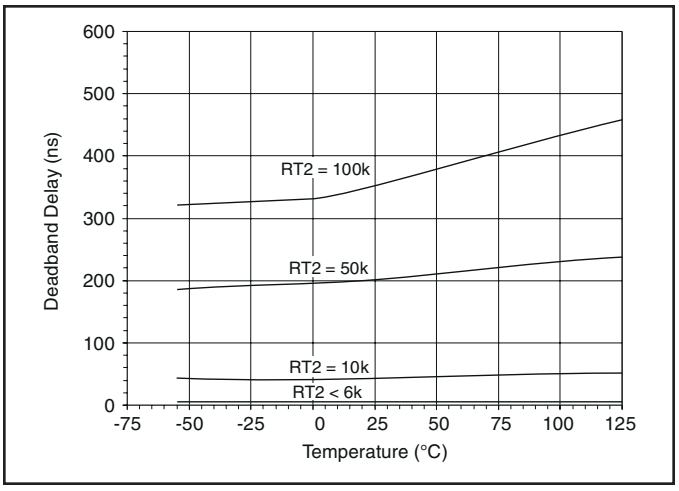
I_{CC} vs Switching Frequency with No Load and 50% Duty Cycle $R_T1 = R_T2 = 50k$



I_{CC} vs R_T with Opposite $R_T = 50k$



T1 Deadband vs. Temperature AUX to PWR



T2 Deadband vs. Temperature PWR to AUX

TYPICAL APPLICATIONS

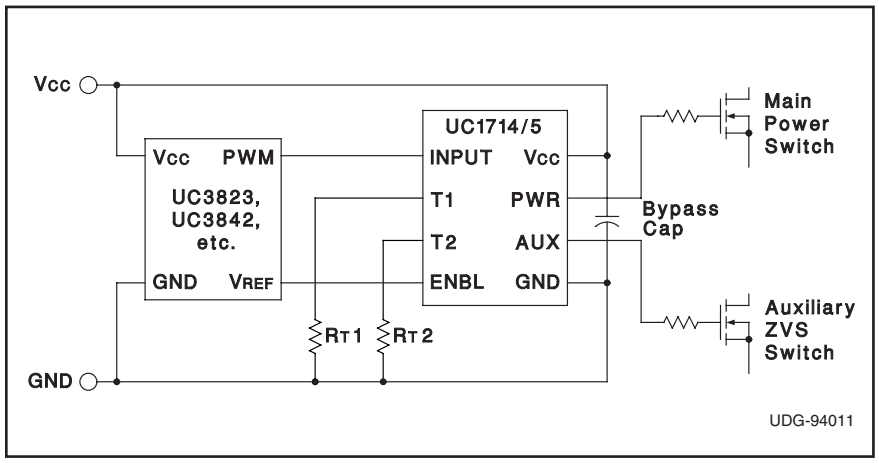


Figure 1. Typical application with timed delays.

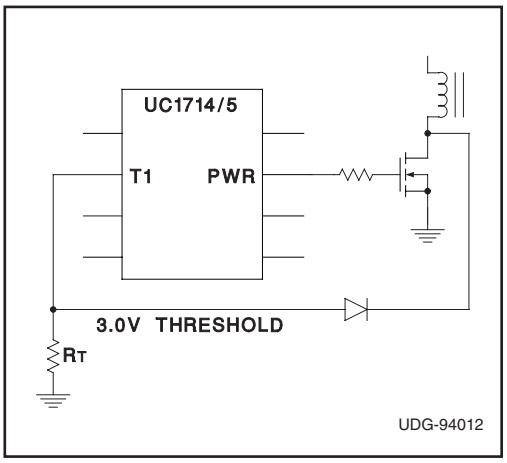


Figure 2. Using the timer input for zero-voltage sensing.

TYPICAL APPLICATIONS (cont.)

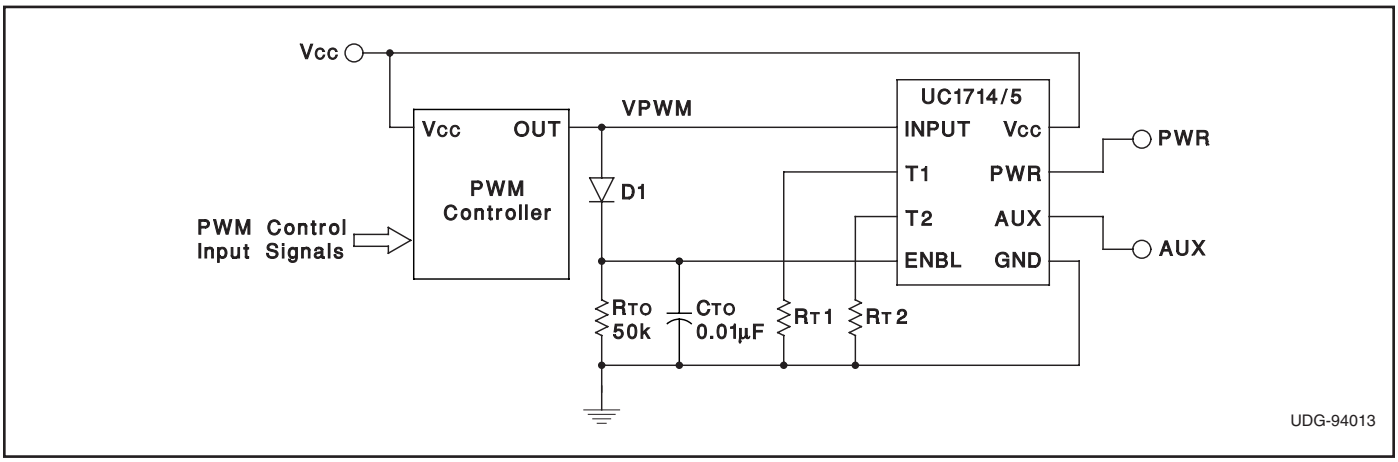


Figure 3. Self-actuated sleep mode with the absence of an input PWM signal. Wake up occurs with the first pulse while turn-off is determined by the (RTO CTO) time constant.

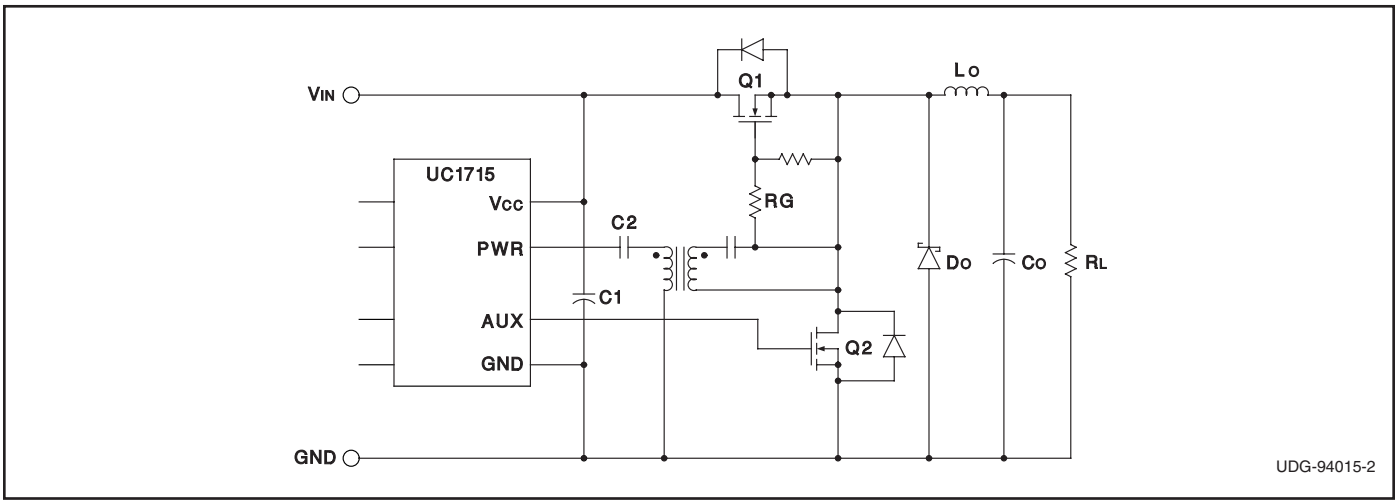


Figure 4. Using the UC1715 as a complementary synchronous rectifier switch driver with n-channel FETs

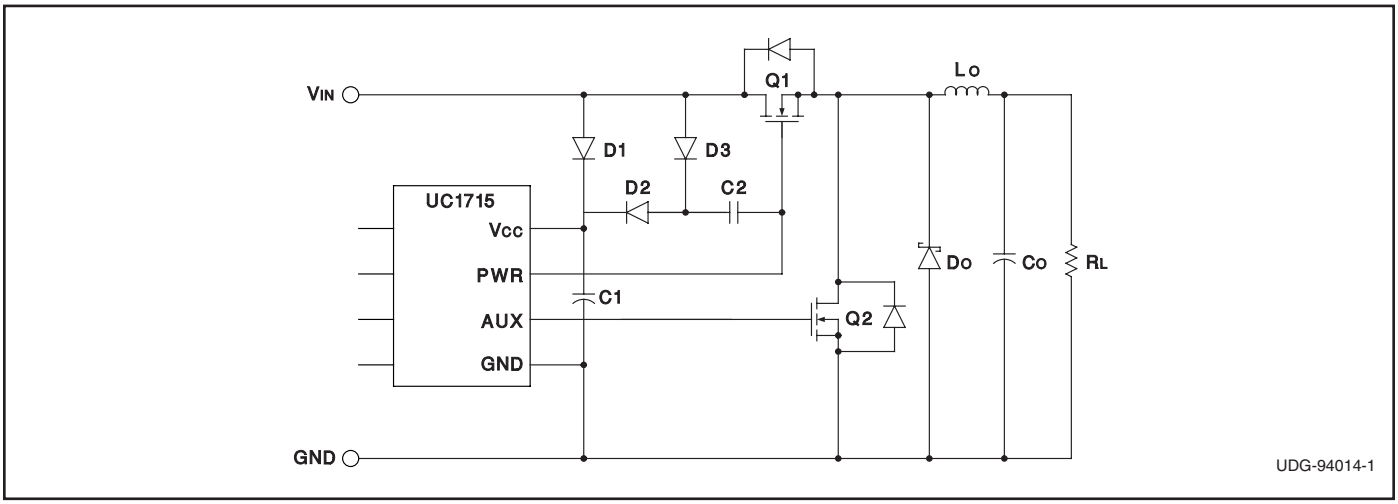


Figure 5. Synchronous rectifier application with a charge pump to drive the high-side n-channel buck switch. V_{IN} is limited to 10V as V_{CC} will rise to approximately $2V_{IN}$.

TYPICAL APPLICATIONS (cont.)

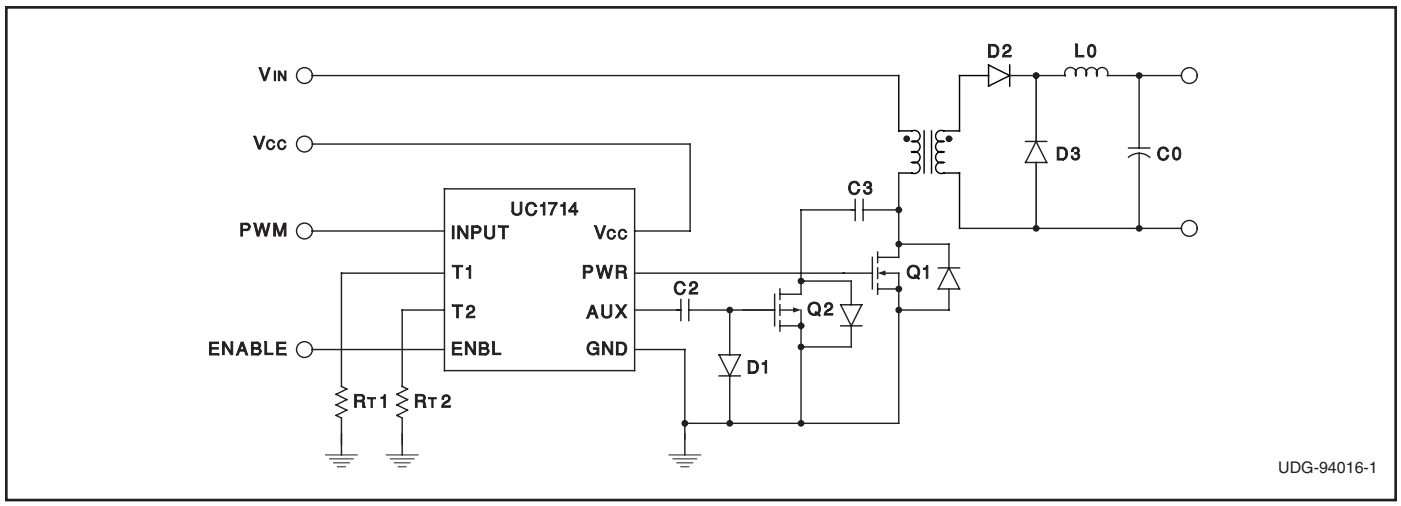


Figure 6. Typical forward converter topology with active reset provided by the UC1714 driving an N-channel switch (Q1) and a P-channel auxilliary switch (Q2).

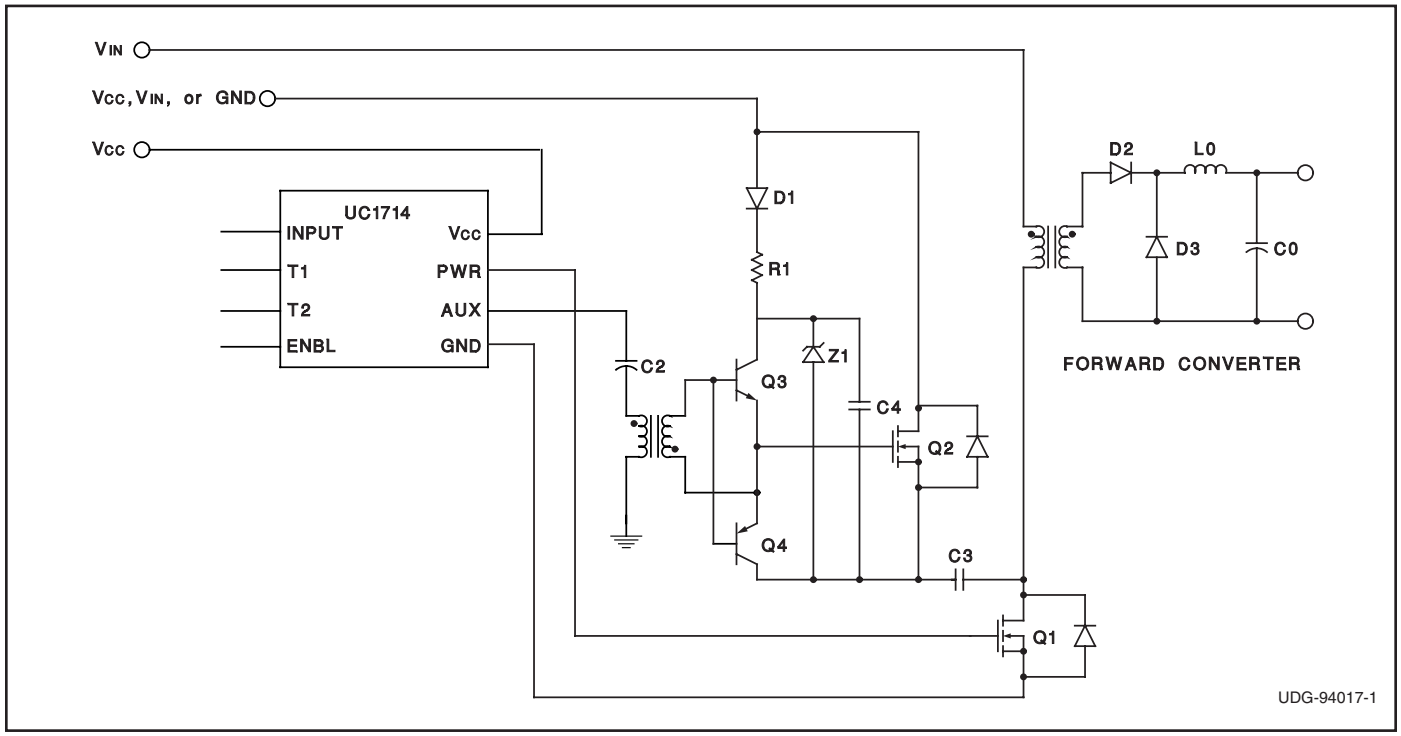


Figure 7. Using an N-channel active reset switch with a floating drive command.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC1714J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI
UC1715J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI
UC1715J883B	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI
UC2714D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2714DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2714DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2714DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2714DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2714DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2714N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2714NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2715DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC2715DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2715DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2715DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2715DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2715N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2715NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3714D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC3714DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC3714DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3714DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3714DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC3714DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC3714N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UC3714NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3715DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3715DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3715DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3715DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC3715DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
UC3715N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3715NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

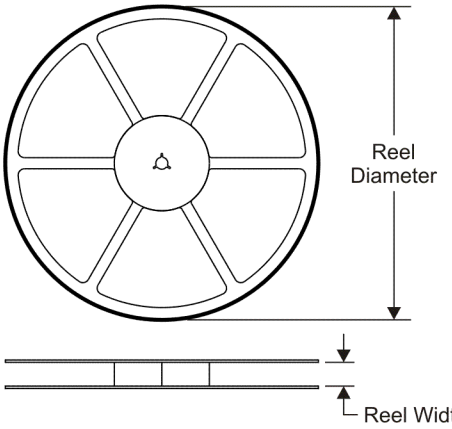
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

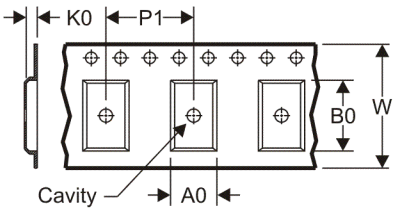
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

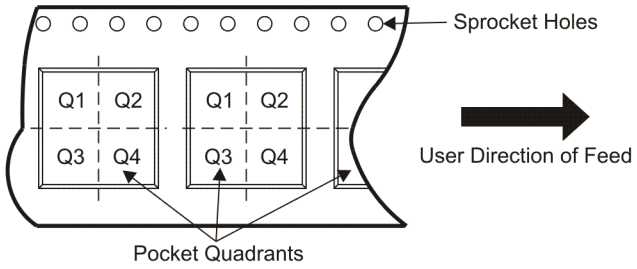


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

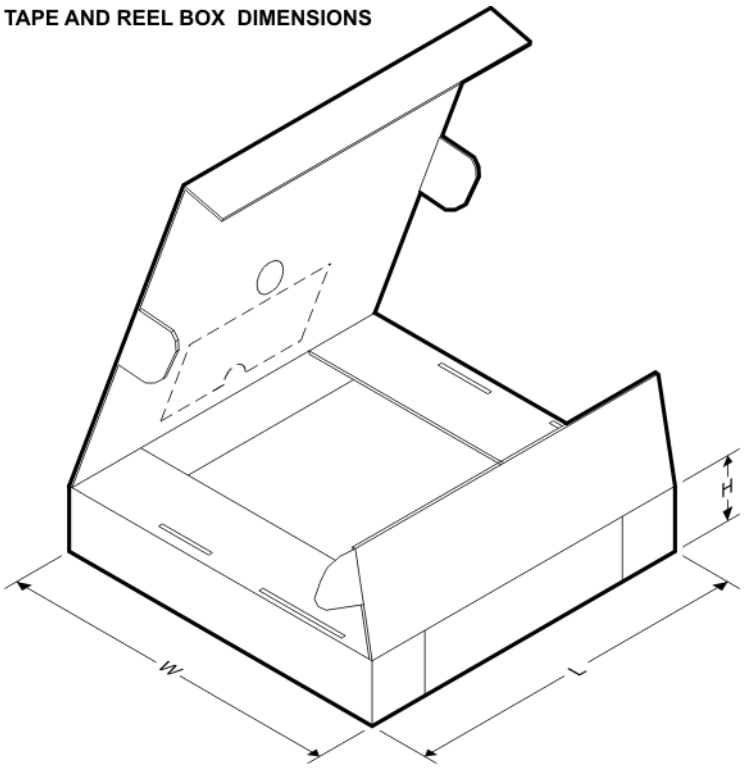
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2714DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2715DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3714DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3715DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2714DTR	SOIC	D	8	2500	346.0	346.0	29.0
UC2715DTR	SOIC	D	8	2500	346.0	346.0	29.0
UC3714DTR	SOIC	D	8	2500	346.0	346.0	29.0
UC3715DTR	SOIC	D	8	2500	346.0	346.0	29.0

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