

**FEATURES/BENEFITS**

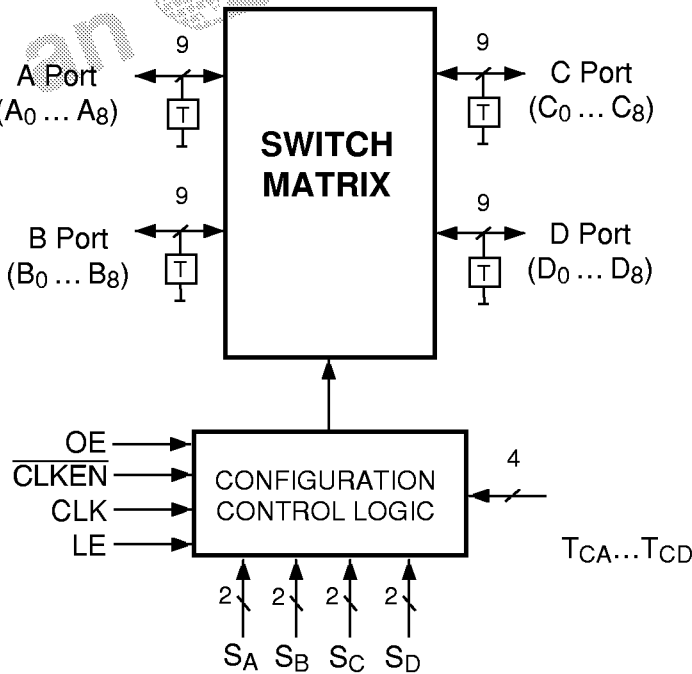
- Fully configurable Switch Matrix
- Sub-nanosecond Propagation Delay
- User-friendly Individual Port Control
- Power-on Reset
- Synchronous/Asynchronous Configuration Control
- Programmable Active Terminators on each Port
- Resistor options for line termination
- Available in 64-pin TQFP package

**DESCRIPTION**

The QS3B491 and QS3B2491 are high speed Crossbar switches organized as four independent 9-bit wide ports using QSI's 0.5micron CMOS technology. The switch matrix consists of N-channel FET switches controlled by the configuration logic. When closed, the switches permit bidirectional data flow with near-zero propagation delay. The N-channel FETs also facilitate 5V to 3.3V, and 5V to 2.5V voltage translation between ports.

The switch matrix can be configured for independent connection between any two ports as well as for multi-port broadcasting. Configuration control is either synchronous or asynchronous. In the

**Figure 1. Functional Block Diagram**



## QS3B491, QS3B2491 ADVANCE INFORMATION

synchronous mode, the control logic behaves like a Register. New configuration is stored on the positive edge of the Clock (CLK) if Clock Enable ( $\overline{\text{CLKEN}}$ ) is at logic LOW. In the Asynchronous mode, switch configuration logic behaves as a Transparent Latch under the control of LE signal. When LE is HIGH, the Latch is in the transparent mode. When LE is LOW, the configuration that meets the set-up time requirements is latched. An internal Power-ON Reset circuit disables all switches during power supply ramp-up and ramp-down.

Two port selection inputs are provided for port-independent interconnect control. Each port can be independently configured as a source or destination. This control scheme eliminates 'illegal' control input combinations.

Each I/O has a programmable Terminator with three modes of operation: OFF, Active Terminator (Last Value Latch), and Passive (Resistive) Terminator. Terminators for each port are connected to independent VBIAS pins ( $V_{BA} \dots V_{BD}$ ) and are controlled by independent Terminator Control (TCx) pins with three-state inputs. This control arrangement provides maximum flexibility for voltage translation between ports.

The QS3B491 is a low resistance Crossbar Switch, with ON resistance of  $9\Omega$  typical. The QS32491 adds an internal series resistor and is ideal for series termination of PCB traces and for the reduction of signal overshoots and undershoots.

**Table 1. Configuration Control**

Control Inputs				Mode	Status
CLKEN	CLK	LE	OE		
X	X	X	L	-	All Switches OFF
X	X	H	H	Asynch	Transparent Mode
H	X	L	H	Synch	Hold Previous Configuration
L	↑	L	H	Synch	Load Configuration
L	H	L	H	Asynch	Hold Previous Configuration
L	L	L	H	Asynch	Hold Previous Configuration

**Table 2. Port Selection Control**

S1A	S0A	A - Port Status
L	L	Source
L	H	Destination (B -> A)
H	L	Destination (C -> A)
H	H	Destination (D -> A)
S1B	S0B	B - Port Status
L	L	Destination (A -> B)
L	H	Source
H	L	Destination (C -> B)
H	H	Destination (D -> B)
S1C	S0C	C - Port Status
L	L	Destination (A -> C)
L	H	Destination (B -> C)
H	L	Source
H	H	Destination (D -> C)
S1D	S0D	D - Port Status
L	L	Destination (A -> D)
L	H	Destination (B -> D)
H	L	Destination (C -> D)
H	H	Source

Table 3. Terminator Control

TCA, TCB, TCC, TCD	Terminator Status
H	Active Terminator (Bus Hold) to $V_{BIAS}$ ( $V_{BA} \dots V_{BD}$ )
L	Resistor Termination to $V_{BIAS}$ ( $V_{BA} \dots V_{BD}$ )
OPEN	Terminator OFF

Figure 2. Pin Configuration  
(All Pins Top View)  
TQFP

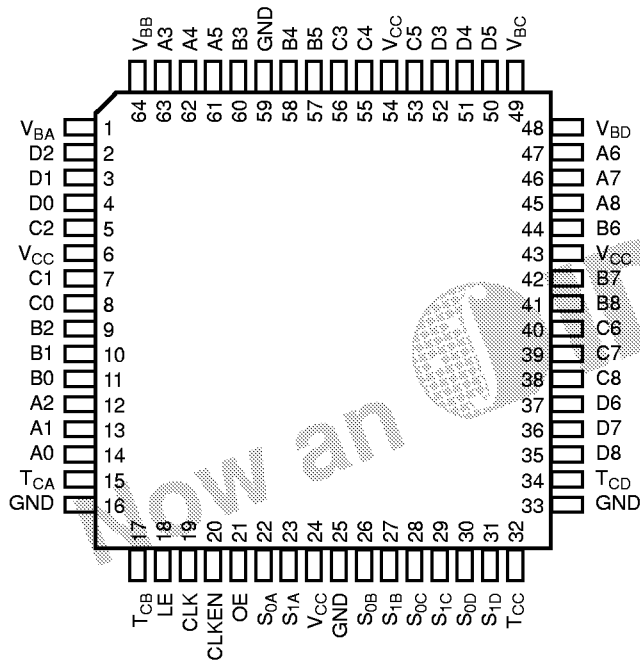


Table 4. Absolute Maximum Ratings

Supply Voltage to Ground .....	-0.5V to 7.0V
Bias Voltage to Ground .....	-0.5V to 7.0V
DC Switch Input Voltage .....	-0.5V to 7.0V
DC Control Input Voltage .....	-0.5V to 7.0V
AC Control Input Voltage (for pulse width $\leq$ 20ns) .....	-3.0V
DC Input Diode Current, $V_{IN} < 0$ .....	-20mA
DC I/O Current, Max. Sink Current Per Pin .....	100mA
Maximum Power Dissipation .....	1.0 watt
Storage Temperature Range .....	-65°C to 150°C

**Note:** ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated rating may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

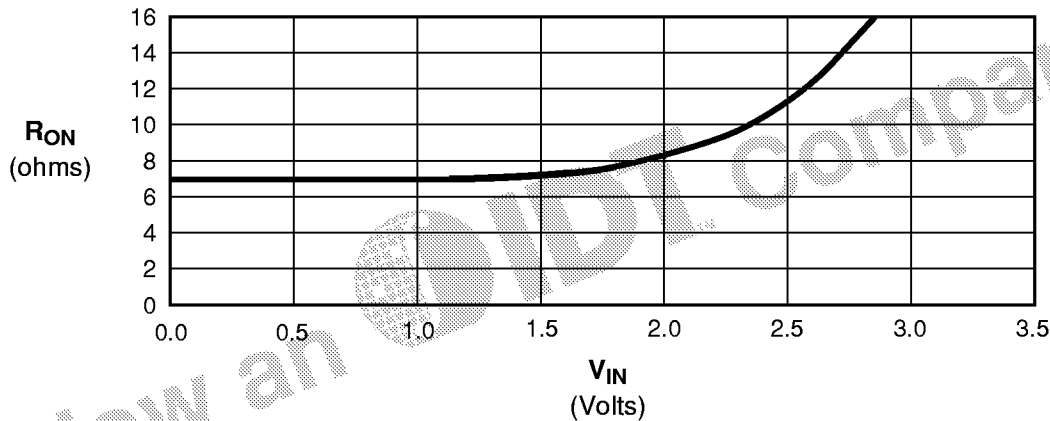
**Table 5. Capacitance**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	64-Pin TQFP		Units
	Typ	Max	
Control Inputs	5	7	pF
I/O (Switches OFF)	12	15	pF
I/O (One-to-one Channels)	25	30	pF

**Note:** Capacitance is characterized but not tested.

**Figure 3. Typical ON Resistance vs  $V_{IN}$  at 5.0  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$  (3B491)**



Note: For QS3B2491 add 25Ω to the above values.

**Table 6. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max	Unit
$I_{CCQ}$	Quiescent Power Supply Current	$V_{IN} = \text{GND}$ or $V_{CC}$ , $f = 0$ $V_{BIAS} = 5.5\text{V}$	600	$\mu\text{A}$
$\Delta I_{CC}$	Power Supply Current <sup>(2)</sup> per Input HIGH	$V_{IN} = 3.4\text{V}$ , $f = 0$ per Control Input	2.5	$\text{mA}$
$Q_{CCD}$	Dynamic Power Supply Current per MHz <sup>(3)</sup>	$V_{CC} = V_{BIAS} = 5.5\text{V}$ , Switching Pins Open Control Inputs Toggling @ 50% Duty Cycle		$\text{mA}/\text{MHz}$

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ , control inputs only). A and B pins do not contribute to  $I_{CC}$ .
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency.
4. This parameter is guaranteed but not production tested.

**QS3B491, QS3B2491 ADVANCE INFORMATION**

**TABLE 7. DC Electrical Characteristics Over Operating Range**

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit	
<b>A. CONTROL INPUTS</b>							
$V_{IH}$	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins, except $T_{CA}\dots T_{CD}$	2.0	—	—	V	
$V_{IL}$	Input LOW Voltage	Guaranteed Logic LOW for Control Pins, except $T_{CA}\dots T_{CD}$	—	—	0.8	V	
$V_{IHH}$	Input HIGH Voltage	3-Level Inputs Only $T_{CA}\dots T_{CD}$	$V_{CC}$ -1.0	—	—	V	
$V_{IMM}$	Input MID Voltage	3-Level Inputs Only $T_{CA}\dots T_{CD}$	$V_{CC}/2$ -0.5	—	$V_{CC}/2$ +0.5	V	
$V_{ILL}$	Input LOW Voltage	3-Level Inputs Only $T_{CA}\dots T_{CD}$	—	—	1.0	V	
$ I_{IN} $	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$ for Control Inputs, except $T_{CA}\dots T_{CD}$	—	0.02	1	$\mu\text{A}$	
$V_{IC}$	Input Clamp Voltage	$I_{IN} = -18\text{mA}$ , $V_{CC} = 4.5\text{V}$	—	—	-1.2	V	
<b>B. Switch I/O (A, B, C &amp; D Ports)</b>							
$ I_{OZ} $	Off-State Current (Hi-Z)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	0.02	1	$\mu\text{A}$	
$R_{ON}$	Switch On Resistance	$V_{CC} = \text{Min.}$ , $V_{IN} = 0.0\text{V}$ , $I_{ON} = 30\text{mA}$	3B491	—	8	10	$\Omega$
			3B2491	—	25	40	
		$V_{CC} = \text{Min.}$ , $V_{IN} = 2.4\text{V}$ , $I_{ON} = 15\text{mA}$	3B491	—	12	15	
			3B2491	—	30	45	
$I_{BHL}$ $I_{BHH}$	Input Hold Current <sup>(2,3)</sup> (A or B Port)	$V_{CC} = V_{BIAS} = 4.50\text{V}$ Switch OFF $T_{CA}\dots T_{CD} = \text{HIGH}$	$V_{IN} = 0.8\text{V}$ $V_{IN} = 2.0\text{V}$	75 -75	— —	— —	$\mu\text{A}$
$ I_{BH} $	Input Current <sup>(4)</sup> A,B Port	$V_{CC} = V_{BIAS} = 5.5\text{V}$ Switch OFF $T_{CA}\dots T_{CD} = \text{HIGH}$	$V_{IN} = 0$ , or $V_{CC}$ $0.8\text{V} < V_{IN} < 2.0\text{V}$	— —	— —	50 650 <sup>(5)</sup>	$\mu\text{A}$
$V_P$	Pass Voltage <sup>(5)</sup>	$V_{IN} = V_{CC} = 5\text{V}$ , $I_{OUT} = -5\mu\text{A}$	3.7	4.0	4.2	V	
$I_{IL}$	Input Current	$V_{CC} = V_{BIAS} = 4.5\text{V}$ $V_{IN} = 0\text{V}$ Switch OFF, $T_{CA}\dots T_{CD} = \text{LOW}$	—	-1	—	mA	

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2.  $I_{BHL}$  - Minimum sustaining "sink" current at the input for  $V_{IN} = 0.8\text{V}$ . Signifies the logic LOW latching capability.
3.  $I_{BHH}$  - Minimum sustaining "source" current at the input for  $V_{IN} = 2.0\text{V}$ . Signifies the logic HIGH latching capability.
4.  $|I_{BH}|$  - Magnitude of the input current specified under two conditions:
  - (a) Input voltage at GND or  $V_{CC}$ . This indicates the input current under steady-state condition.
  - (b) Input voltage between 0.8V and 2.0V (TTL input threshold range). This indicates the maximum input current during transient condition. The driver connected to the input must overcome this current requirement in order to switch the logic state of the Bus-hold circuit.
5. Pass voltage is guaranteed, but not production tested.

## QS3B491, QS3B2491 ADVANCE INFORMATION

**Table 8. Switching Characteristics Over Operating Range**

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 30\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted

Symbol	Description	Min	Typ	Max	Units
$t_{PLH}$	Single Channel Port-Port Propagation	—	0.5		ns
$t_{PHL}$	Delay (3B491)				
$t_{PLH}$	Single Channel Port-Port Propagation	—	1.5		ns
$t_{PHL}$	Delay (3B2491)				
$t_{PZL}$	Asynchronous Enable to Switch	1.5	—	6.5	ns
$t_{PZH}$	Turn-on Delay				
$t_{PLZ}$	Asynchronous Enable to Switch	1.5	—	5.5	ns
$t_{PHZ}$	Turn-off Delay				
$t_{PZL}$	Select Control to Switch Turn-on Delay	1.5	—	6.5	ns
$t_{PZH}$	(Asynchronous Mode)				
$t_{PLZ}$	Select Control to Switch Turn-off Delay	1.5	—	5.5	ns
$t_{PHZ}$	(Asynchronous Mode)				
$t_{PZL}$	CLK to Switch Turn-on Delay	1.5	—	6.5	ns
$t_{PZH}$	(Synchronous Mode)				
$t_{PLZ}$	CLK to Switch Turn-off Delay	1.5	—	5.5	ns
$t_{PHZ}$	(Synchronous Mode)				
$t_{SCS}$	Select Control Input to CLK Set-up Time	3	—		ns
$t_{HCS}$	Select Control Input to CLK Hold Time	0	—		ns
$t_{SEC}$	$\overline{\text{CLKEN}}$ to CLK Set-up Time	3	—		ns
$t_{HEC}$	$\overline{\text{CLKEN}}$ to CLK Hold Time	0	—		ns
$t_{SCL}$	Select Control Input to LE Set-up Time	3	—		ns
$t_{HCL}$	Select Control Input to LE Hold Time	0	—		ns
$t_W$	Clock Pulse Width (HIGH)	4	—		ns