TBB1004

Twin Built in Biasing Circuit MOS FET IC VHF/UHF RF Amplifier

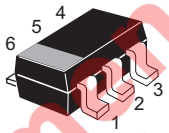
R07DS0314EJ1200
(Previous: REJ03G0842-1100)
Rev.12.00
Mar 28, 2011

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Built in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

RENESAS Package code: PTSP0006JA-A
(Package name: CMPAK-6)



1. Drain(1)
2. Source
3. Gate-1(1)
4. Gate-1(2)
5. Gate-2
6. Drain(2)

Notes: 1. Marking is “DM”.
2. TBB1004 is individual type number of RENESAS TWIN BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch[*3]	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 3. Value on the glass epoxy board (49mm × 38mm × 1mm).

Electrical Characteristics

The below specification are applicable for UHF unit (FET1)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5 V, V_{G2S} = 4 V I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V I_D = 100 µA
Drain current	$I_{D(op)}$	13	17	21	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 100 kΩ
Forward transfer admittance	$\|y_{fs}\|$	21	26	31	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ, f = 1 kHz
Input capacitance	Ciss	1.4	1.8	2.2	pF	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} =4 V, R_G = 100 kΩ f = 1 MHz
Output capacitance	Coss	1.0	1.4	1.8	pF	
Reverse transfer capacitance	Crss	—	0.02	0.04	pF	
Power gain	PG	16	21	—	dB	V_{DS} = V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ, f = 900 MHz Zi = S11*, Zo = S22*(:PG) Zi = S11opt (:NF)
Noise figure	NF	—	1.7	2.5	dB	

The below specification are applicable for VHF unit (FET2)

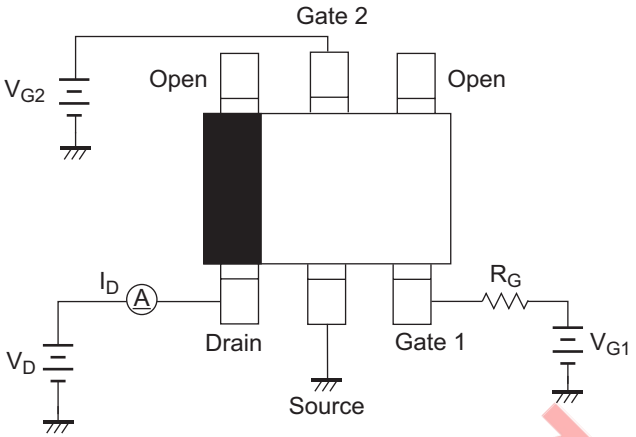
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5 V, V_{G2S} = 4 V I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V I_D = 100 µA
Drain current	$I_{D(op)}$	16	20	24	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 100 kΩ
Forward transfer admittance	$\|y_{fs}\|$	27	32	37	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ, f = 1 kHz
Input capacitance	Ciss	2.3	2.7	3.1	pF	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 100 kΩ f = 1 MHz
Output capacitance	Coss	1.4	1.8	2.2	pF	
Reverse transfer capacitance	Crss	—	0.03	0.05	pF	
Power gain	PG	24	29	—	dB	V_{DS} = V_{G1} = 5 V, V_{G2S} = 4 V R_G = 100 kΩ, f = 200 MHz
Noise figure	NF	—	1.2	1.7	dB	

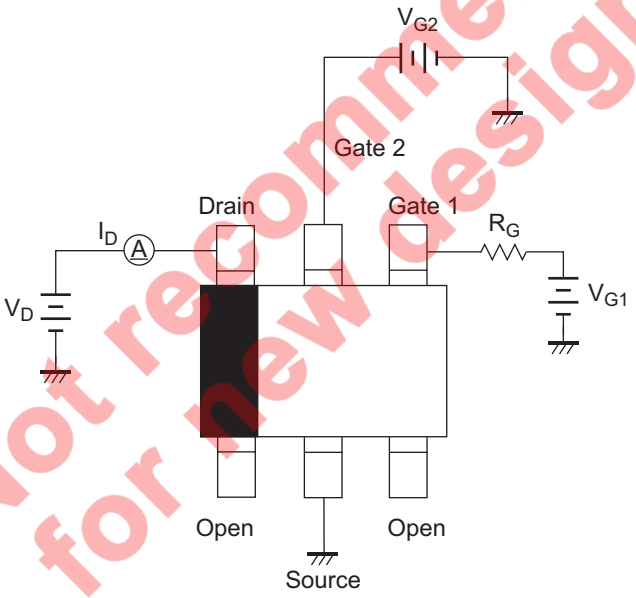
Test Circuits

- **DC Biasing Circuit for Operating Characteristic Items** ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

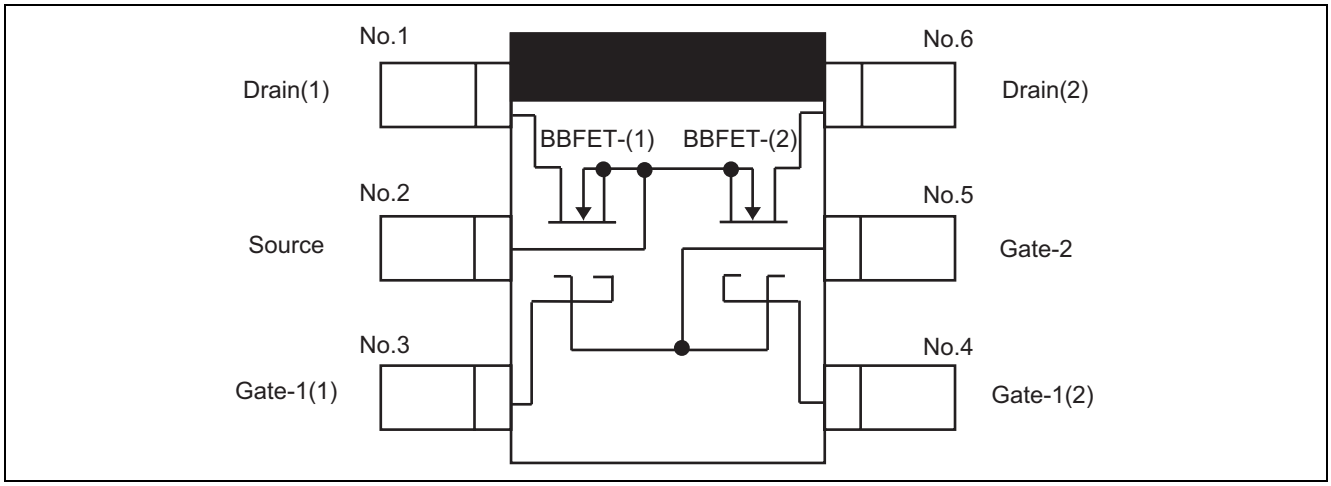
Measurment of FET1



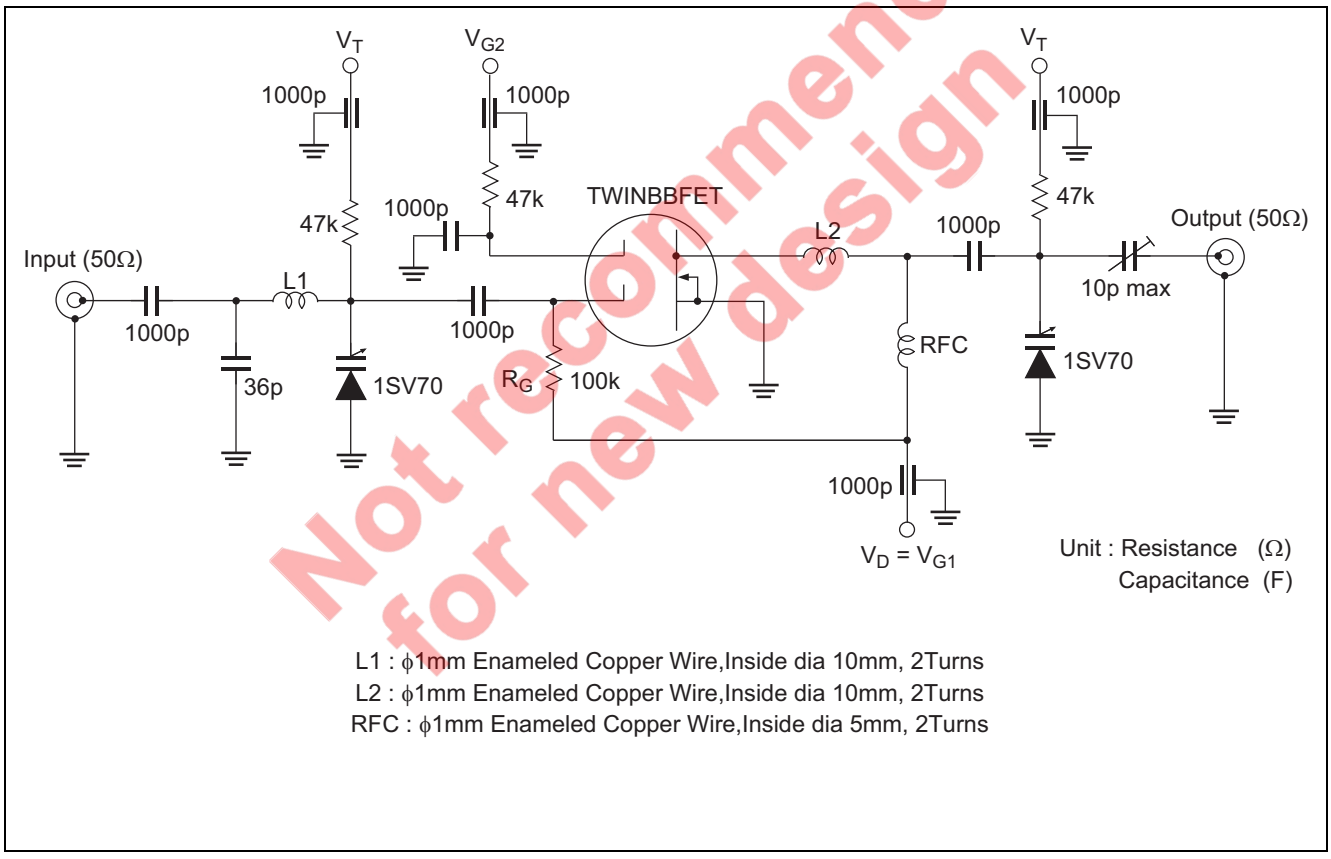
Measurment of FET2



- **Equivalent Circuit**

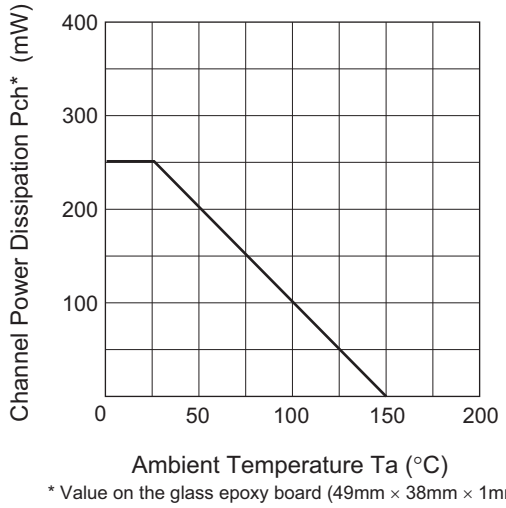


- **200 MHz Power Gain, Noise Figure Test Circuit**



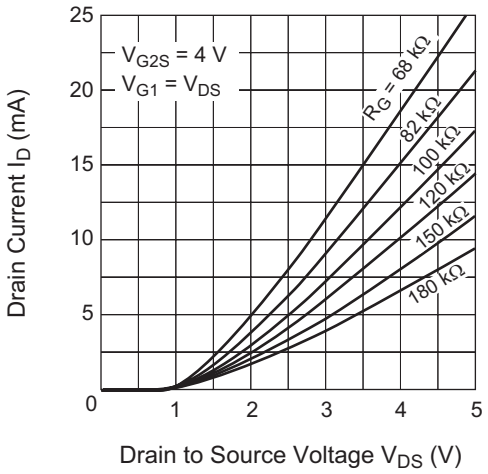
L1 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
L2 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
RFC : ϕ1mm Enameled Copper Wire,Inside dia 5mm, 2Turns

Maximum Channel Power Dissipation Curve

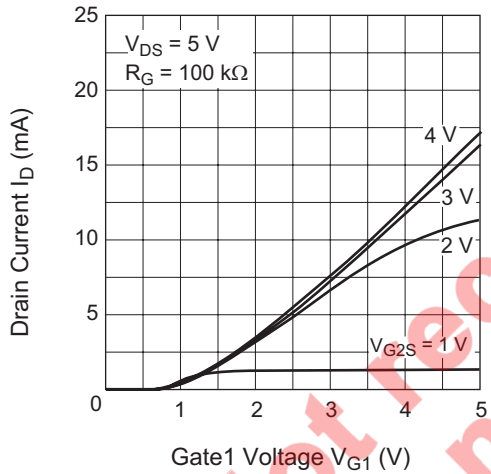


* Value on the glass epoxy board (49mm × 38mm × 1mm)

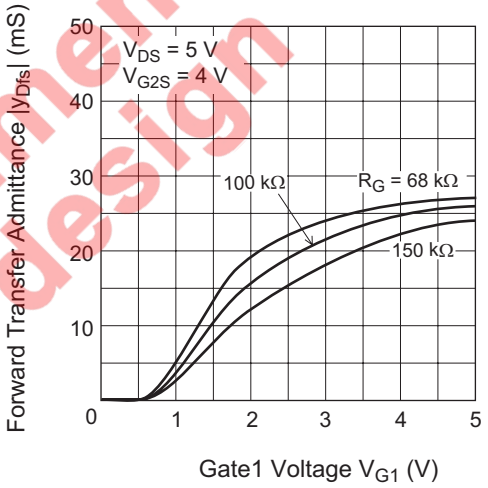
Typical Output Characteristics (FET1)



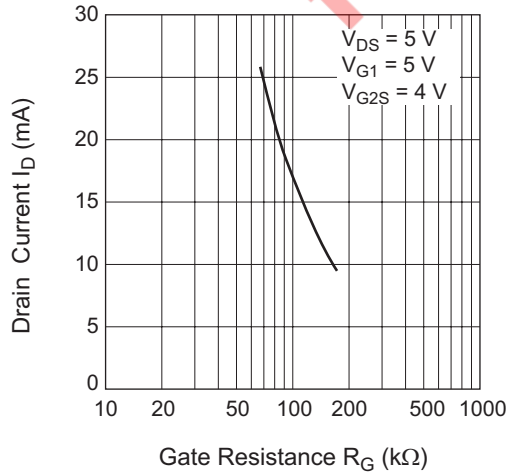
Drain Current vs. Gate1 Voltage (FET1)



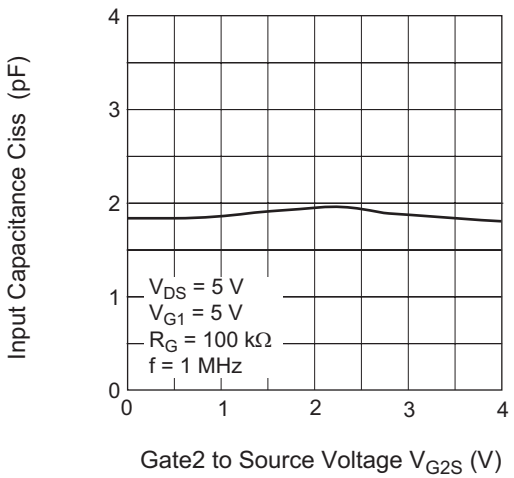
Forward Transfer Admittance vs. Gate1 Voltage (FET1)



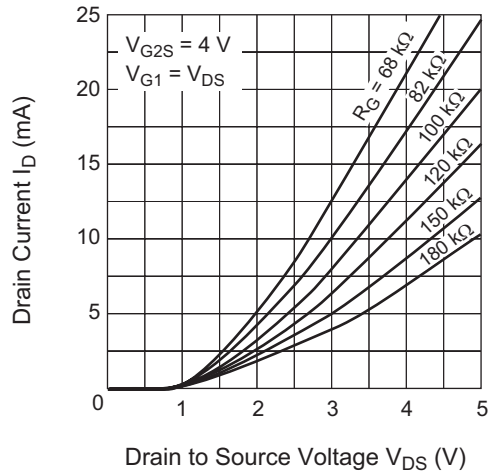
Drain Current vs. Gate Resistance (FET1)



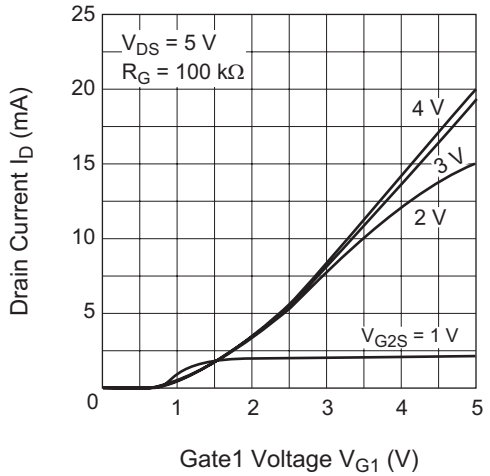
Input Capacitance vs. Gate2 to Source Voltage (FET1)



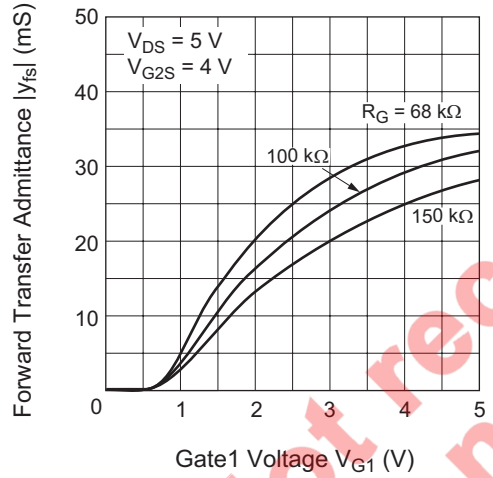
Typical Output Characteristics (FET2)



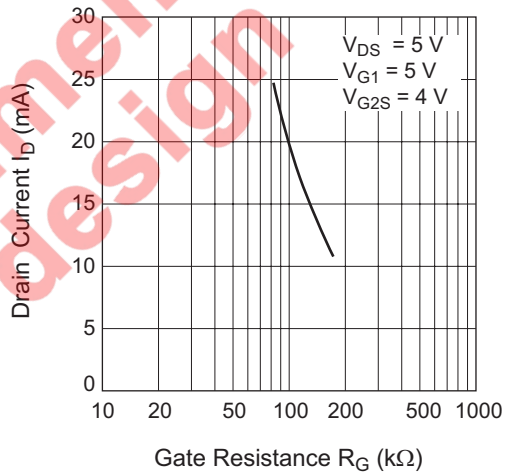
Drain Current vs. Gate1 Voltage (FET2)



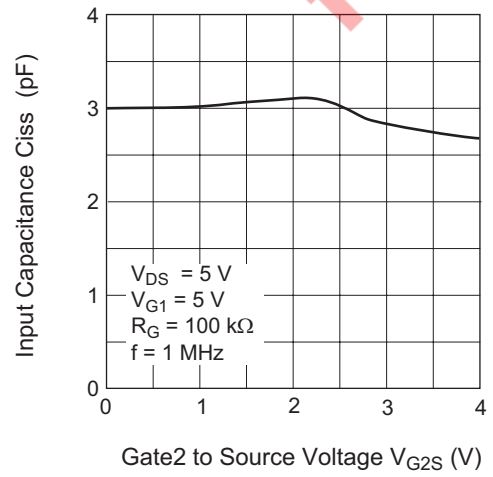
Forward Transfer Admittance vs. Gate1 Voltage (FET2)



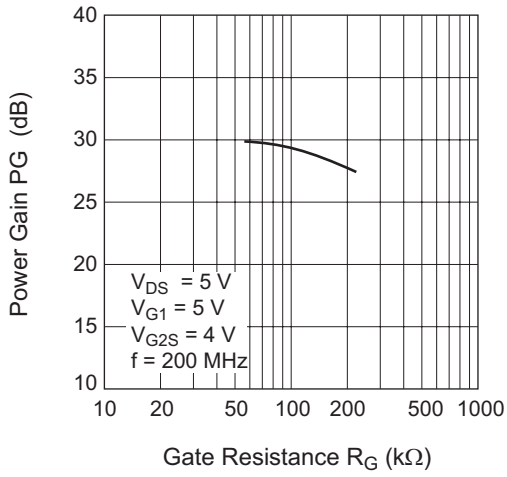
Drain Current vs. Gate Resistance (FET2)



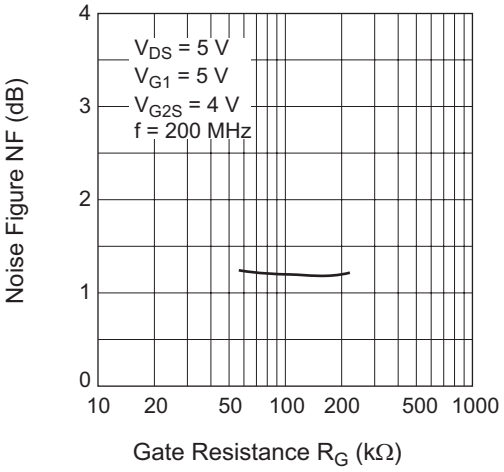
Input Capacitance vs. Gate2 to Source Voltage (FET2)



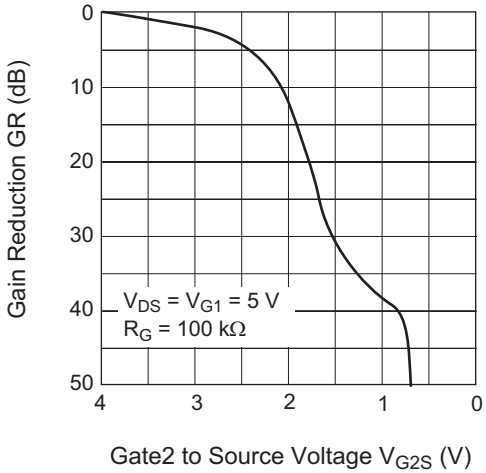
Power Gain vs. Gate Resistance (FET2)



Noise Figure vs.
Gate Resistance (FET2)

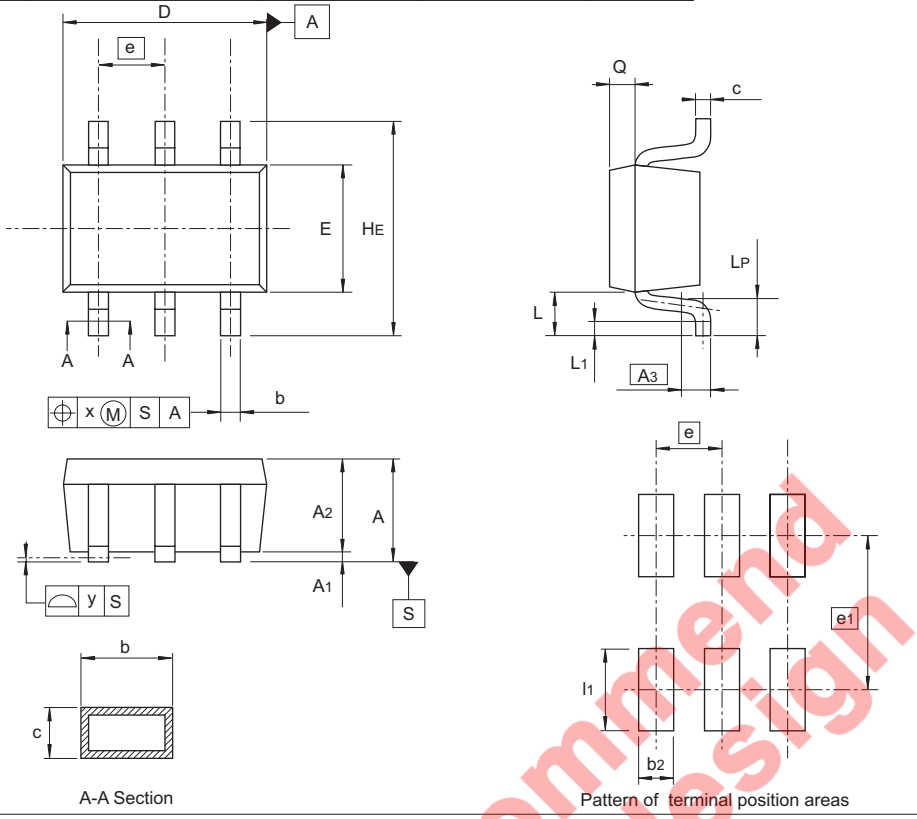


Gain Reduction vs.
Gate2 to Source Voltage (FET2)



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
CMPAK-6	SC-88	PTSP0006JA-A	CMPAK-6 / CMPAK-6V	0.006g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.8	–	1.1
A_1	0	–	0.1
A_2	0.8	0.9	1.0
A_3	–	0.25	–
b	0.15	0.2	0.25
c	0.1	0.15	0.25
D	1.8	2.0	2.2
E	1.15	1.25	1.35
e	–	0.65	–
H_E	2.0	2.1	2.2
L	0.3	–	0.7
L_1	0.1	–	0.5
L_P	0.2	–	0.6
x	–	–	0.05
y	–	–	0.05
b_2	–	–	0.35
e_1	–	1.5	–
l_1	–	–	0.9
Q	–	0.25	–

Ordering Information

Orderable Part Number	Quantity	Shipping Container
TBB1004DMTL-E TBB1004DMTL-H	3000	ϕ 178 mm Reel, 8 mm Emboss Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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