

Features

- automatic cable equalization
- fully compatible with SMPTE 259M
- typically equalizes greater than 350m of high quality cable at 270Mb/s
- signal strength indicator
- output data muting when input data is lost
- output 'eye' monitor (OEM) with large signal amplitude and power down option
- low power: 240mW at 5V
- 14 pin SOIC package
- programmable output data squelch for max cable length limiting
- carrier detect with programmable threshold level
- serial data output "High Z" select to allow muxing of EQ inputs
- Pb-free and Green

Applications

Front-end cable equalization for digital video systems; Input equalization for serial digital distribution amplifiers, routers, production switchers and other receiving equipment.

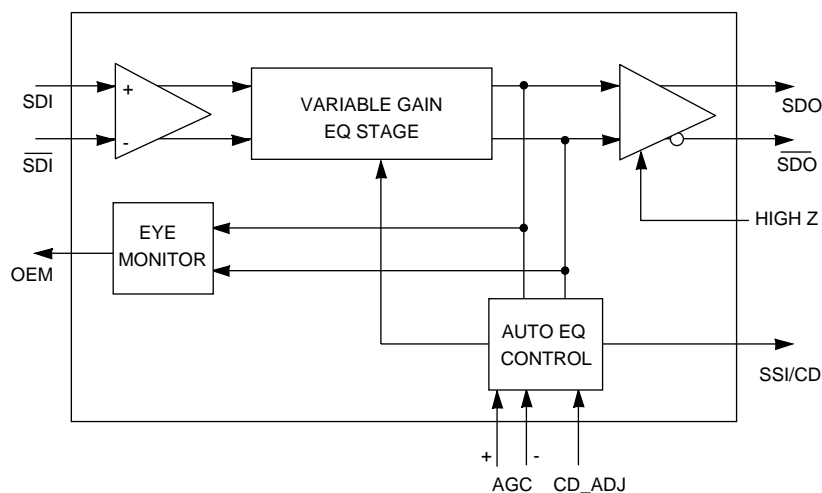
Description

The GS9024 is a high performance automatic cable equalizer designed for serial digital data rates from 143Mb/s to 540Mb/s. The GS9024 receives either single-ended or differential serial data and outputs equalized differential signals at PECL levels (800mV). The GS9024 provides up to 40dB of gain at 200MHz which will typically result in equalization of greater than 350m at 270Mb/s of Belden 8281 cable.

The GS9024 incorporates an analog signal strength indicator/carrier detect (SSI/CD) output indicating both the presence of a carrier and the amount of equalization applied to the signal. Optional external resistors allow the carrier detect threshold level to be customized to the user's requirement.

The GS9024 also features selectable High Z serial data outputs eliminating the need for input muxing circuitry in routers. In addition, the GS9024 provides an 'Output Eye Monitor' (OEM) which allows the verification of signal integrity after equalization, prior to reslicing.

The GS9024 operates from a single +5V or -5V power supply and consumes only 240mW of power. Packaged in a small 14 pin SOIC, the GS9024 is ideal for router applications where high density component placement is required.



Block diagram

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1. Electrical Characteristics

Table 1-1: Absolute Maximum Ratings

| Parameter | Value |
|--------------------------------------|---|
| Supply Voltage | 5.5V |
| Input Voltage Range (any input) | $V_{CC} + 0.5$ to $V_{EE} - 0.5V$ |
| Operating Temperature Range | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ |
| Storage Temperature Range | $-65^{\circ}C \leq T_S \leq 150^{\circ}C$ |
| Lead Temperature (soldering, 10 sec) | 260°C |

1.1 DC Electrical Characteristics

Table 1-2: DC Electrical Characteristics

$V_{CC} = 5V$, $V_{EE} = 0V$, $T_A = 0^{\circ}C$ TO $70^{\circ}C$ unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ ¹ | Max | Units | Notes | Test Level |
|---|--------------|------------------------------------|------|------------------|------|---------|-------|------------|
| Supply Voltage | V_{CC} | – | 4.75 | 5.0 | 5.25 | V | | |
| Power Consumption | P_D | – | – | 240 | – | mW | | 3 |
| | | with OEM active | – | 340 | – | mW | | 3 |
| Supply Current | I_S | – | – | 44 | – | mA | | 1 |
| | | with OEM active | – | 58 | – | mA | | 1 |
| Serial Data O/P Current | I_{SDO} | $R_L = 75\Omega$ | – | 11 | – | mA | | 3 |
| SDI/ \overline{SDI} Common Mode Voltage | – | – | – | 2.5 | – | V | | 1 |
| AGC+/AGC- Mode Voltage | – | – | – | 2.7 | – | V | | 1 |
| OEM Bias Potential | – | – | – | 4.5 | – | V | | 1 |
| SSI/CD Output Current | I_{SOURCE} | $C_{LMAX} = 50pF$ $R_L = \infty$ | – | – | 18 | μA | | |
| | | $C_{LMAX} = 50pF$ $R_L = 5k\Omega$ | – | – | 110 | μA | | |
| | I_{SINK} | – | – | 1.0 | 1.5 | mA | | |
| High Z Input Voltage | V_{HIGH} | – | 2.4 | – | – | V | | 1 |
| | V_{LOW} | – | – | – | 0.8 | V | | 1 |

TEST LEVELS

- 100% tested at 25°C.
- Guaranteed by design.
- Inferred or co-related value.

NOTES

- Typical values are parametric norms at 25°C.

1.2 AC Electrical Characteristics

Table 1-3: AC Electrical Characteristics

$V_{CC} = 5V$, $V_{EE} = 0V$, $T_A = 0^{\circ}C$ TO $70^{\circ}C$ unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ ¹ | Max | Units | Notes | Test Level |
|-------------------------------------|--------------|---|-----|------------------|------|------------|-----------|------------|
| Data Rate | | | 143 | – | 540 | Mb/s | | 1 |
| Output Signal Swing | V_{SDO} | $R_L = 75\Omega$ | 700 | 850 | 1000 | mV | | 1 |
| Additive Jitter | t_j | 270Mb/s, 300m | – | 275 | – | ps p-p | see Fig 5 | 5 |
| | | 540Mb/s, 100m | – | 200 | – | ps p-p | see Fig 5 | 5 |
| Output Rise and Fall Times (20-80%) | t_r, t_f | – | 0.5 | 0.65 | – | ns | | 3 |
| Output Duty Cycle Distortion | – | – | – | 30 | – | ps | | 2 |
| Input Resistance | R_{IN} | SDI, \overline{SDI} | – | 10 | – | k Ω | | 2 |
| Input Capacitance | C_{IN} | SDI, \overline{SDI} | – | 1.0 | – | pF | | 2 |
| Carrier Detect Response Time | t_{CDON} | Carrier Applied $R_L = \infty$, $C_L \leq 50pF$ on SSI/CD | – | 3 | – | μs | | 2 |
| | t_{CDOFF} | Carrier Removed $R_L = \infty$, $C_L \leq 50pF$ on SSI/CD | – | 30 | – | μs | | 2 |
| High Z Response Time | t_{rHIGHZ} | – | – | 17 | – | ns | | 2 |
| Input Return Loss | | at 270MHz | 15 | 20 | – | dB | see Fig 8 | 3 |
| Maximum Equalizer Gain | A_{EQ} | at 200MHz | – | 40 | – | dB | see Fig 4 | 3, 5 |

TEST LEVELS

- 100% tested at 25°C.
- Guaranteed by design.
- Inferred or co-related value.
- Evaluated using test setup [Figure 2-1](#).
- Evaluated using test setup [Figure 2-2](#).

NOTES

- Typical values are parametric norms at 25°C.

2. Test Setup

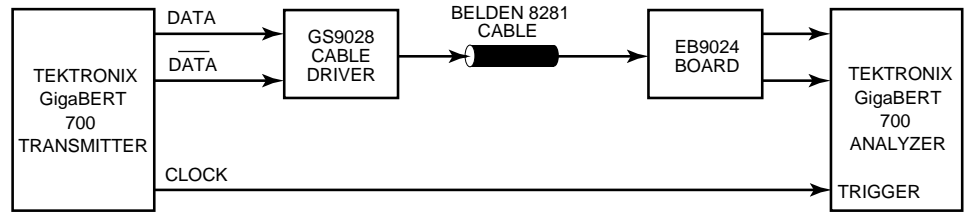


Figure 2-1: Test Setup for Figure 4-1.

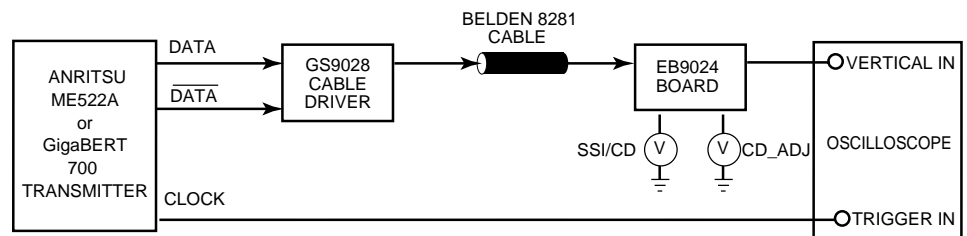


Figure 2-2: Test Setup for Figure 4-2, Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-8, and Figure .

3. Pin Connections

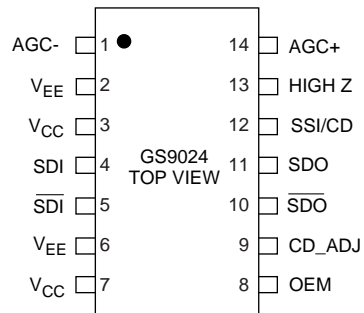


Table 3-1: Pin Descriptions

| Number | Symbol | Type | Description |
|--------|------------------------------|------|--|
| 1, 14 | AGC-, AGC+ | I | External AGC capacitor. |
| 4, 5 | SDI/ $\overline{\text{SDI}}$ | I | Differential serial digital data inputs. |
| 8 | OEM | O | Output 'Eye' monitor. OEM is a single ended current mode output and requires an external 50 Ω pullup resistor. |
| 9 | CD_ADJ | I | Carrier detect threshold adjust. |
| 10, 11 | $\overline{\text{SDO}}$ /SDO | O | Equalized serial digital data outputs. |
| 12 | SSI/CD | O | Signal strength indicator/Carrier Detect. |
| 13 | HIGH Z | I | The $\overline{\text{SDO}}$ /SDO outputs are High Z when this pin is HIGH. If High Z functionality is not used, this input can be left floating or tied LOW. |

4. Typical Performance Curves

($V_S = 5V$, $T_A = 25^\circ C$ unless otherwise shown.)

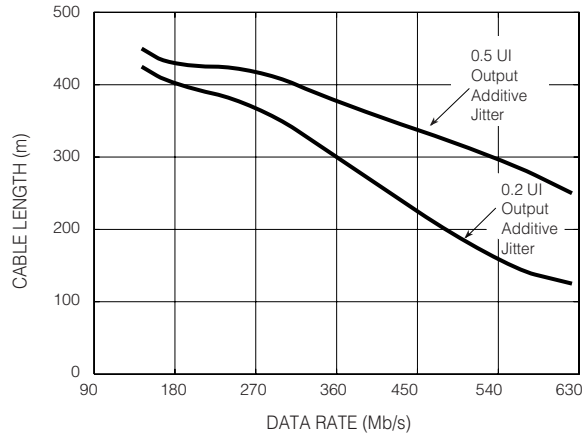


Figure 4-1: Maximum Data Rate vs. Cable Length - Belden 8281n (see Test Setup in Figure 2-1)

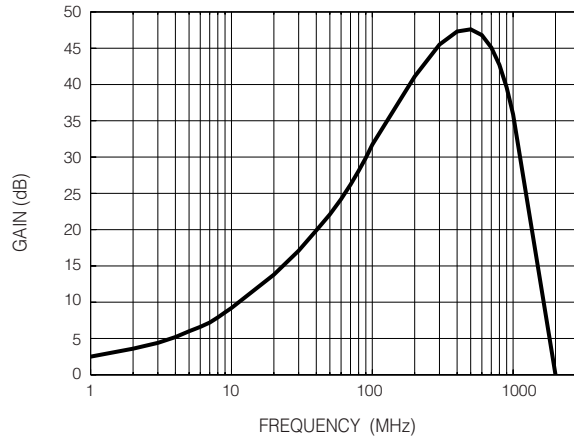


Figure 4-2: Equalizer Gain vs. Frequency

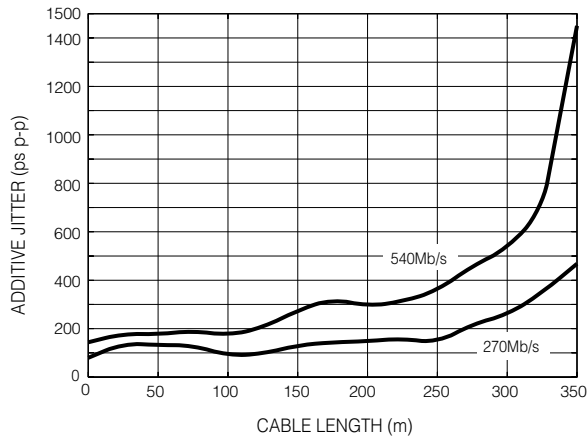


Figure 4-3: Additive Jitter vs. Input Cable Length — Belden 8281

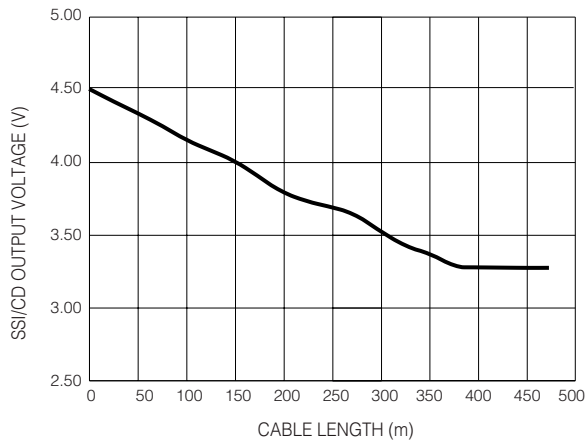


Figure 4-4: SSI/CD Voltage vs. Cable Length — Belden 8281 (CD_ADJ = 0V)

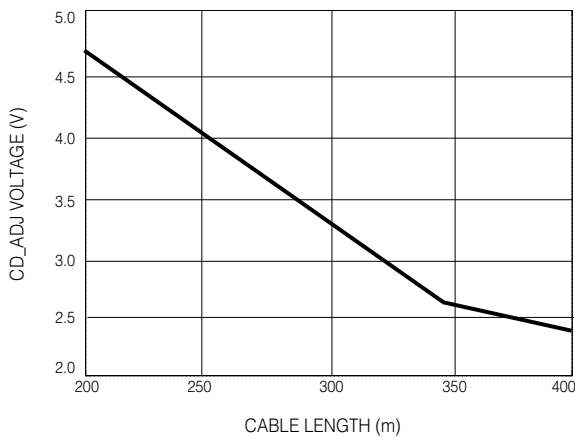
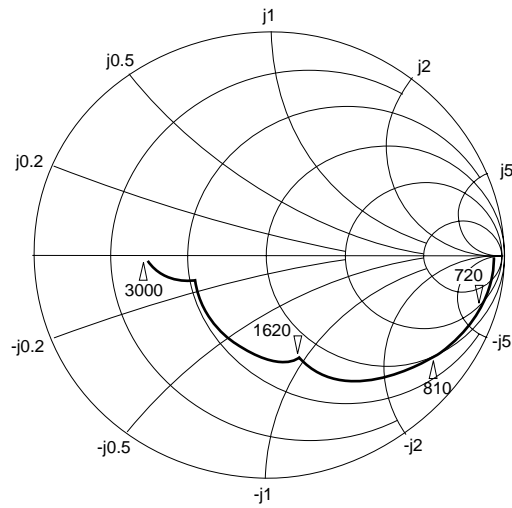


Figure 4-5: Carrier Detect Adjust Voltage Threshold Characteristics



Frequencies in MHz, impedances normalized to 50Ω.

Figure 4-6: Input Impedance

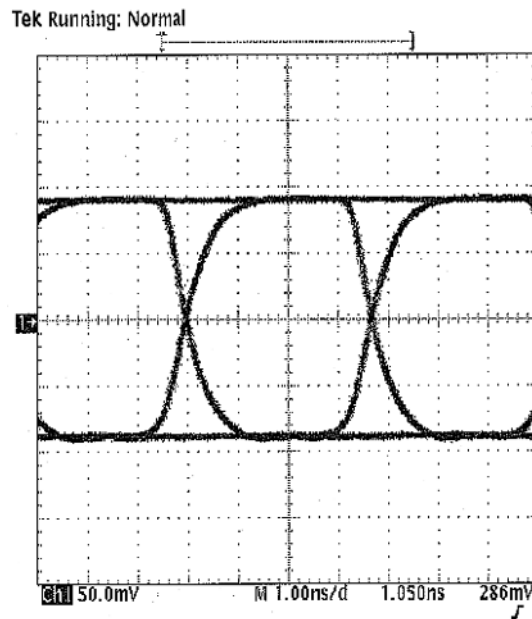


Figure 4-7: Output Data Waveform at 270Mb/s, 300m

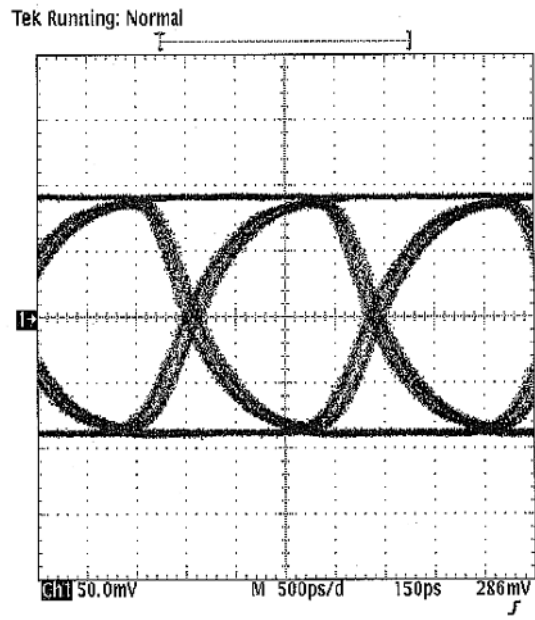


Figure 4-8: Output Data Waveform at 540Mb/s, 200m

5. Detailed Description

The GS9024 Automatic Cable Equalizer is a bipolar integrated circuit designed to equalize serial digital data signals between 30Mbps and 622Mbps. Powered from a single +5V or -5V supply, the device consumes approximately 240mW of power.

The serial data signal is connected to the input pins ($\overline{\text{SDI}}/\text{SDI}$) either differentially or single ended. The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length. The gain stage provides up to 40dB of gain at 200MHz which will typically result in equalization of greater than 350m at 270Mb/s of Belden 8281 cable.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by an external differential AGC filter capacitor (AGC+/AGC-) providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter.

The equalized signal is DC restored, thereby restoring its logic threshold to its corrective level regardless of shifts due to AC coupling. The digital output signals have PECL voltage levels (800mV) and are available at pins $\overline{\text{SDO}}$ and SDO.

5.1 Output HIGH Z

A HIGH Z pin allows the data outputs to be put into a high impedance state which disconnects them from the output traces. This feature is ideal for input expansion in router applications as it eliminates the need for input muxes or crosspoints.

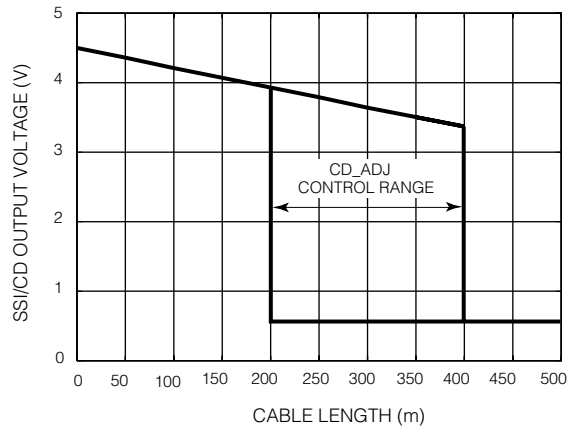
NOTE: The high impedance feature will only take effect if the device outputs are not muted.

5.2 Signal Strength Indication/Carrier Detect

The GS9024 incorporates an analog signal strength indicator/carrier detect output (SSI/CD) which indicates both the presence of a carrier and the amount of equalization applied to the signal. The voltage output of this pin versus cable length (signal strength) is shown in [Figure .](#) With 0m of cable (800mV input signal levels), the SSI/CD output voltage is approximately 4.5V.

As the cable length increases, the SSI/CD voltage decreases linearly providing accurate correlation between the SSI/CD voltage and cable length.

When the signal strength decreases to the level set at the "Carrier Detect Threshold Adjust" pin, the SSI/CD voltage goes to a logic "0" state (0.8V) and can be used to drive other TTL/CMOS compatible logic inputs. In addition, when loss of carrier is detected the $\overline{\text{SDO}}$ /SDO outputs are muted (set to a known static state).



5.3 Carrier Detect Threshold Adjust

The threshold level at which loss of carrier is detected is adjustable via external resistors at the CD_ADJ pin. The control voltage at the CD_ADJ pin is set by a simple resistor divider circuit. The threshold level is adjustable from 200m to 350m. By default (no external resistors), the threshold is typically 320m. Connecting this pin to Ground disables the $\overline{\text{SDO}}$ /SDO muting function and allows for maximum possible cable length equalization.

This feature is designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. This problem is not solved by using a Carrier Detect function with a fixed internal reference because the signal to noise ratio on the circuit board may be significantly less than the default signal detection level set by the on-chip reference. To solve this problem, the GS9024 provides a user adjustable threshold to meet the unique conditions that exist in each user's application. Override and internal default settings are provided to give the user total flexibility.

5.4 Output Eye Monitor

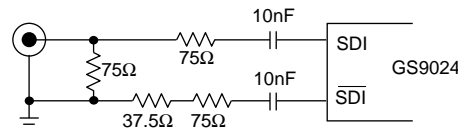
The GS9024 provides an 'Output Eye Monitor' (OEM) which allows the verification of signal integrity after equalization, prior to reslicing. The OEM pin is an open collector current output that requires an external 50 Ω pullup resistor. When the pullup resistor is not used, the OEM block is disabled and the internal OEM circuit is powered down. The OEM provides a 0.25Vp-p signal when driving a 50 Ω oscilloscope input.

5.5 I/O Description

5.5.1 High Speed Analog Inputs (SDI/ $\overline{\text{SDI}}$)

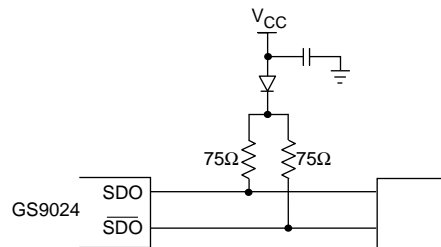
SDI/ $\overline{\text{SDI}}$ are high impedance inputs which accept differential or single-ended input drive.

Figure shows the recommended interface when a single-ended serial digital signal is used.



5.5.2 High Speed Outputs ($\overline{\text{SDO}}$ /SDO)

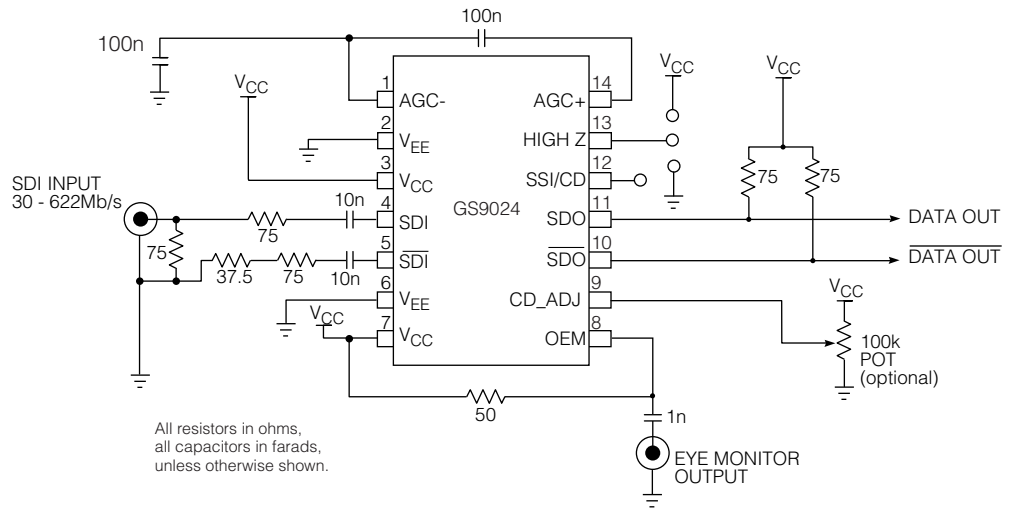
$\overline{\text{SDO}}$ /SDO are current mode outputs that require external pullups (see Figure). The output signal swings are 800mV when 75Ω resistors are used. A diode can be placed between V_{CC} and the pullups to shift the signal levels down by approximately 0.7 volts. When the output traces are longer than 1 inch, controlled impedance traces should be used. The pullup resistors should be placed at the end of the output traces as they terminate the trace in its characteristic impedance (75Ω).



6. Applications Information

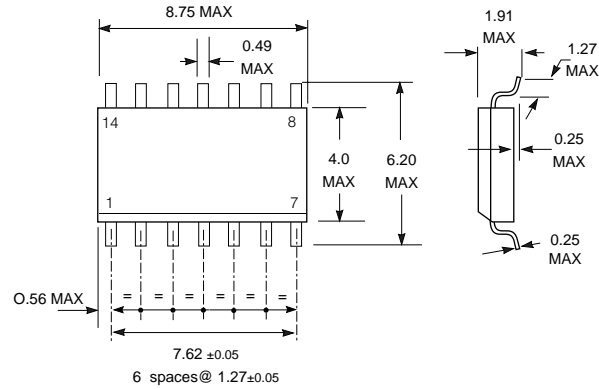
The Typical Application Circuit shown on [page 14](#) is useful for both SMPTE and DVB-ASI signals. The two AGC capacitors shown however increase the AGC time constant from the original times shown in earlier SMPTE-only application circuits. In this case a minimum off-time of 50ms is needed when break-before-make switching is used at the input in order for the AGC voltage to recover.

7. Typical Application Circuit



8. Package Dimensions

All dimensions in millimeters.



9. Ordering Information

| Part Number | Package | Temperature | Pb-Free and Green |
|--------------|------------------|-------------|-------------------|
| GS9024-CKB | 14 pin SOIC | 0°C to 70°C | No |
| GS9024-CTB | 14 pin SOIC Tape | 0°C to 70°C | No |
| GS9024-CKBE3 | 14 pin SOIC | 0°C to 70°C | Yes |
| GS9024-CTBE3 | 14 pin SOIC Tape | 0°C to 70°C | Yes |

10. Revision History

| Version | ECR | Date | Changes |
|---------|--------|---------------|--|
| 10 | 135403 | February 2005 | Added note to clarify that the High Impedance feature is available only when the device outputs are not muted. |

CAUTION

ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

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