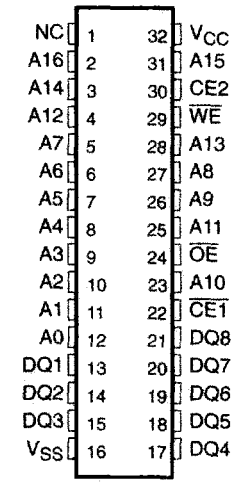
- **Processed to MIL-PRF-38535**
- **Organization . . . 128K Words × 8 Bits**
- **Fast Static Operation**
- **Single 5-V Supply (±10% Tolerance)**
- **Maximum Access Time From Address or Chip Enable:**
  - **'5C1008-20 20 ns**
  - **'5C1008-25 25 ns**
- **TTL Compatible Inputs and Outputs**
- **Low-Power Standby**
- **3-State Outputs**
- **Ceramic Package Options**
  - **32-Pin Ceramic Dual In-Line Package (CDIP) (400 mil), JDC Suffix**
  - **32-Pin Leadless Ceramic Chip Carrier (LCCC), HM Suffix**
- **Military Operating Temperature Range −55°C to 125°C**

JDC or HM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A16	Address Inputs
$\overline{CE1}$, CE2	Chip Enables
DQ1 – DQ8	Data In/Data Out
NC	No Connect
$\overline{OE}$	Output Enable
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{WE}$	Write Enable

description

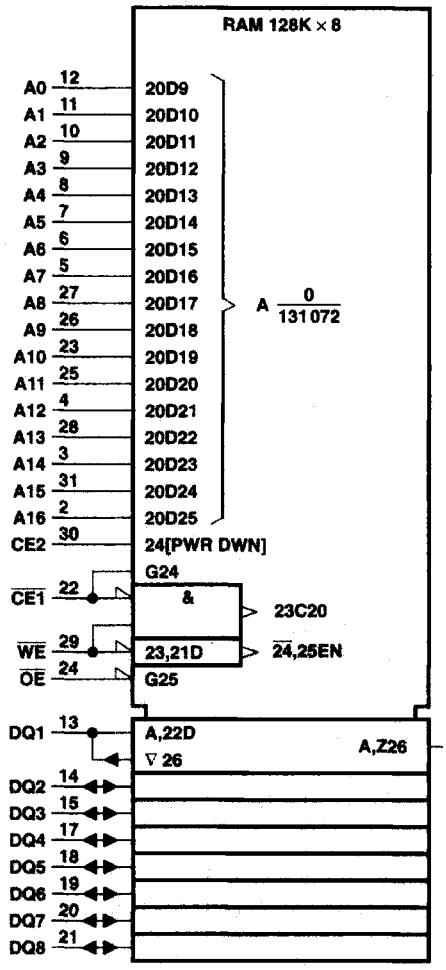
The SMJ5C1008 is a high-performance 1048576-bit CMOS static random-access memory (SRAM) organized as 128K words × 8 bits. The device features maximum address or chip-enable access times of 20 ns or 25 ns.

The SMJ5C1008 offers dual chip enables ($\overline{CE1}$, CE2) and an output enable ($\overline{OE}$) for greater system flexibility. The chip enables place the device in an active or standby-power mode, while $\overline{OE}$ allows the outputs to be placed in the high-impedance state, eliminating bus contention problems. In the standby-power mode, the device is disabled, resulting in reduced power consumption. This allows designers to meet extremely low standby-power requirements.

To write to the device, the $\overline{WE}$ and $\overline{CE1}$ inputs are held at logic low while CE2 is at logic high. To read from the device, $\overline{WE}$ and CE2 are held at logic high and $\overline{CE1}$ and $\overline{OE}$ are held at logic low.

All devices operate from a single 5-V (±10%) supply. They are MIL-PRF-38535, Device Class Q qualified and are operational from −55°C to 125°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JDC package.

truth table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I/O PIN	CYCLE	CURRENT
H	X	X	X	Not selected	Hi-Z	—	I_{CC1}
X	L	X	X	Not selected	Hi-Z	—	I_{CC1}
L	H	H	H	Output disabled	Hi-Z	—	I_{CC}
L	H	L	H	Read	D_{OUT}	Read	I_{CC}
L	H	X	L	Write	D_{IN}	Write	I_{CC}

H = High, L = Low, X = don't care

operation

address (A0–A16)

Seventeen address lines allow access to each of the 128K 8-bit words in RAM.

data inputs/data outputs (DQ1–DQ8)

Data can be written into the device when $\overline{CE1}$ and $\overline{WE}$ are low and CE2 is high. DQ1 – DQ8 are TTL compatible. The device is placed in a low-power standby mode with the DQs in the high-impedance state when $\overline{CE1}$ is at logic high or CE2 is at logic low. The device remains active with high-impedance DQs when $\overline{OE}$, CE2, and $\overline{WE}$ are high, and when $\overline{CE1}$ is low.

chip enable ($\overline{CE1}$, CE2)

Two separate chip enables, $\overline{CE1}$ and CE2, are provided for greater design flexibility. Whenever $\overline{CE1}$ is low and CE2 is high, the device is active. Standby mode is reached when either $\overline{CE1}$ is high or CE2 is low. Data is retained during standby.

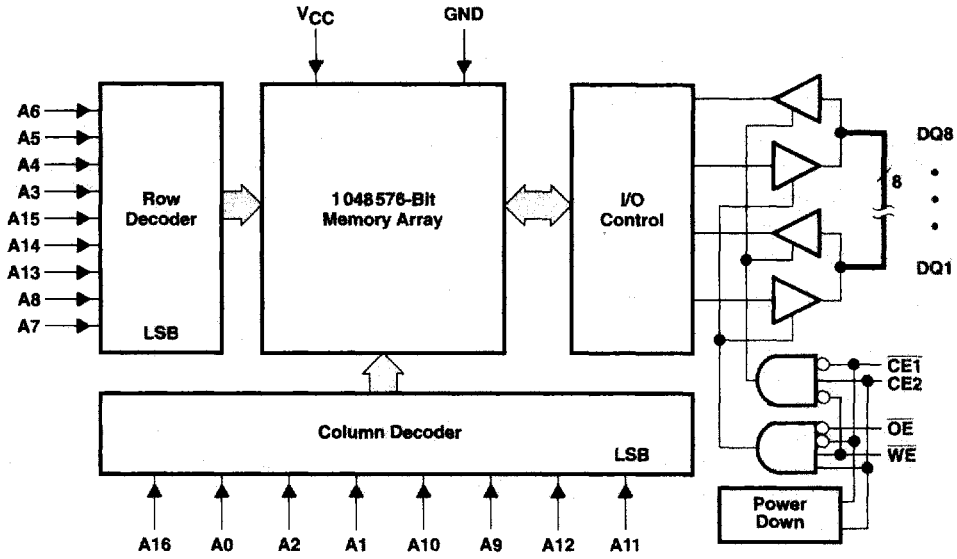
write enable ($\overline{WE}$)

The read or write mode is selected through the use of $\overline{WE}$. $\overline{WE}$ must be high for the read mode and low for the write mode. $\overline{WE}$ must be high when address changes occur to prevent erroneously writing data into new memory locations. $\overline{WE}$ is a don't care function when the device is in standby mode.

output enable ($\overline{OE}$)

When in the read mode, $\overline{OE}$ controls the state of the DQs. A high on $\overline{OE}$ places the DQs in the high-impedance state, while a low provides data on the outputs.

functional block diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.5 V to 7 V
Input voltage range (see Note 2) ..... –0.5 to V_{CC} + 0.5 V
Output voltage range in high-impedance state ..... – 0.5 V to V_{CC} + 0.5 V
Short-circuit output current (per output) ..... 20 mA
Maximum operating free-air temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to V_{SS}.
2. Negative undershoots on V_{IL} and V_{OL} can be tolerated if they are ≥–3.0 V with a maximum pulse duration of 20 ns. Prolonged operation at levels below –1 V results in excessive currents that can damage the device input.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		V_{CC} + 0.5	V
V_{IL}	Low-level input voltage	– 0.5		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'5C1008-20 MIN	'5C1008-20 MAX	'5C1008-25 MIN	'5C1008-25 MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = – 4 mA	2.4		2.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA		0.4		0.4	V
I_I	Input current (load)		V_{CC} = 5.5 V, 0 V ≤ V_I ≤ V_{CC}	– 5	5	– 5	5	µA
I_O	Output current (leakage)		V_{CC} = 5.5 V, 0 V ≤ V_O ≤ V_{CC}, Output disabled	– 5	5	– 5	5	µA
I_{CC}	V_{CC} supply current, operating		V_{CC} = 5.5 V, I_O = 0 mA, $\overline{CE1}$ = V_{IL} MAX, CE2 = $\overline{OE}$ = $\overline{WE}$ = V_{IH}, f = MAX		150		140	mA
I_{CC1}	V_{CC} supply current, standby	TTL-level inputs	V_{CC} = 5.5 V, $\overline{CE1}$ ≥ V_{IH} MIN, V_{IN} ≤ V_{IL} MAX or ≥ V_{IH} MIN, f = MAX = 1/$t_{c(R)}$		40		35	mA
			V_{CC} = 5.5 V, $\overline{CE1}$ ≥ V_{IH} MIN, V_{IN} ≤ V_{IL} MAX or ≥ V_{IH} MIN, f = 0 MHz		38		38	
		CMOS-level inputs	V_{CC} = 5.5 V, $\overline{CE1}$ ≥ V_{CC} – 0.2 V and [V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ V_{SS} + 0.2 V] f = 0 MHz		10		10	mA

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

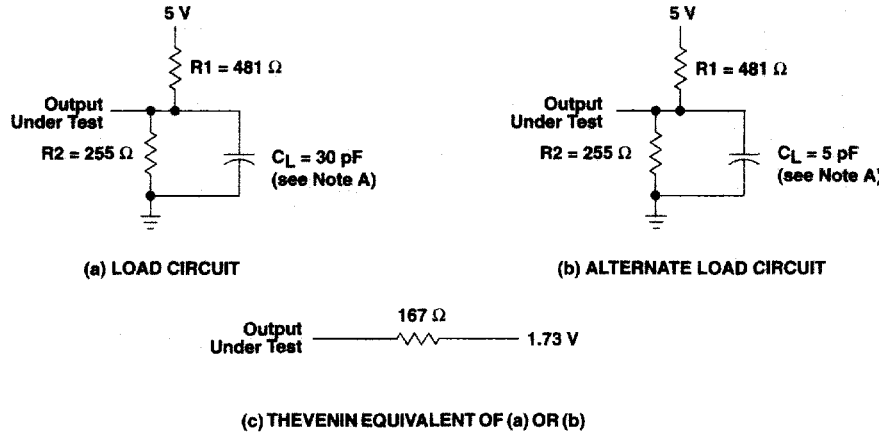
capacitance over recommended ranges of supply voltage, f = 1 MHz, T_A = 25°C‡

PARAMETER			MIN	MAX	UNIT
C_i	Input capacitance	$\overline{OE}$, A2, A3, A10		12	pF
		All other inputs		10	
C_o	Output capacitance	DQ1–DQ8		14	pF

‡ Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

PARAMETER	VALUE
Input pulse levels	0 V to 3 V
Input rise and fall times	2 ns
Input and output reference levels	1.5 V



(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

(c) THEVENIN EQUIVALENT OF (a) OR (b)

NOTE A: C_L includes probe and fixture capacitances.

Figure 1. Output Load Circuits

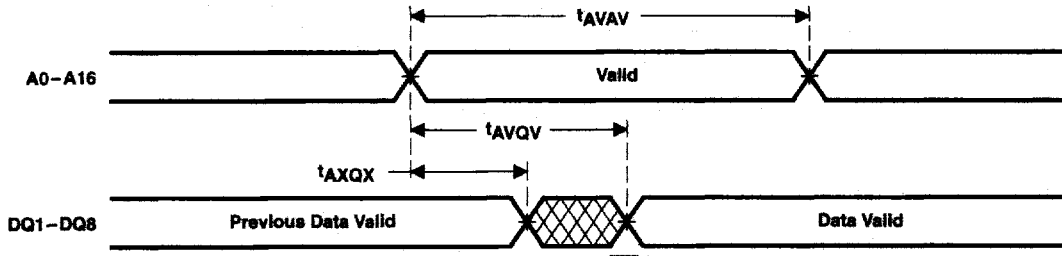
read-cycle timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		ALT. SYMBOL	'5C1008-20		'5C1008-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(R)}$	Cycle time, read	t_{AVAV}	20		25		ns

read-cycle switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		ALT. SYMBOL	'5C1008-20		'5C1008-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A16	t_{AVQV}		20		25	ns
$t_{a(E1)}$	Access time from $\overline{CE1}$ low	t_{ELQV}		20		25	ns
$t_{a(E2)}$	Access time from CE2 high	t_{ELQV}		20		25	ns
$t_{a(G)}$	Access time from $\overline{OE}$ low	t_{OLQV}		7		10	ns
$t_{v(A)}$	Valid time of output data after address change	t_{AXQX}	3		3		ns
$t_{en(E)}$†‡	Output enable time from $\overline{CE1}$ low or CE2 high	t_{ELQX}	3		3		ns
$t_{en(G)}$†‡	Output enable time from $\overline{OE}$ low	t_{OLQX}	0		0		ns
$t_{dis(E)}$†‡	Output disable time from $\overline{CE1}$ high and CE2 low	t_{EHQZ}	0	8		10	ns
$t_{dis(G)}$†‡	Output disable time from $\overline{OE}$ high	t_{OHQZ}	0	8		10	ns

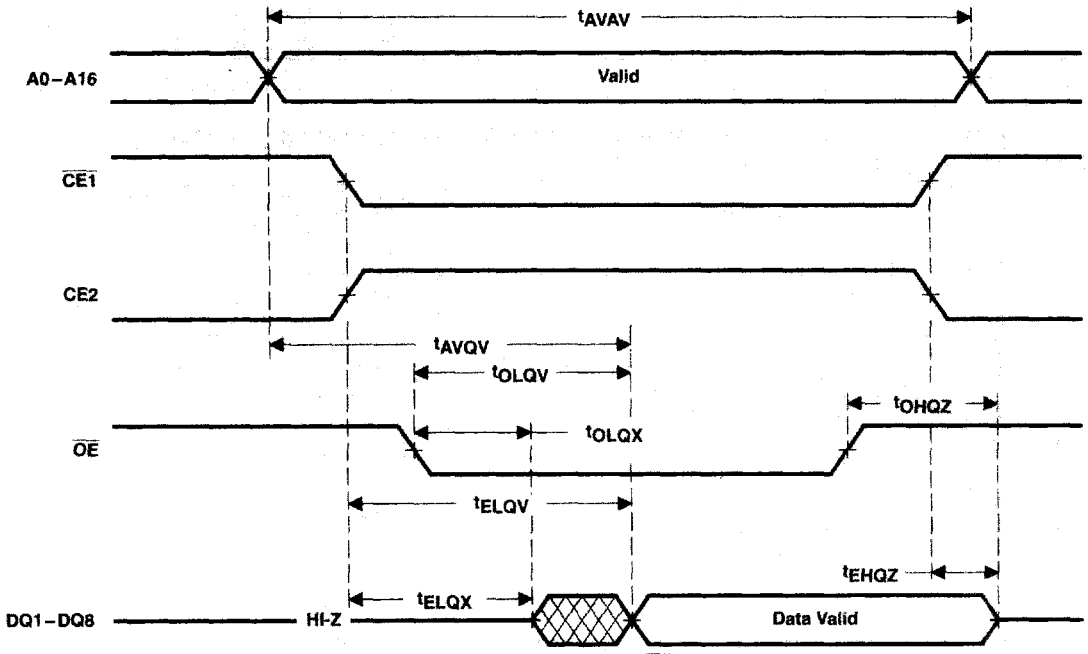
† This parameter is specified by design but not tested.
‡ Transition is measured ± 500 mV from steady-state voltage with the load shown in Figure 1(b).



NOTE A: All chip enables and output enables are held in their active state. $\overline{WE}$ is high.

Figure 2. Read-Cycle Timing, Device Continously Selected

PARAMETER MEASUREMENT INFORMATION



NOTE A: Addresses valid prior to or coincident with latest occurring chip enable. $\overline{WE}$ is high.

Figure 3. Read-Cycle Timing, Enable Controlled

write-cycle ($\overline{WE}$ controlled) timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		ALT. SYMBOL	'5C1008-20		'5C1008-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	20		25		ns
$t_{w(W)}$	Pulse duration, write	t_{WLWH} t_{WLEH}	15		20		ns
$t_{su(A)}$†	Setup time, address	t_{AVWL}	0		0		ns
$t_{su(D)}$‡	Setup time, data to end of write	t_{DVWH}	10		15		ns
$t_{su(AWH)}$‡	Setup time, address to end of write	t_{AVWH}	15		20		ns
$t_{h(A)}$‡	Hold time, address from end of write	t_{WHAX}	0		0		ns
$t_{h(D)}$‡	Hold time, data from end of write	t_{WHDX}	0		0		ns

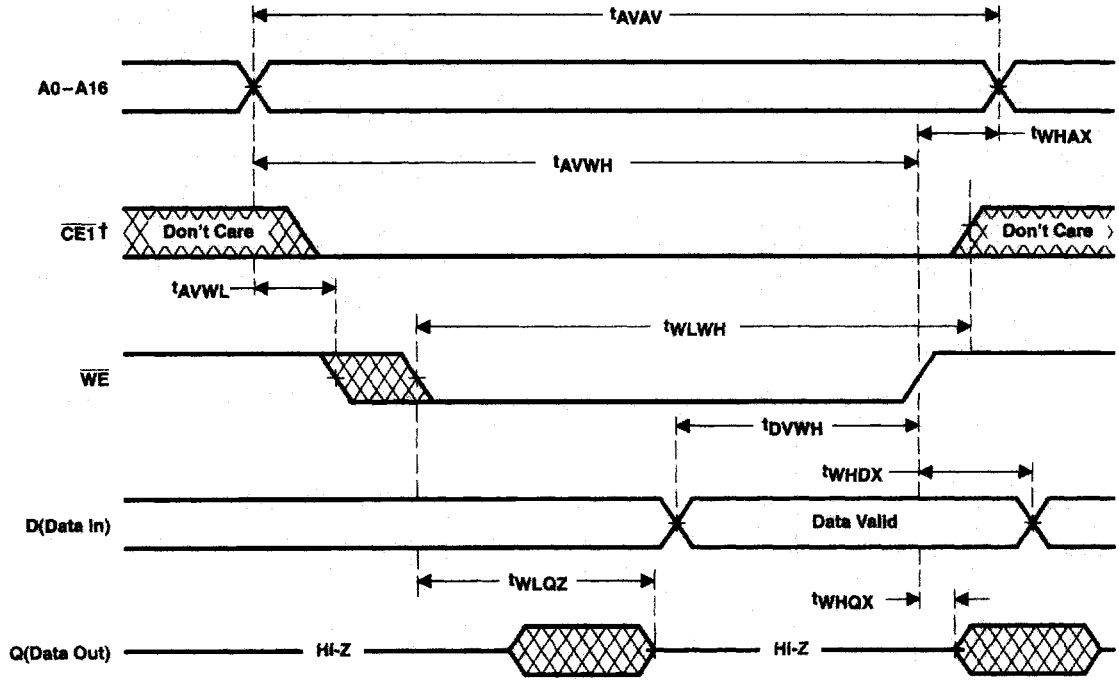
† Referenced to latest end of $\overline{WE}$, $\overline{CE1}$, or CE2
‡ Referenced to earliest end of $\overline{WE}$, $\overline{CE1}$, or CE2

write-cycle ($\overline{WE}$ controlled) switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 3 and 4)

PARAMETER		ALT. SYMBOL	'5C1008-20		'5C1008-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{en(W)}$§¶	Enable time, output from $\overline{WE}$ high	t_{WHQX}	5		5		ns
$t_{dis(W)}$§¶	Disable time, output from $\overline{WE}$ low	t_{WLQZ}	0	9	0	10	ns

§ Transition is measured ± 500 mV from steady-state voltage with the load shown in Figure 1(b).
¶ This parameter is specified by design but not tested.
NOTES: 3. If $\overline{OE}$ goes low coincident with or after $\overline{W}$ goes low, the output remains in the high-impedance state.
4. If $\overline{CE1}$ goes low coincident with or after $\overline{W}$ goes high, the output remains in the high-impedance state.

PARAMETER MEASUREMENT INFORMATION



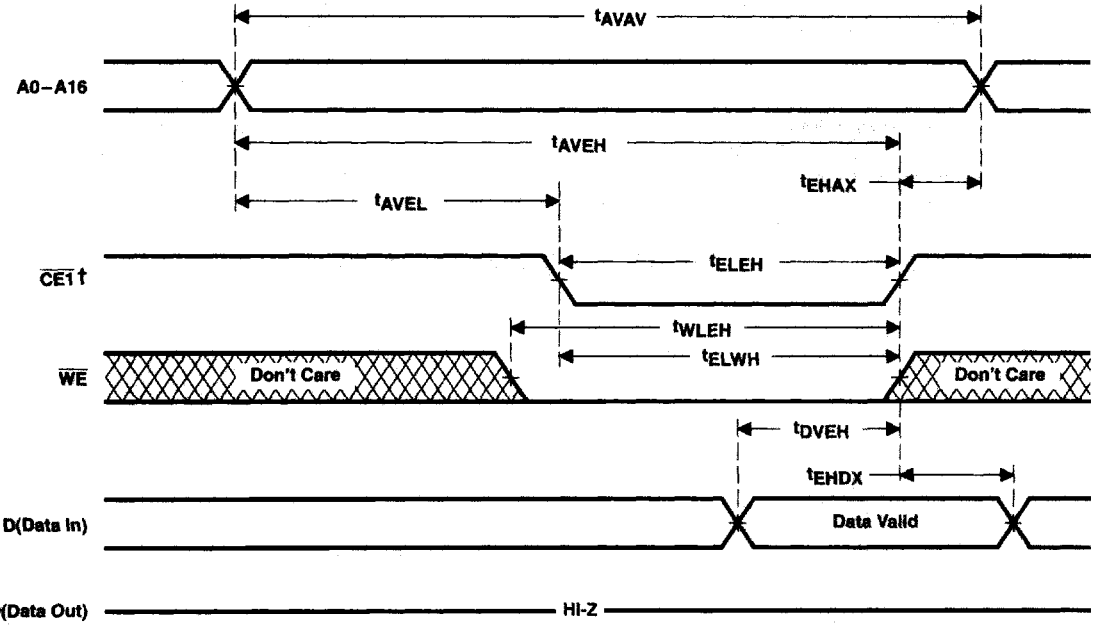
† $\overline{OE}$ is inactive (high). CE2 timing is the same as $\overline{CE1}$ timing except the CE2 waveform is inverted with respect to $\overline{CE1}$.

Figure 4. Write-Cycle Timing, Write-Enable Controlled

write-cycle ($\overline{CE}$ controlled)timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Notes 3 and 4)

		ALT. SYMBOL	'5C1008-20		'5C1008-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	20		25		ns
$t_{w(W)}$	Pulse duration, write	t_{WLEH}	15		20		ns
$t_{su(EW)}$	Setup time. chip-enable to end of write	t_{ELEH} t_{ELWH}	15		20		ns
$t_{su(A)}$†	Setup time. address	t_{AVEL}	0		0		ns
$t_{su(D)}$‡	Setup time. data to end of write	t_{DVEH}	10		15		ns
$t_{su(AWH)}$‡	Setup time. address to end of write	t_{AVEH}	15		20		ns
$t_{h(A)}$‡	Hold time, address from end of write	t_{EHAX}	0		0		ns
$t_{h(D)}$‡	Hold time, data from end of write	t_{EHDX}	0		0		ns

† Referenced to latest end of $\overline{WE}$, $\overline{CE1}$, or C
‡ Referenced to earliest end of $\overline{WE}$, $\overline{CE1}$, or CE2
NOTES: 3. If $\overline{OE}$ goes low coincident with or after $\overline{W}$ goes low, the output remains in the high-impedance state.
4. If $\overline{CE1}$ goes low coincident with or after $\overline{W}$ goes high, the output remains in the high-impedance state.



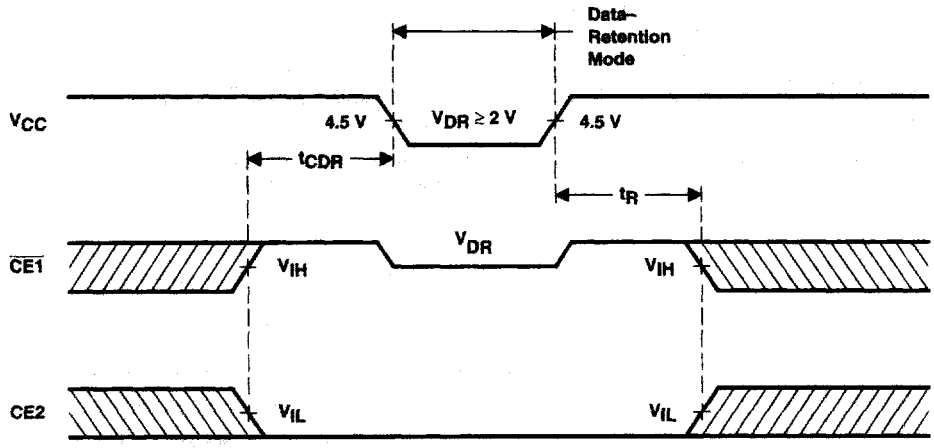
† $\overline{OE}$ is inactive (high). CE2 timing is the same as $\overline{CE1}$ timing except the CE2 waveform is inverted with respect to $\overline{CE1}$.

Figure 5. Write-Cycle Timing, Chip-Enable Controlled

data-retention characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	'5C1008-20		'5C1008-25		UNIT
			MIN	MAX	MIN	MAX	
V_{DR}	Data–retention voltage supply	V_{CC} = 2 V	2		2		V
$I_{CC\ DR}$	Data–retention current	$\overline{CE1} \geq V_{CC} - 0.2$ V or		2		2	mA
t_{CDR}	Retention time†	$CE2 \leq V_{SS} + 0.2$ V	0		0		ns
t_R	Operation recovery time†	$V_{IN} \geq V_{CC} - 0.2$ V or ≤ 0.2 V	20		25		ns

† This parameter is tested initially and after any design or process change.



NOTES: A. Either $\overline{CE1}$ or CE2 can be used to begin data–retention mode.
B. For t_R and t_{CDR}: $\overline{CE1} \geq V_{CC} - 0.2$ V or $CE2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or ≤ 0.2 V.

Figure 6. Data–Retention Waveform