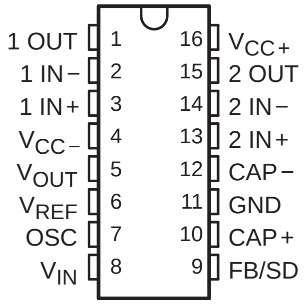
TLE2682
HIGH-SPEED JFET-INPUT DUAL OPERATIONAL AMPLIFIER WITH SWITCHED-CAPACITOR VOLTAGE CONVERTER

SLOS127 − JUNE 1993

- **Single-Supply Operation With Rail-to-Rail Inputs**
- **± 30-mA Min Short-Circuit Output Current**
- **Wide V_{CC} Range . . . 3.5 V to 15 V**
- **V_{OUT} Supplies up to 100 mA for External Loads**
- **Shutdown Mode**
- **External 2.5-V Voltage Reference Available**
- **40-V/μs Slew Rate Typ**
- **High Gain-Bandwidth Product . . . 10 MHz**

DW PACKAGE
(TOP VIEW)



description

The TLE2682 offers the advantages of JFET-input operational amplifiers and rail-to-rail common-mode input voltage range with the convenience of single-supply operation. By combining a switched-capacitor voltage converter with a dual operational amplifier in a single package, Texas Instruments now gives circuit designers new options for conditioning low-level signals in single-supply systems.

The TLE2682 features two high-speed, high-output drive JFET-input operational amplifiers with a switched-capacitor building block. Using two external capacitors, the switched-capacitor network can be configured as a voltage inverter generating a negative supply voltage capable of sourcing up to 100 mA. This supply functions not only as the amplifier’s negative rail but is also available to drive external circuitry. In this configuration, the amplifier common-mode input voltage range extends from the positive rail to below ground, thus providing true rail-to-rail inputs from a single supply. Furthermore, the outputs can swing to and below ground while sinking over 25 mA. This feature was previously unavailable in operational amplifier circuits. The TLE2682 operational amplifier section has output stages that can drive 20-mA loads to 2.3 V with a 5-V rail. With a 2-mA load, the output swing extends to 3.9 V.

This amplifier design features a 25-V/μs minimum slew rate, which results in a high-power bandwidth. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8-MHz minimum. The TLE2682 offers significant speed and noise advantages at a low 1.5-mA typical supply current per channel.

The TLE2682 features a shutdown pin (FB/SD), which can be used to disable the switched-capacitor section. When disabled, the switched-capacitor voltage converter block draws less then 150 μA from the power supply, V_{IN}.

The switched-capacitor voltage converter block also provides an on-board regulator; with the addition of an external divider, a well-regulated output voltage is easily obtained. The internal oscillator runs at a nominal frequency of 25 kHz. This can be synchronized to an external clock signal or can be varied using an external capacitor. A 2.5-V reference is brought out to V_{REF} for use with the on-board regulator or external circuitry. Additional filtering can be added to minimize switching noise.

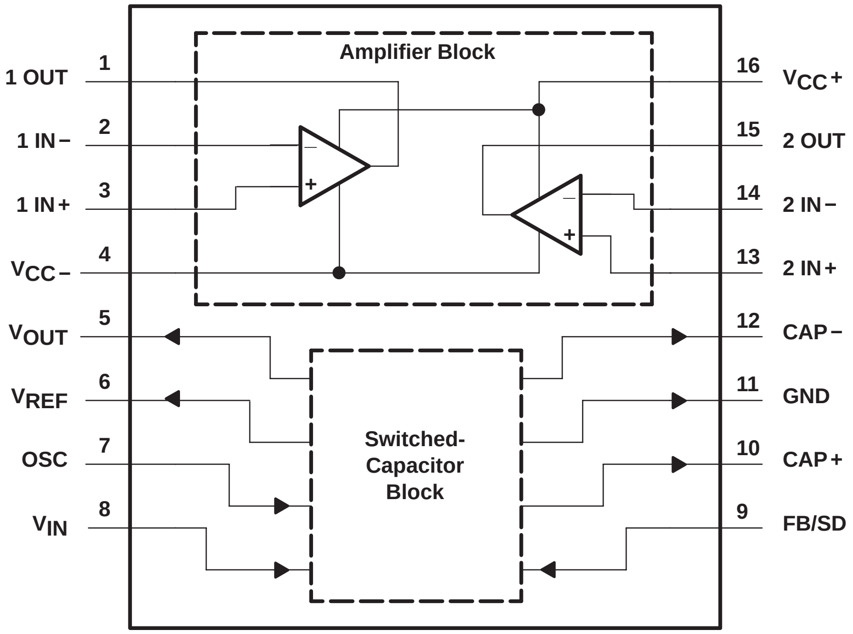
The TLE2682 is characterized for operation over the industrial temperature range of −40°C to 85°C. This device is available in a 16-pin wide-body surface-mount package.

AVAILABLE OPTION

T_A	PACKAGE
	SMALL OUTLINE (DW)
−40°C to 85°C	TLE2682IDW

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., TLE2682IDWR).

functional block diagram



ACTUAL DEVICE COMPONENT COUNT

AMPLIFIER BLOCK		SWITCHED-CAPACITOR BLOCK	
Transistors	57	Transistors	71
Resistors	37	Resistors	44
Diodes	5	Diodes	2
Capacitors	11	Capacitors	5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{IN} (see Note 1)	16 V
Supply voltage, V_{CC+} (see Note 2)	16 V
Supply voltage, V_{CC-} (see Note 2)	−16 V
Differential input voltage, V_{ID} (see Note 3)	32 V
Input voltage, V_I (any input of amplifier) (see Note 2)	$V_{CC\pm}$
Input voltage range, V_I (FB/SD) (see Note 1)	0 V to V_{IN}
Input voltage range, V_I (OSC) (see Note 1)	0 V to V_{REF}
Input current, I_I (each input of amplifier)	± 1 mA
Output current, I_O (each output of amplifier)	± 80 mA
Total current into V_{CC+}	160 mA
Total current out of V_{CC-}	160 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 4) (each amplifier)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Junction temperature (see Note 5)	150°C
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the switched-capacitor block GND pin.
2. Voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at IN+ with respect to IN−.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
5. The devices are functional up to the absolute maximum junction temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC+}/V_{IN}		3.5	15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−1	5	V
	$V_{CC\pm} = \pm15$ V	−11	15	
Output current at V_{OUT}, I_O		0	100	mA
Operating free-air temperature, T_A		−40	85	°C

OPERATIONAL AMPLIFIER SECTION

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		0.9	7.5	mV
				Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, See Figure 4	V_O = 0,	25°C		5	100	pA
				Full range			950	
I_{IB}	Input bias current			25°C		15	175	pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		V
				Full range	5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		V
				Full range	3.7			
		I_O = −2 mA		25°C	3.5	3.9		
				Full range	3.4			
		I_O = −20 mA		25°C	1.5	2.3		
				Full range	1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		V
				Full range	−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		
				Full range	−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		
				Full range	−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	75	91		dB
				Full range	74			
			R_L = 2 kΩ	25°C	85	100		
				Full range	84			
			R_L = 10 kΩ	25°C	90	106		
				Full range	89			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11		pF
			Differential	25°C		2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	25°C	70	89		dB
				Full range	68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0	R_S = 50 Ω	25°C	82	99		dB
				Full range	80			
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	2.9	3.6	mA
				Full range			3.6	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35		mA
			V_{ID} = −1 V			45		

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_{O(PP)} = \pm2.3$ V, $A_{VD} = -1$, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	25°C		35		V/μs
				Full range	20			
SR−	Negative slew rate			25°C		38		V/μs
				Full range	20			
	Settling time	$A_{VD} = -1$, 2-V step, $R_L = 1$ kΩ, $C_L = 100$ pF	To 10 mV	25°C		0.25		μs
			To 1 mV			0.4		
V_n	Equivalent input noise voltage	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		28		nV/$\sqrt{\text{Hz}}$
			f = 10 kHz			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6		μV
			f = 0.1 Hz to 10 Hz			0.6		
I_n	Equivalent input noise current	$V_{IC} = 0$,	f = 10 kHz	25°C		2.8		fA/$\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 5$ V, f = 1 k Hz, $R_S = 25\Omega$	$A_{VD} = 10$, $R_L = 2$ kΩ,	25°C		0.013%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $C_L = 25$ pF,	$R_L = 2$ kΩ, See Figure 2	25°C		9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4$ V, $R_L = 2$ kΩ,	$A_{VD} = -1$, $C_L = 25$ pF	25°C		2.8		MHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $C_L = 25$ pF,	$R_L = 2$ kΩ, See Figure 2	25°C		56°		

† Full range is 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	$V_O = 0$,	25°C		1.1	7.5	mV
				Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25	µV/°C
I_{IO}	Input offset current	$V_{IC} = 0$, See Figure 4	$V_O = 0$,	25°C		6	100	pA
				Full range			950	
I_{IB}	Input bias current			25°C		20	175	pA
				Full range			2.5	nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C	15 to −11	15 to −11.9		V
				Full range	15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -200\ \mu A$		25°C	13.8	14.1		V
				Full range	13.7			
		$I_O = -2$ mA		25°C	13.5	13.9		
				Full range	13.4			
		$I_O = -20$ mA		25°C	11.5	12.3		
				Full range	11.5			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 200\ \mu A$		25°C	−13.8	−14.2		V
				Full range	−13.7			
		$I_O = 2$ mA		25°C	−13.5	−14		
				Full range	−13.4			
		$I_O = 20$ mA		25°C	−11.5	−12.4		
				Full range	−11.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V	$R_L = 600\ \Omega$	25°C	75	96		dB
				Full range	74			
			$R_L = 2\ k\Omega$	25°C	90	109		
				Full range	89			
			$R_L = 10\ k\Omega$	25°C	90	118		
				Full range	89			
r_i	Input resistance	$V_{IC} = 0$		25°C		10^{12}		Ω
c_i	Input capacitance	$V_{IC} = 0$, See Figure 5	Common mode	25°C		7.5		pF
			Differential	25°C		2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	$V_O = 0$,	25°C	80	98		dB
				Full range	79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$,	$R_S = 50\ \Omega$	25°C	82	99		dB
				Full range	80			
I_{CC}	Supply current (both channels)	$V_O = 0$,	No load	25°C	2.7	3.1	3.6	mA
				Full range			3.6	
a_x	Crosstalk attenuation	$V_{IC} = 0$,	$R_L = 2\ k\Omega$	25°C		120		dB
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	25°C	−30	−45		mA
			$V_{ID} = -1$ V		30	48		

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_{O(PP)} = \pm10$ V, $A_{VD} = -1$, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	25°C	25	40		V/µs
				Full range	20			
SR−	Negative slew rate			25°C	25	45		V/µs
				Full range	20			
	Settling time	$A_{VD} = -1$, 10-V step, $R_L = 1$ kΩ, $C_L = 100$ pF	To 10 mV	25°C		0.4		µs
			To 1 mV			1.5		
V_n	Equivalent input noise voltage	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		28		nV/√Hz
			f = 10 kHz			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6		µV
			f = 0.1 Hz to 10 Hz			0.6		
I_n	Equivalent input noise current	$V_{IC} = 0$,	f = 10 kHz	25°C		2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} =$ 20 V, f = 1 kHz, $R_S = 25$Ω	$A_{VD} = 10$, $R_L = 2$ kΩ,	25°C		0.008%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $C_L = 25$ pF,	$R_L = 2$ kΩ, See Figure 2	25°C	8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 20$ V, $R_L = 2$ kΩ,	$A_{VD} = -1$, $C_L = 25$ pF	25°C	478	637		kHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $C_L = 25$ pF,	$R_L = 2$ kΩ, See Figure 2	25°C		57°		

† Full range is −40°C to 85°C.

SWITCHED-CAPACITOR SECTION

electrical characteristics over recommended supply voltage range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
Regulated output voltage, V_{OUT}	V_{CC} = 5 V, T_J = 25°C, $R_L(V_{OUT})$ = 500 Ω, See Note 6		25°C	−3.75	−4	−4.25	V
	V_{CC} = 7 V, T_J = 25°C, $R_L(V_{OUT})$ = 500 Ω, See Note 7		25°C	−4.7	−5	−5.2	
Input regulation	V_{CC} = 5 V to 15 V, $R_L(V_{OUT})$ = 500 Ω, See Note 6		Full range		7	27	mV
	V_{CC} = 7 V to 12 V, $R_L(V_{OUT})$ = 500 Ω, See Note 7		Full range		5	25	
Output regulation	V_{CC} = 5 V, $R_L(V_{OUT})$ = 100 Ω to 500 Ω		Full range		20	140	mV
	V_{CC} = 7 V, $R_L(V_{OUT})$ = 100 Ω to 500 Ω		Full range		20	70	
Voltage loss, $V_{CC} - \lvert V_{OUT} \rvert$ (see Note 8)	V_{CC} = 7 V, $C_{IN} = C_{OUT}$ = 100-µF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
		I_O = 100 mA	Full range		1.1	1.8	
Output resistance	ΔI_O = 10 mA to 100 mA, See Note 9		Full range		10	15	Ω
Oscillator frequency			Full range	15	25	35	kHz
Reference voltage, V_{ref}	V_{CC} = 5 V, I_{ref} = 50 µA		25°C	2.35	2.5	2.65	V
			Full range	2.25		2.75	
	V_{CC} = 7 V, I_{ref} = 60 µA		25°C	2.35	2.5	2.65	
			Full range	2.25		2.75	
Maximum switch current			25°C		300		mA

† Data applies for the switched-capacitor block only. Amplifier block is not connected.
‡ Full range is −40°C to 85°C.

NOTES: 6. Regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator (see Figure 105) with R1 = 23.7 kΩ, R2 = 102.2 kΩ, C_{IN} = 10 µF (tantalum), C_{OUT} = 100 µF (tantalum), and C1 = 0.002 µF.
7. Regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator (see Figure 105) with R1 = 20 kΩ, R2 = 102.5 kΩ, C_{IN} = 10 µF (tantalum), C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF.
8. For voltage-loss tests, the switched-capacitor section is connected as a voltage inverter, with V_{REF}, OSC, and FB/SD (pins 6, 7, and 9) unconnected. The voltage losses may be higher in other configurations.
9. Output resistance is defined as the slope of the curve (ΔV_O vs ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve are higher at currents less than 10 mA due to the characteristics of the switch transistors.

AMPLIFIER AND SWITCHED-CAPACITOR SECTIONS CONNECTED

electrical characteristics, $V_{IN} = V_{CC+}$ = 5 V, T_A = 25°C (see Figure 6)

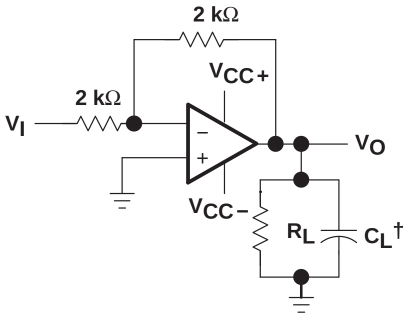
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ			4.1		V
		R_L = 600 Ω			3.6		
		R_L = 100 Ω			2.3		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ			−3.9		V
		R_L = 600 Ω			−3.3		
		R_L = 100 Ω			−1.9		
	Voltage loss, $V_{IN} - \lvert V_{OUT} \rvert$ (see Note 8)	V_{ID} = −100 mV, $C_{IN} = C_{OUT}$ = 100-µF tantalum	R_L = 10 kΩ		0.55		V
			R_L = 600 Ω		0.65		
			R_L = 100 Ω		0.9		

NOTE 8: For voltage-loss tests, the switched-capacitor section is connected as a voltage inverter, with V_{REF}, OSC, and FB/SD (pins 6, 7, and 9) unconnected. The voltage losses may be higher in other configurations.

supply current (no load), T_A = 25°C

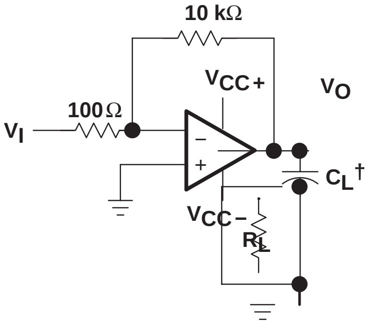
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	V_{CC+} = 5 V, V_{IN} = 5 V, $V_{FB/SD}$ = 2.5 V, V_O = 0		8.9		mA
Supply current in shutdown	V_{CC+} = 5 V, V_{IN} = 5 V, $V_{FB/SD}$ = 0 V		2.5		mA

PARAMETER MEASUREMENT INFORMATION



† Includes fixture capacitance

Figure 1. Slew-Rate Test Circuit



† Includes fixture capacitance

Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

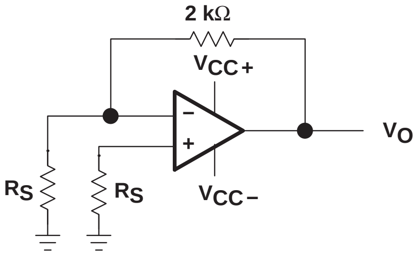


Figure 3. Noise-Voltage Test Circuit

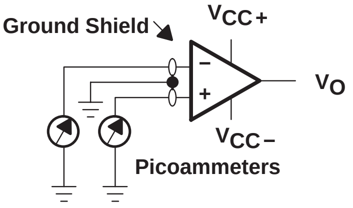


Figure 4. Input-Bias and Offset-Current Test Circuit

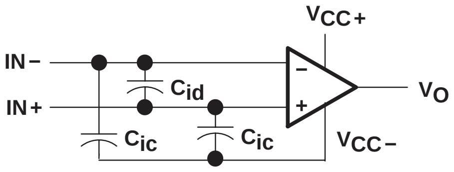


Figure 5. Internal Input Capacitance

PARAMETER MEASUREMENT INFORMATION

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2682, accurate measurement of the bias currents becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket, and a second test is performed that measures both the socket leakage and the device input bias current (see Figure 6). The two measurements are then subtracted algebraically to determine the bias current of the device.

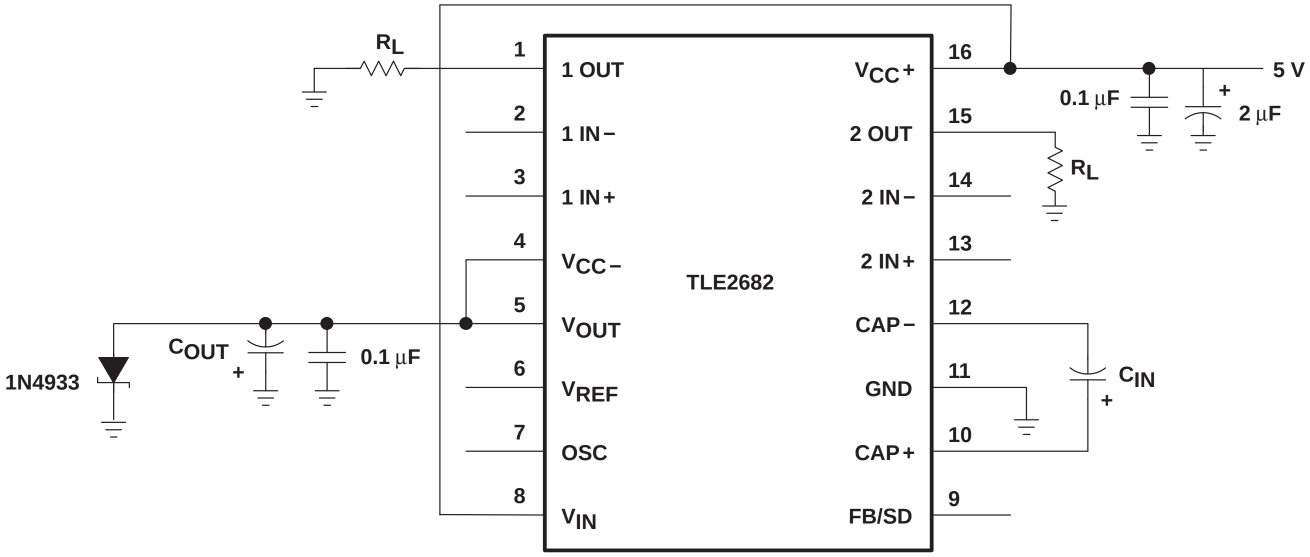


Figure 6. Bias-Current Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs for Operational Amplifier Section

			FIGURE
V_{IO}	Input offset voltage	Distribution	7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8
I_{IO}	Input offset current	vs Free-air temperature	9, 10
I_{IB}	Input bias current	vs Free-air temperature vs Supply voltage	9, 10 11
V_{IC}	Common-mode input voltage range	vs Free-air temperature	12
V_{ID}	Differential input voltage	vs Output voltage	13, 14
V_{OM+}	Maximum positive peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	15 17, 18 19
V_{OM-}	Maximum negative peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	16 17, 18 19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
V_O	Output voltage	vs Settling time	21
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Free-air temperature vs Frequency	22 23, 24 25, 26
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	27 28
k_{SVR}	Supply voltage rejection ratio	vs Frequency vs Free-air temperature	29 30
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	31 32 33, 34
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	35 36 37
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V_n	Input-referred noise voltage	vs Noise bandwidth Over a 10-second time interval	43 44
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TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

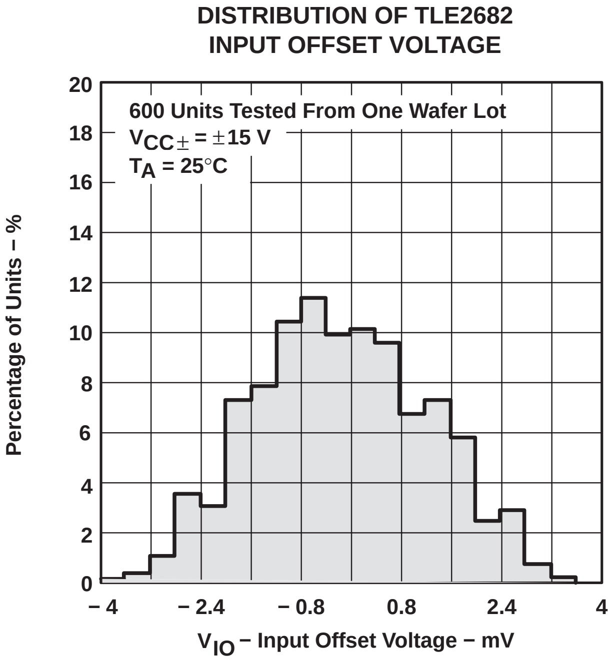

Figure 7

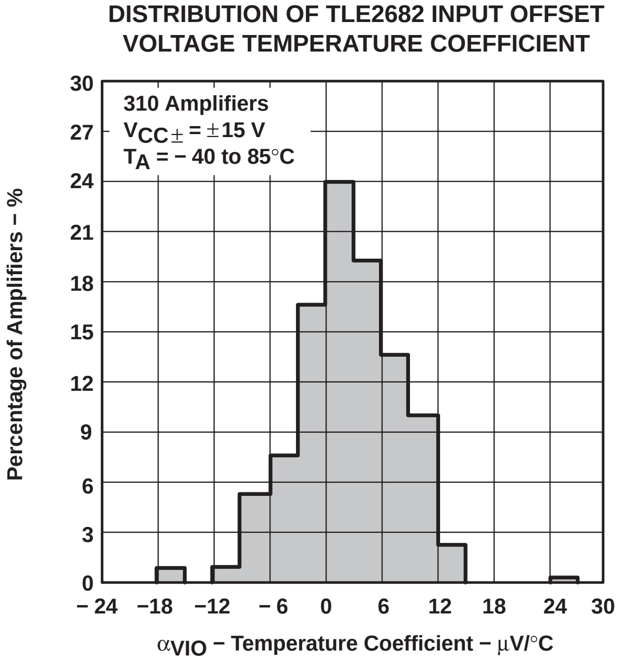

Figure 8

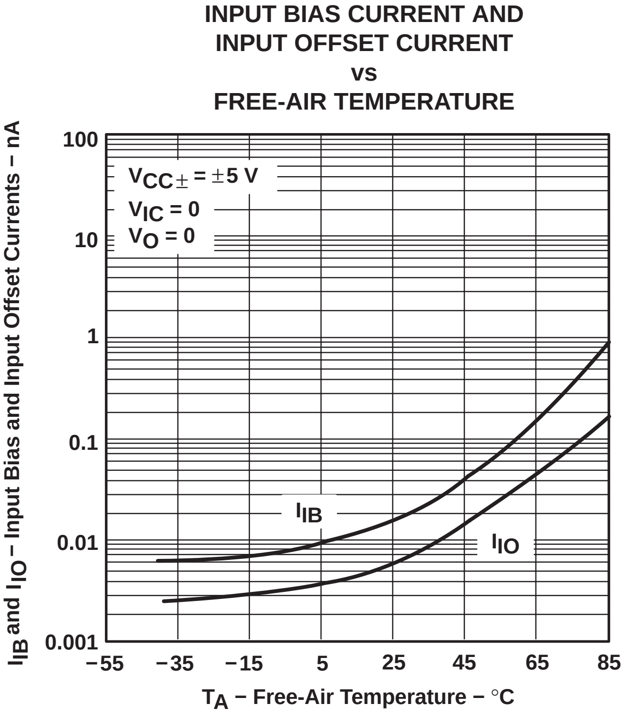

Figure 9

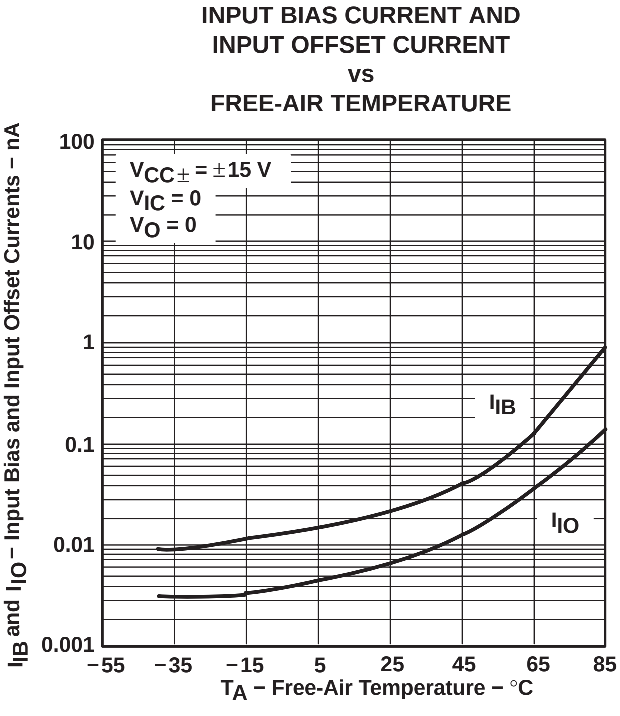

Figure 10

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

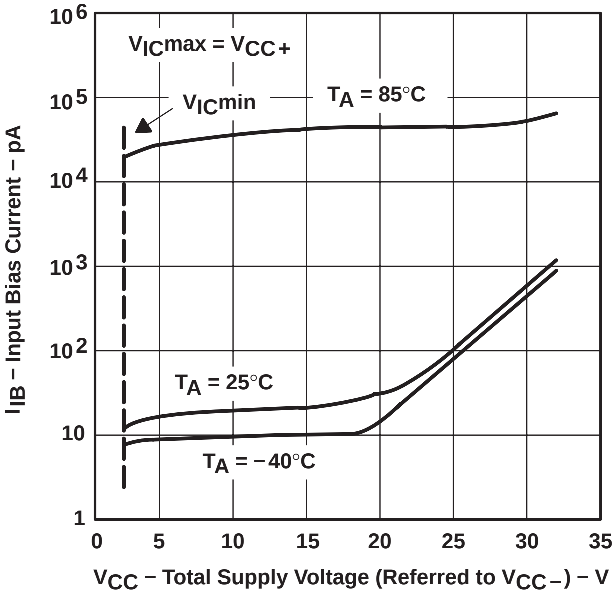

Figure 11

COMMON-MODE INPUT VOLTAGE RANGE
vs
TEMPERATURE

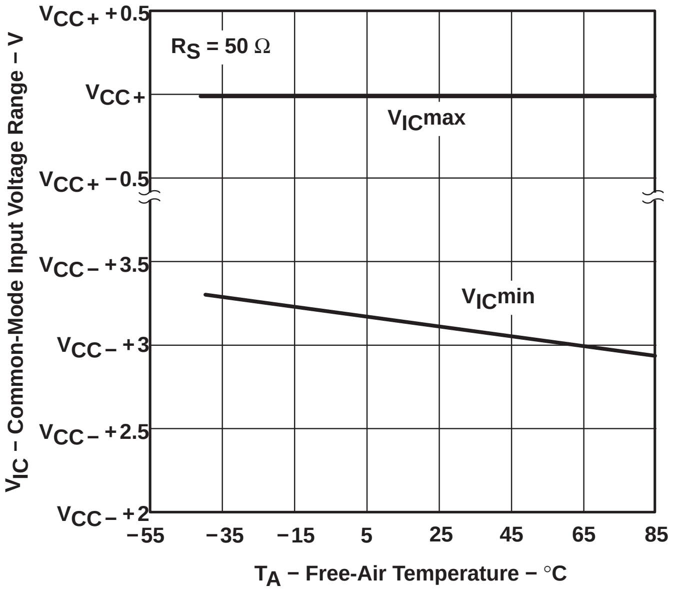

Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

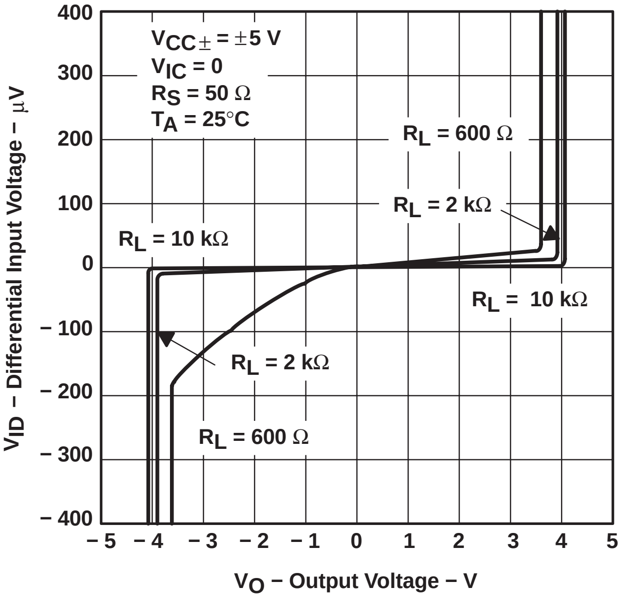

Figure 13

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

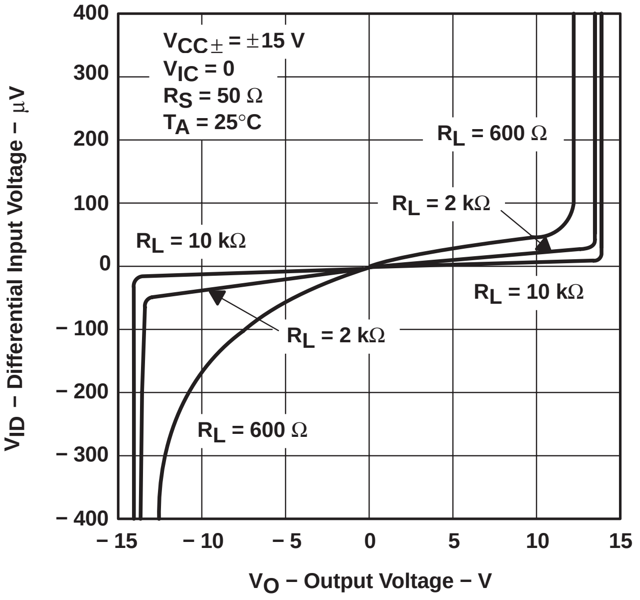

Figure 14

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

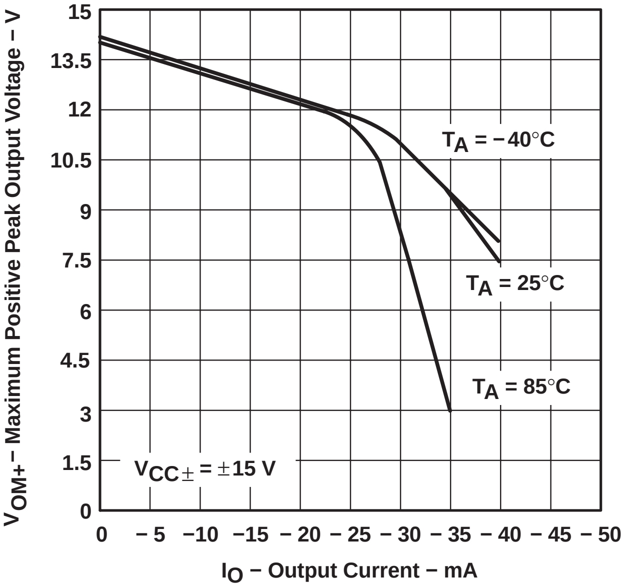

Figure 15

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

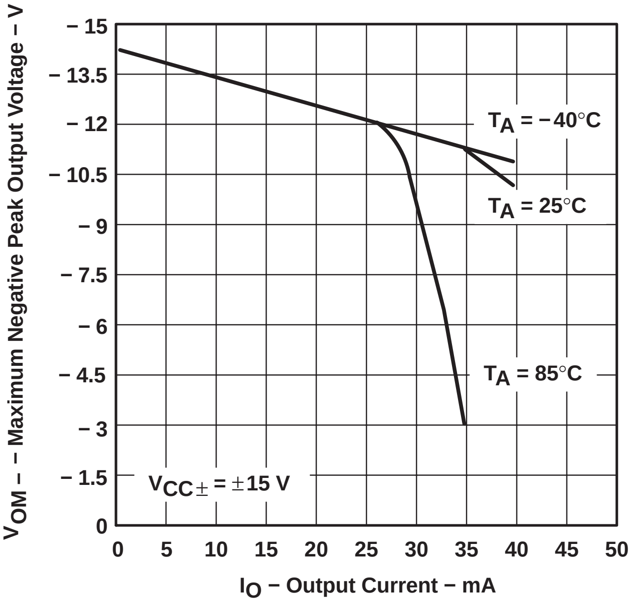

Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

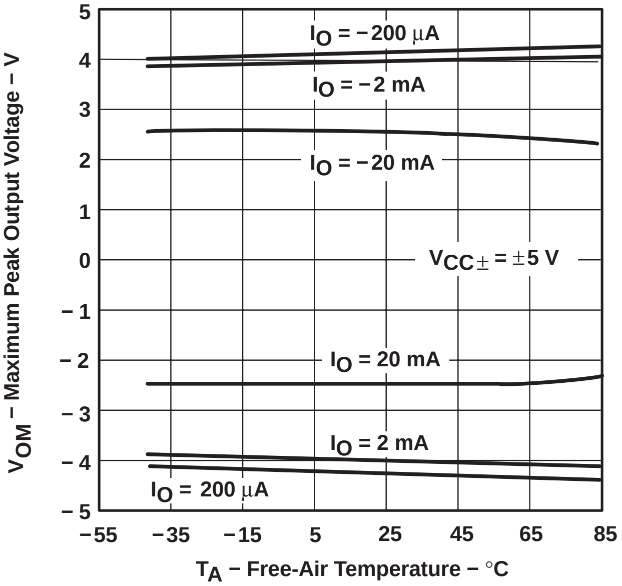

Figure 17

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

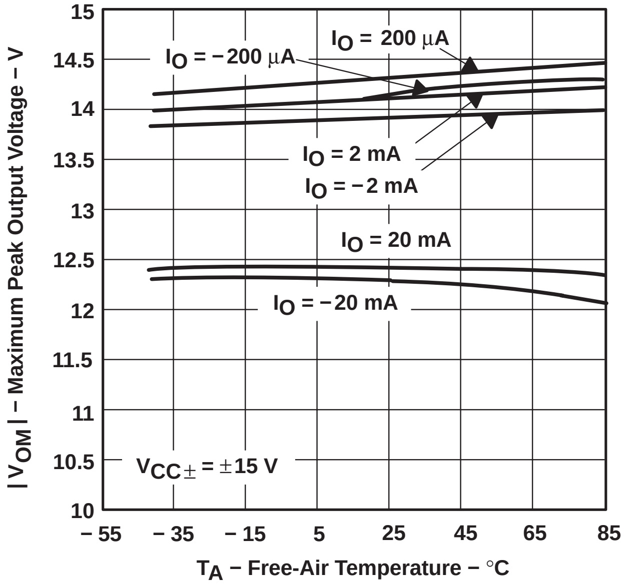

Figure 18

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

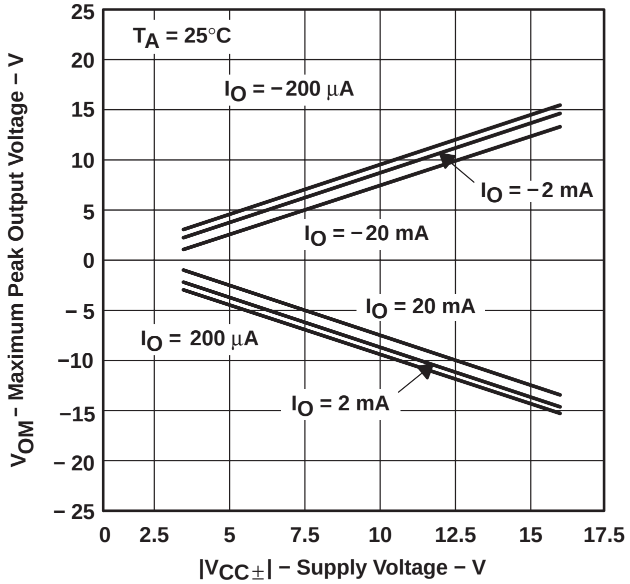
MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

Figure 19

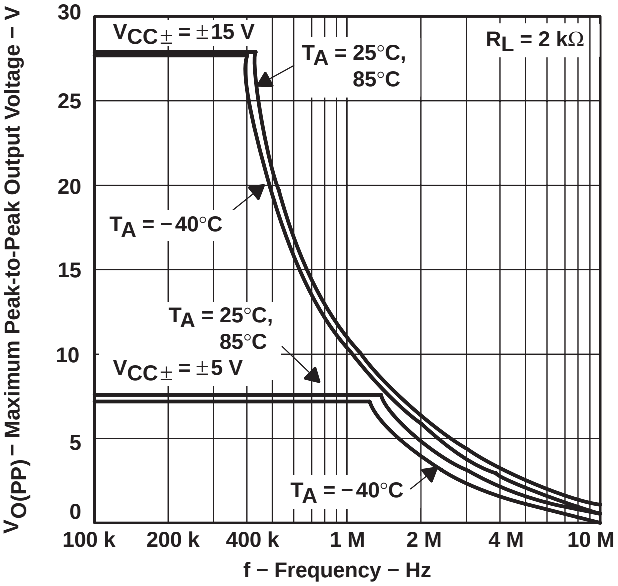
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 20

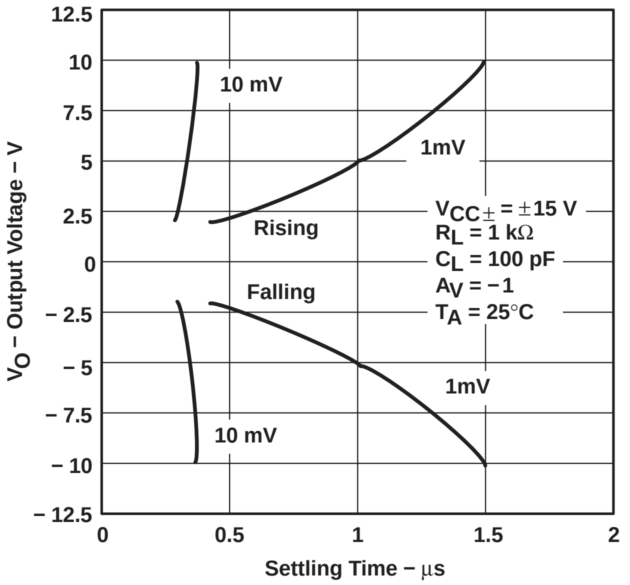
OUTPUT VOLTAGE
vs
SETTLING TIME

Figure 21

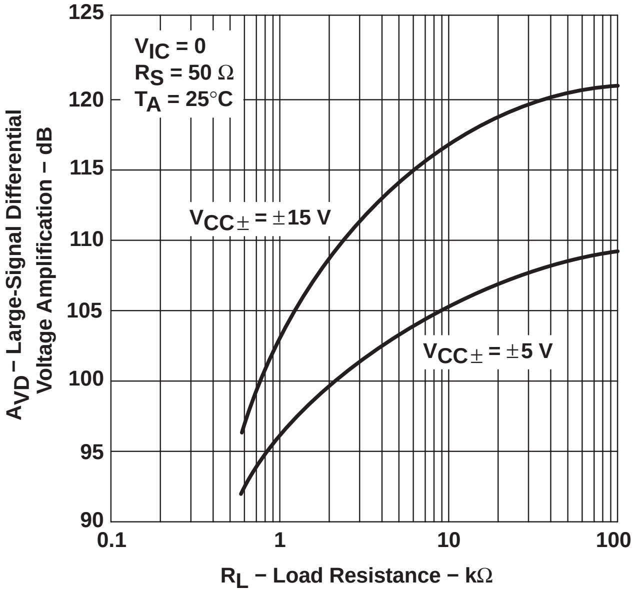
LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

Figure 22

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

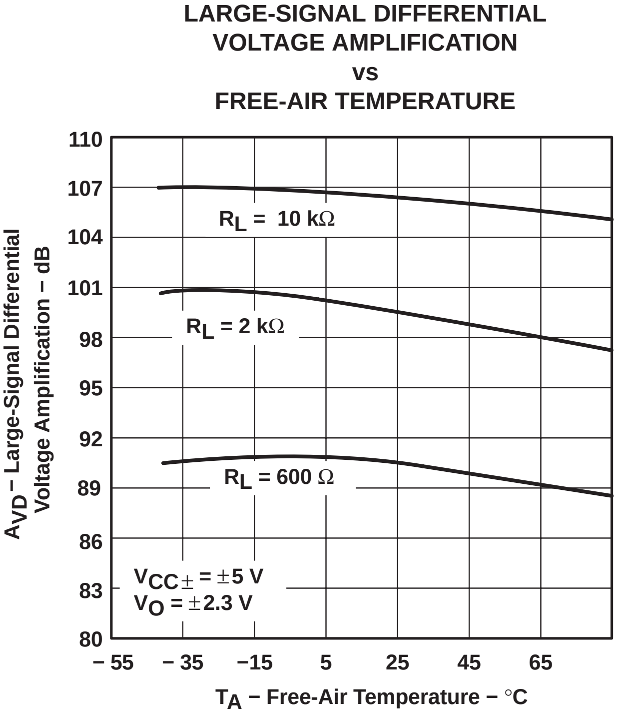

Figure 23

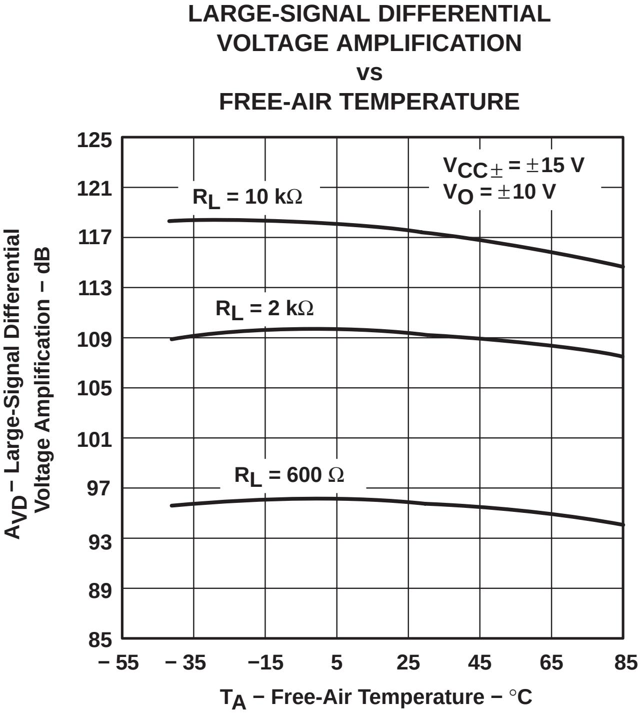

Figure 24

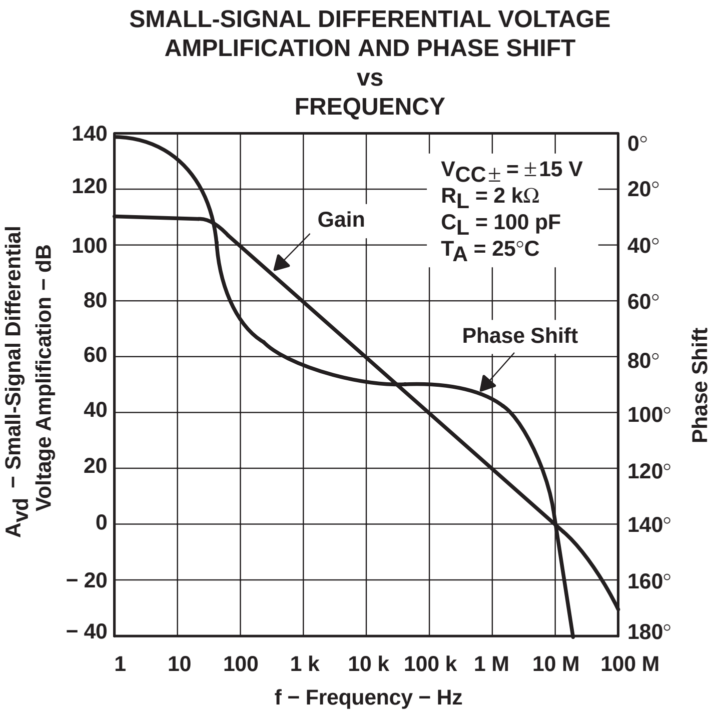

Figure 25

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

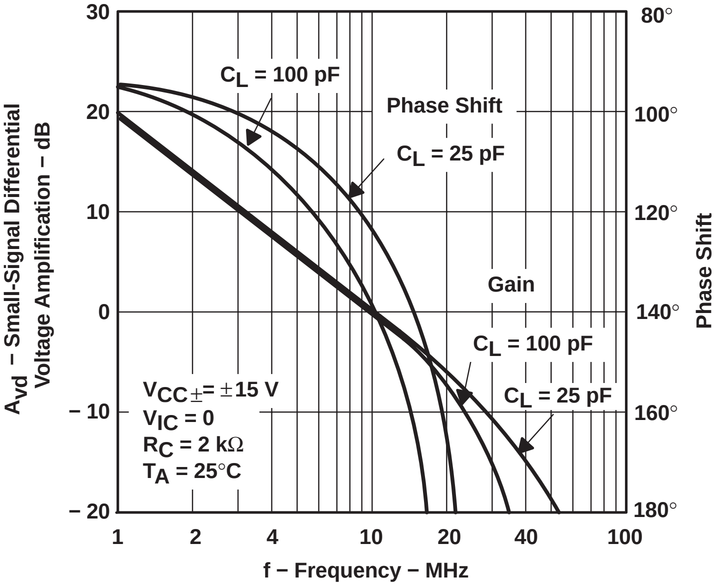

Figure 26

COMMON-MODE REJECTION RATIO vs FREQUENCY

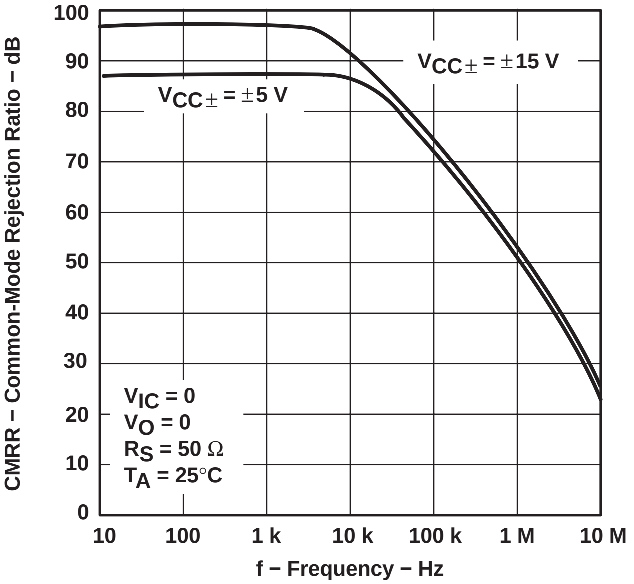

Figure 27

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

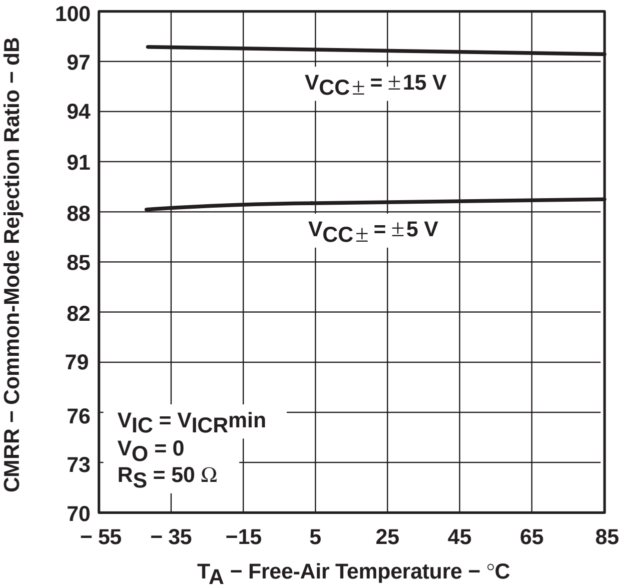

Figure 28

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

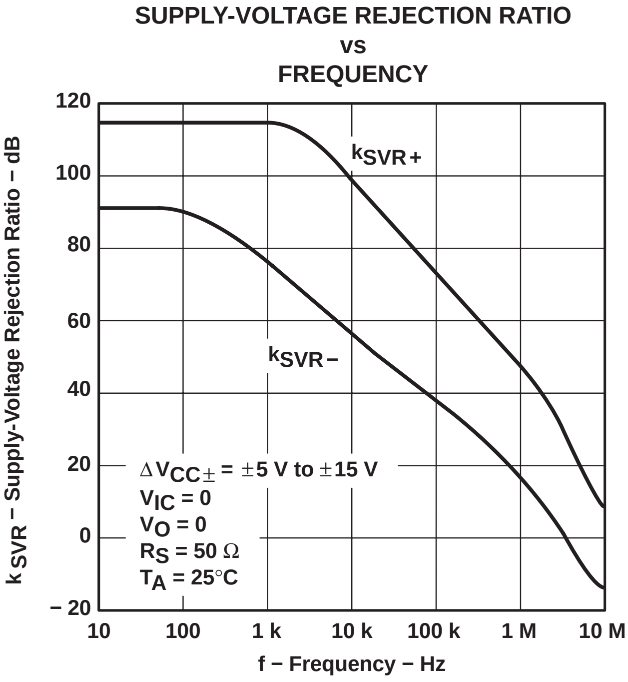

Figure 29

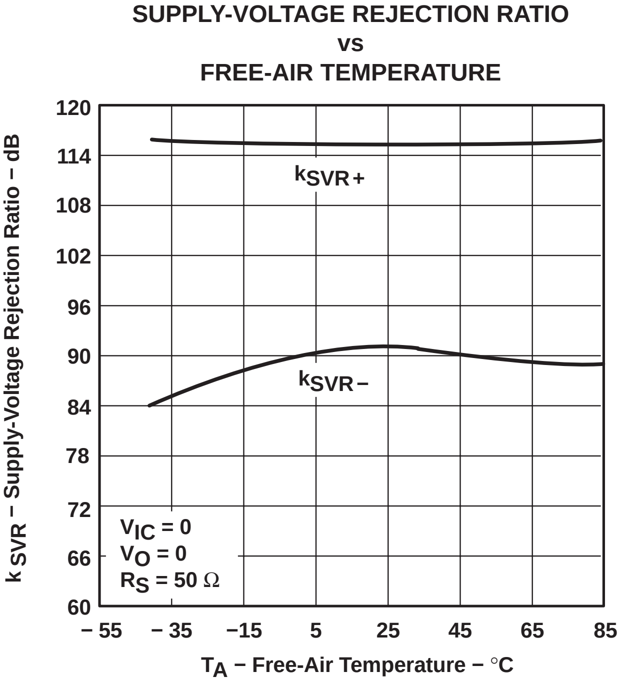

Figure 30

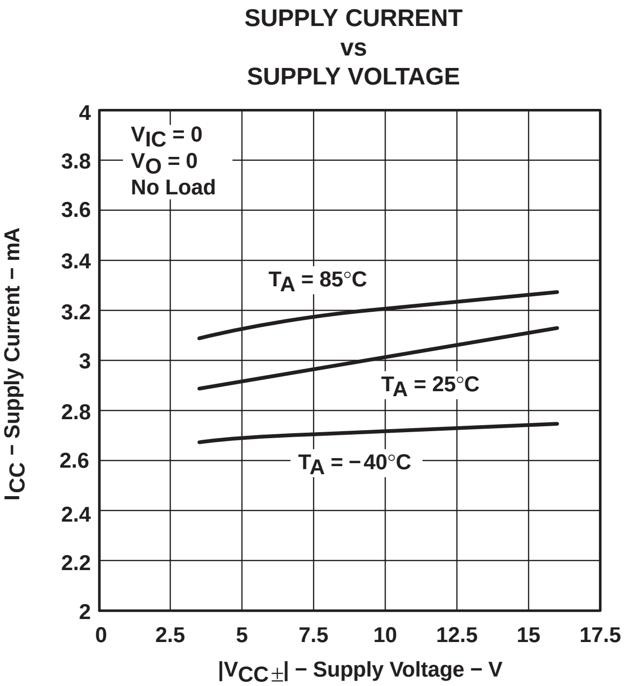

Figure 31

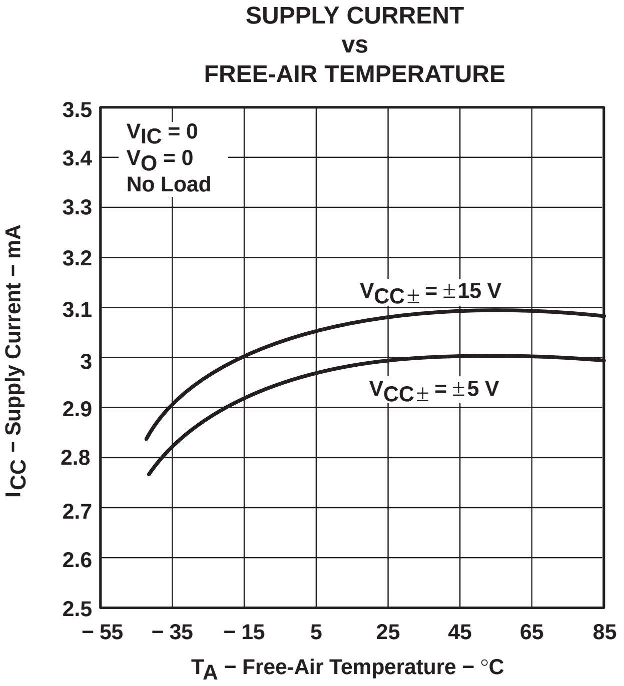

Figure 32

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

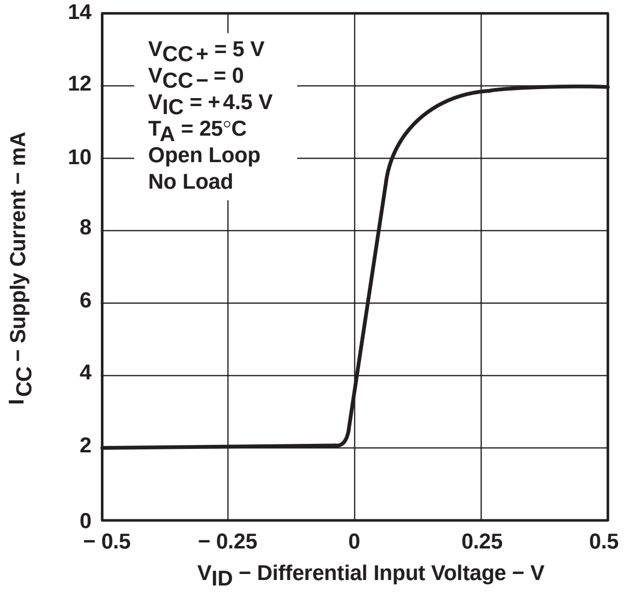

Figure 33

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

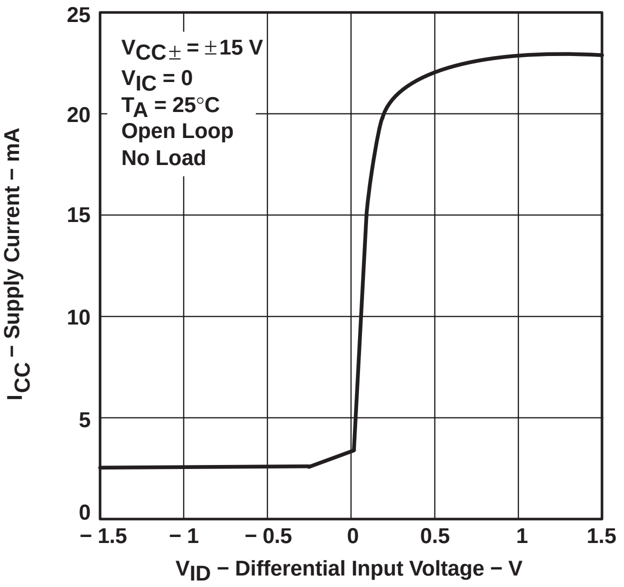

Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

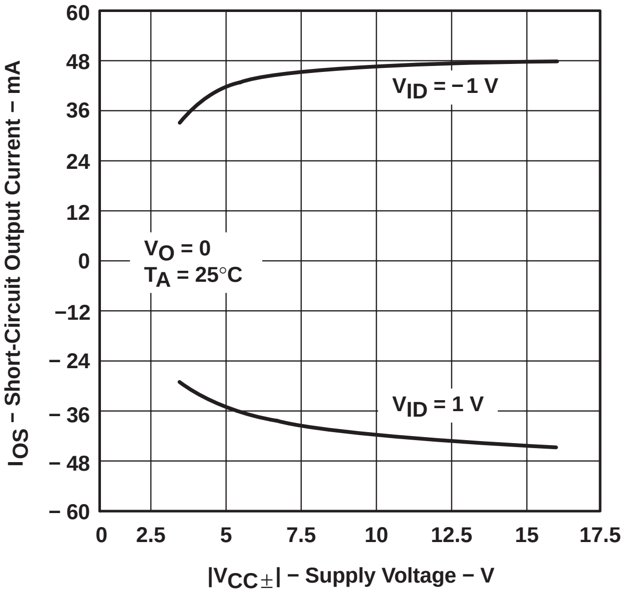

Figure 35

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

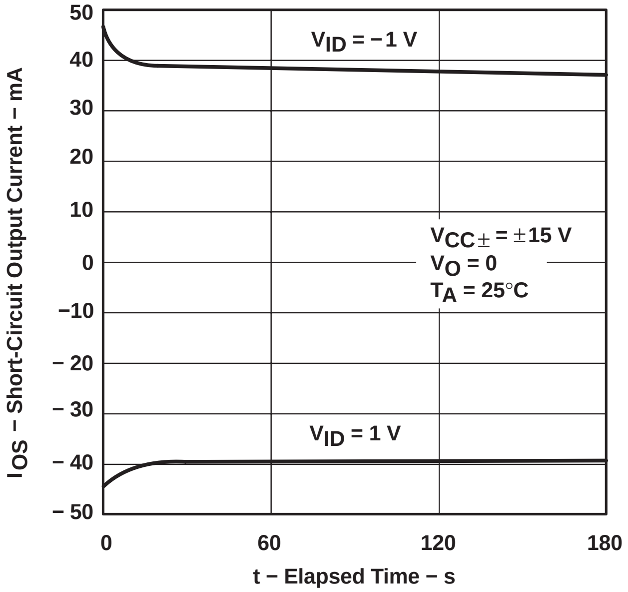

Figure 36

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

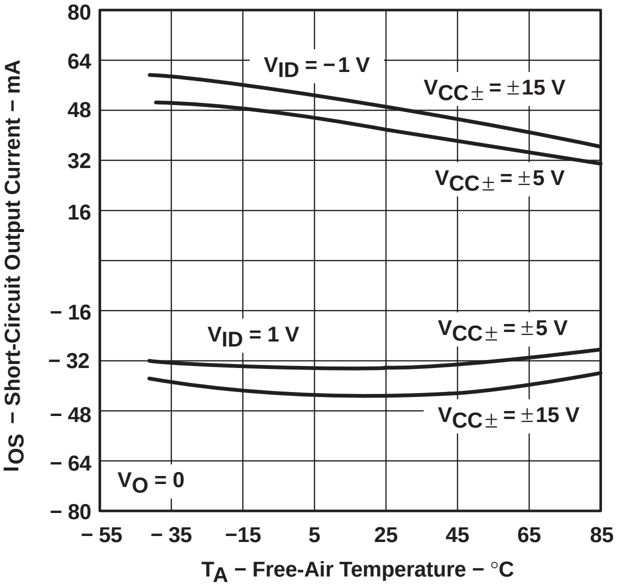

Figure 37

SLEW RATE
vs
FREE-AIR TEMPERATURE

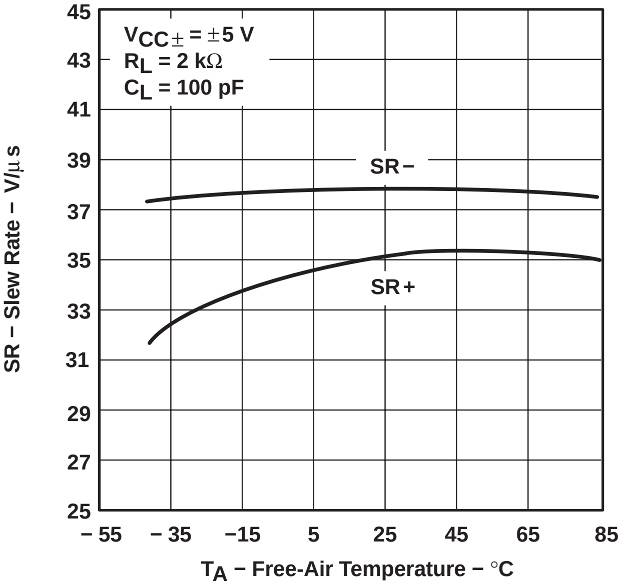

Figure 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

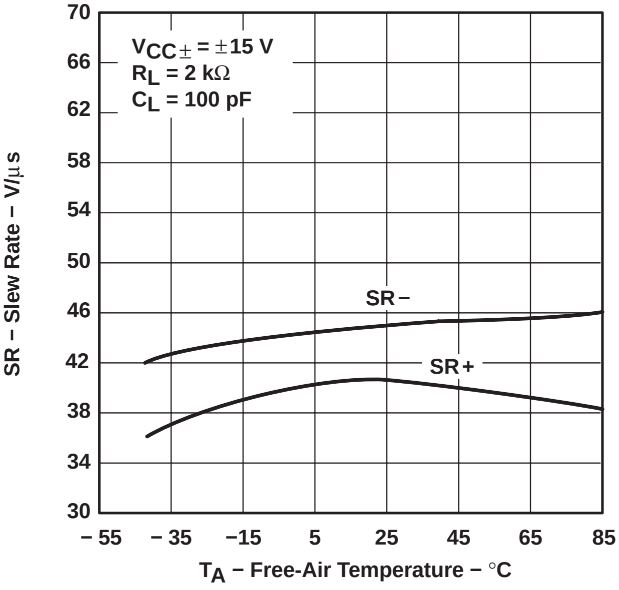

Figure 39

SLEW RATE
vs
LOAD RESISTANCE

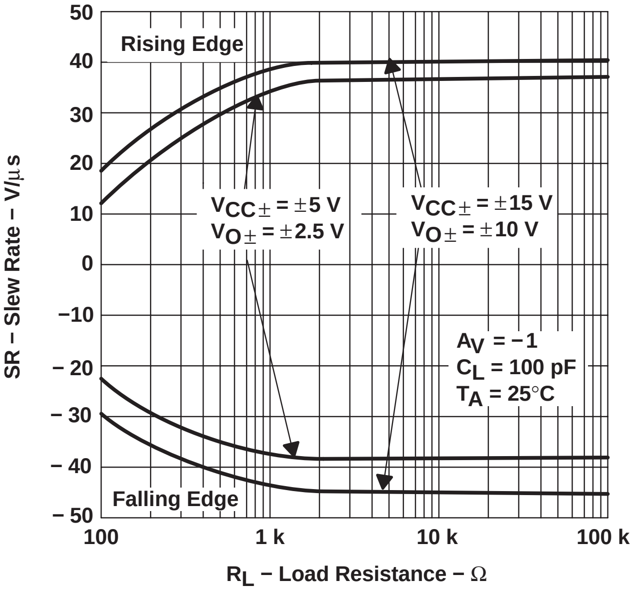

Figure 40

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

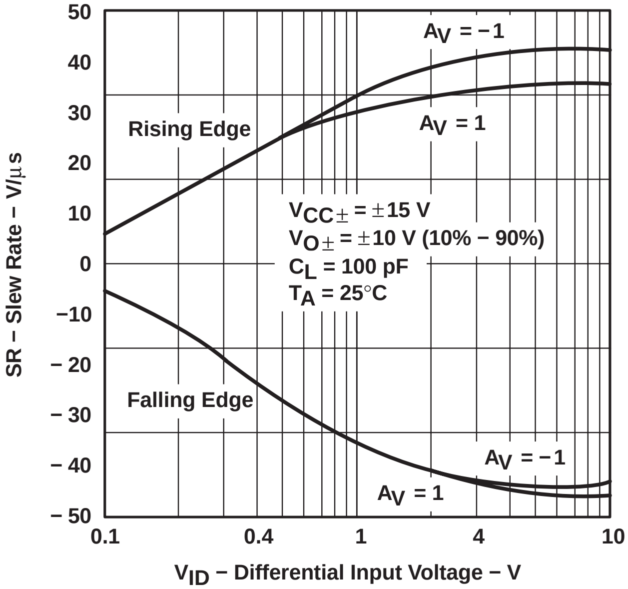

Figure 41

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

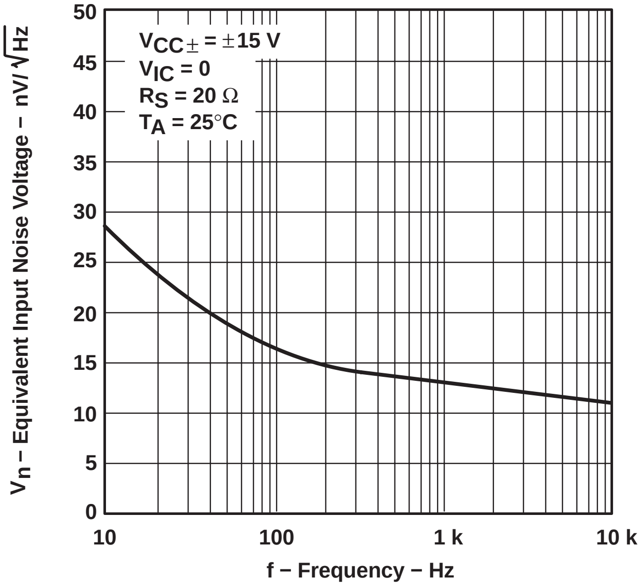

Figure 42

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

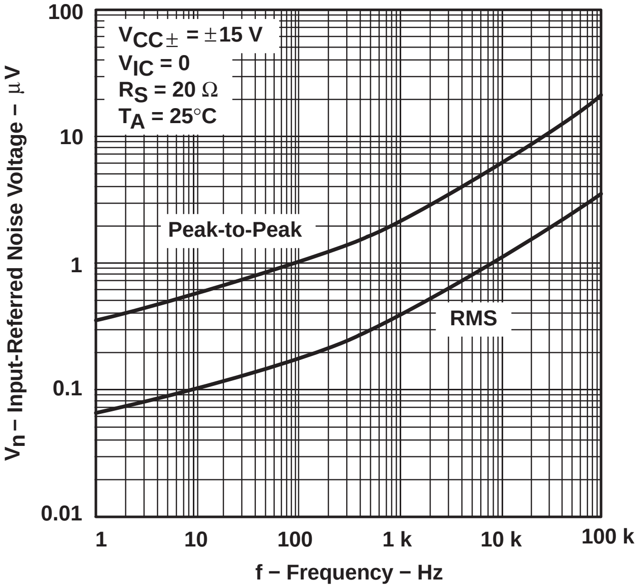

Figure 43

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

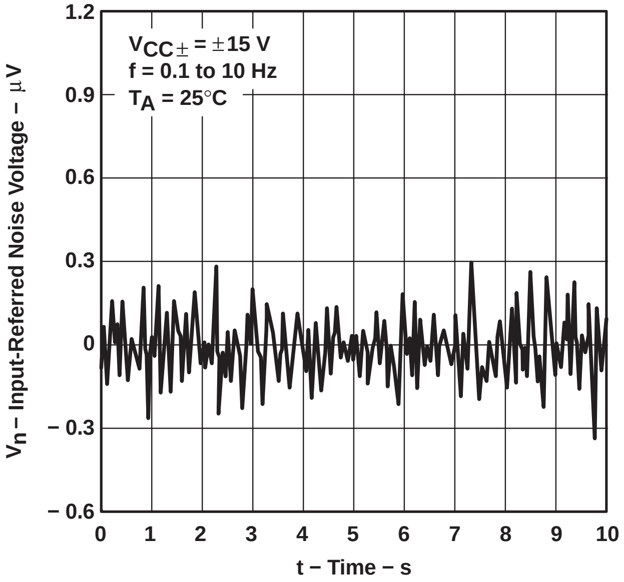

Figure 44

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS[†]
OPERATIONAL AMPLIFIER SECTION

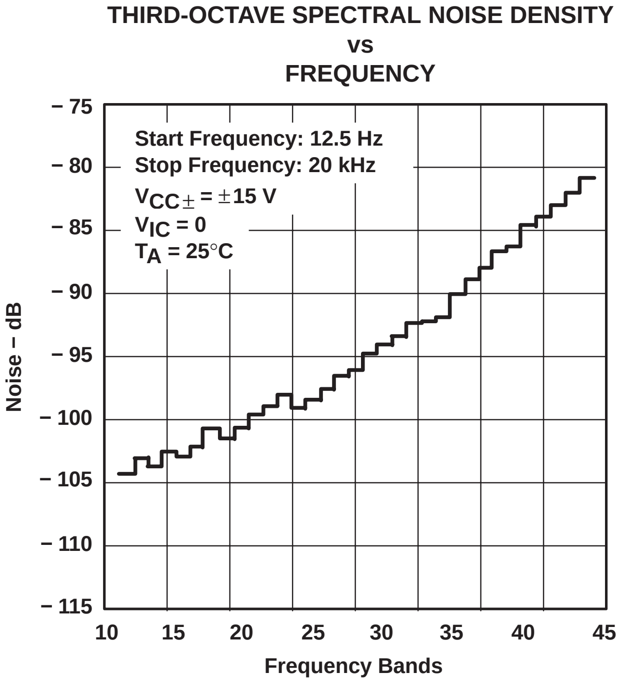

Figure 45

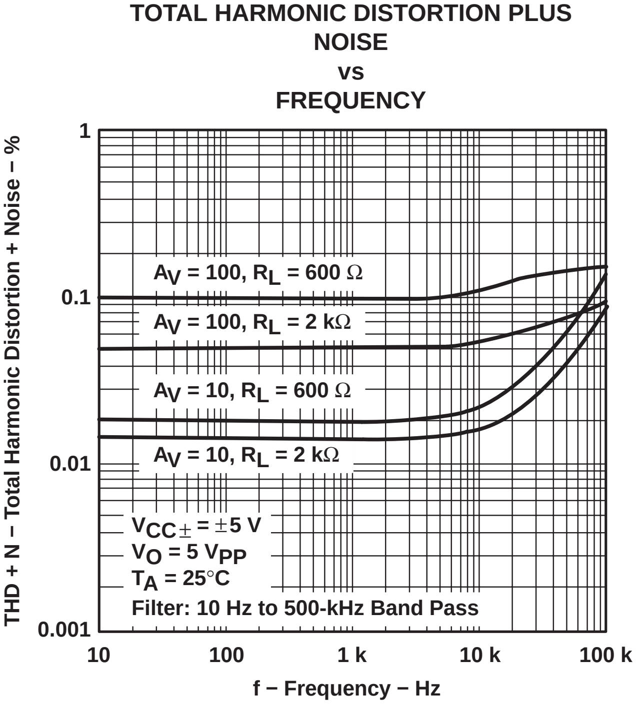

Figure 46

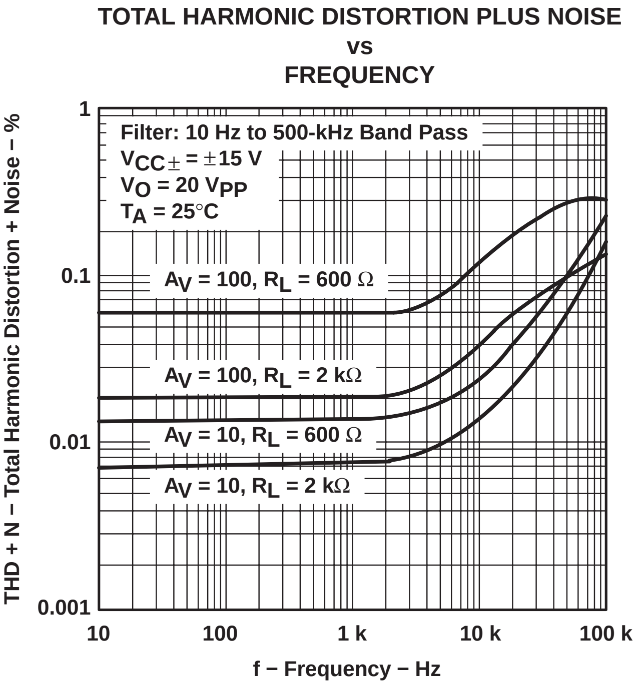

Figure 47

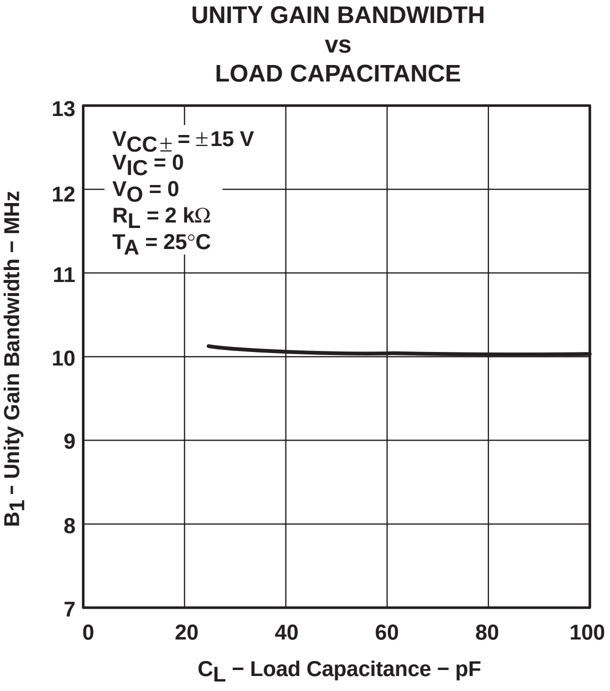

Figure 48

[†] Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

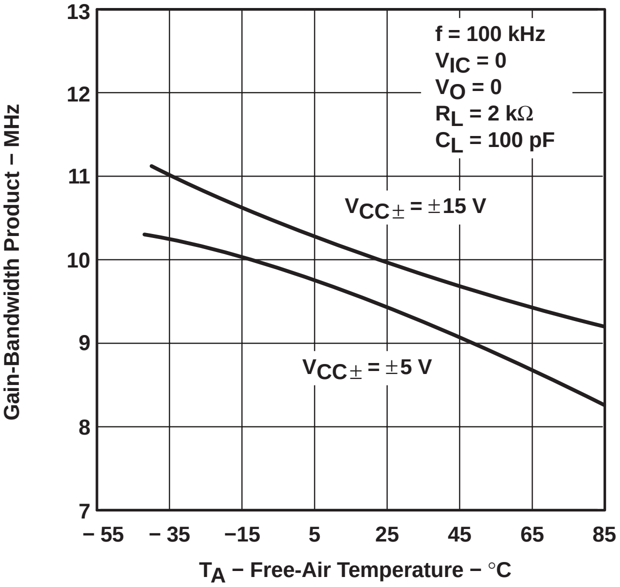

Figure 49

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

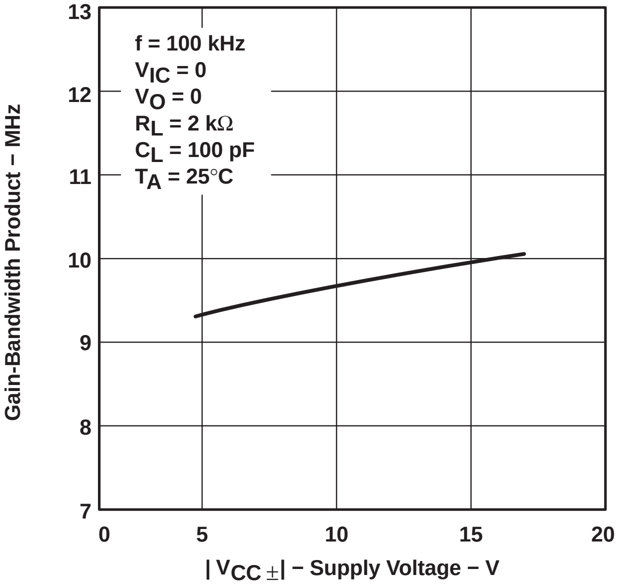

Figure 50

GAIN MARGIN
vs
LOAD CAPACITANCE

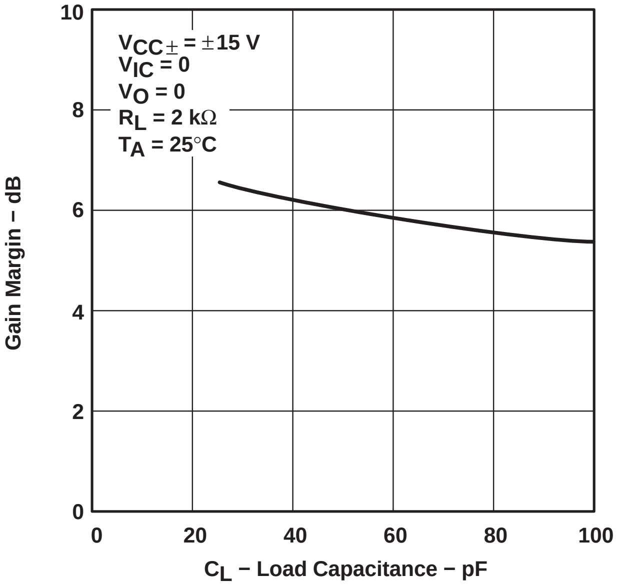

Figure 51

PHASE MARGIN
vs
TEMPERATURE

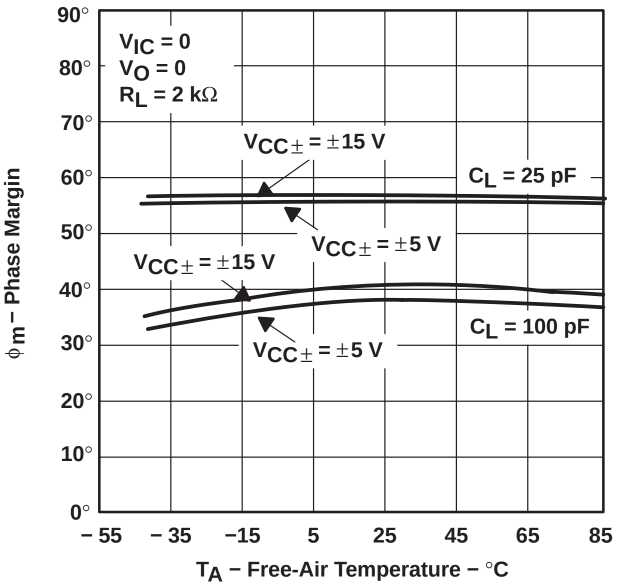

Figure 52

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

PHASE MARGIN vs SUPPLY VOLTAGE

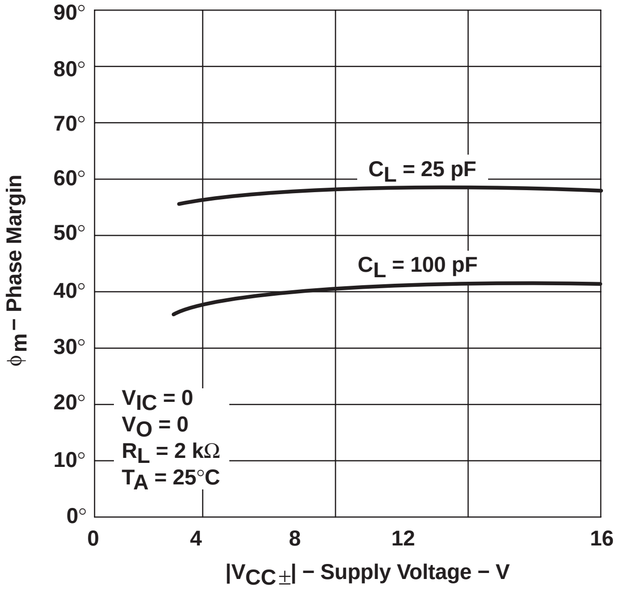

Figure 53

PHASE MARGIN vs LOAD CAPACITANCE

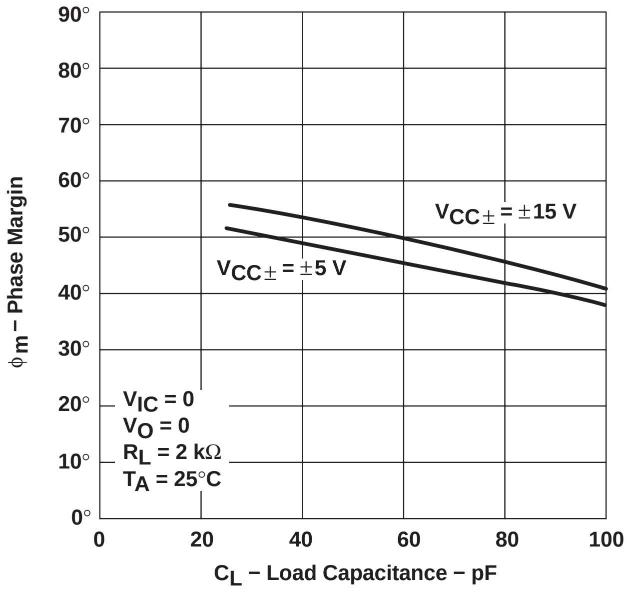

Figure 54

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

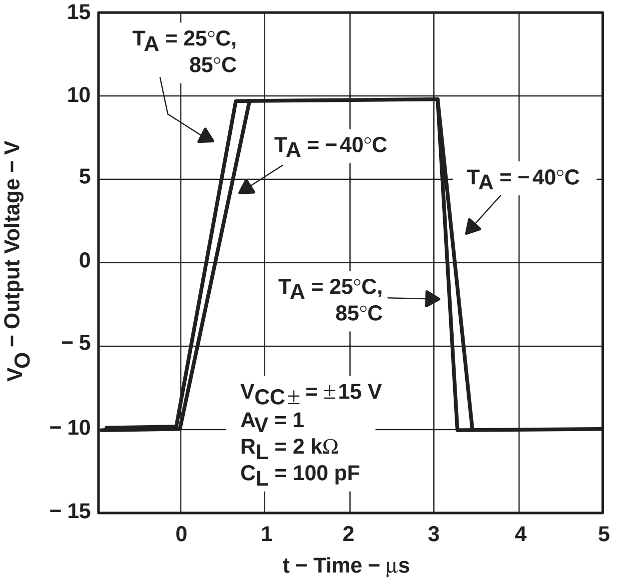

Figure 55

SMALL-SIGNAL PULSE RESPONSE

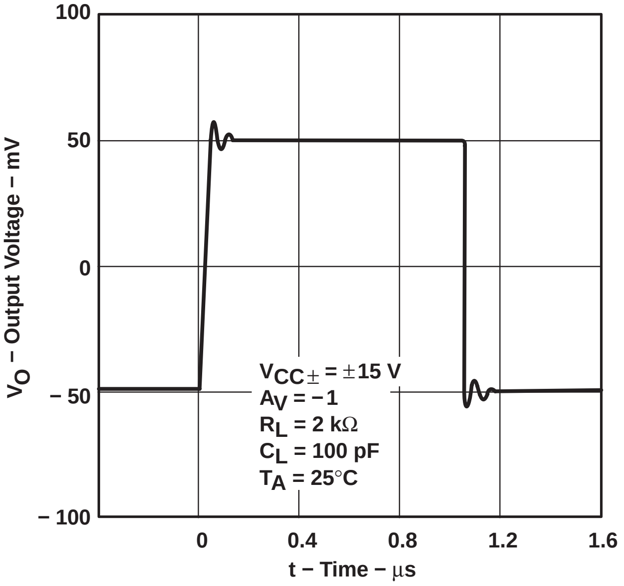

Figure 56

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† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS[†]
OPERATIONAL AMPLIFIER SECTION

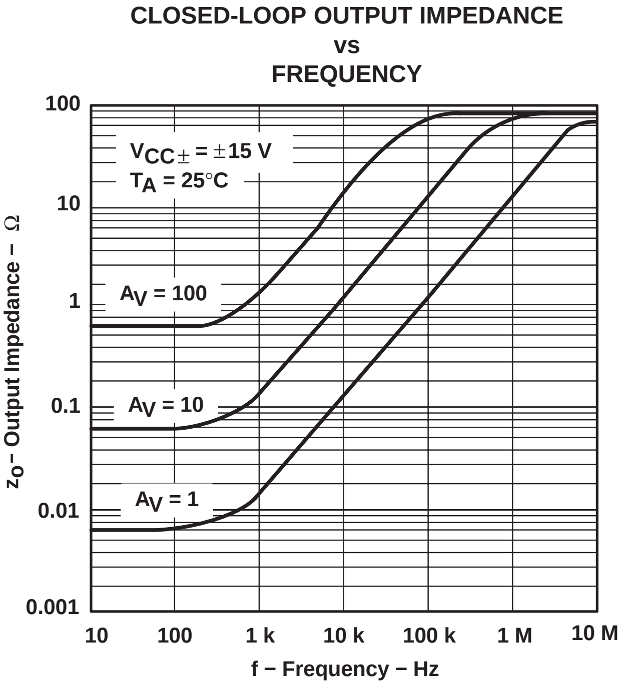

Figure 57

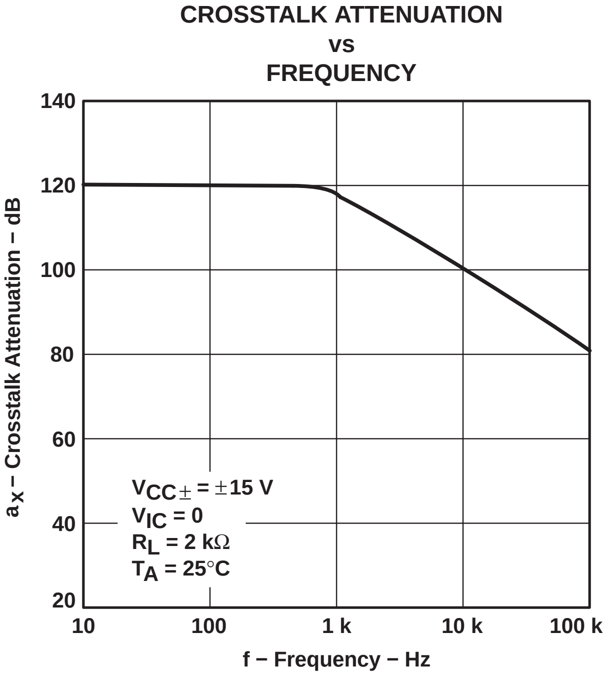

Figure 58

[†] Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

SHUTDOWN THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

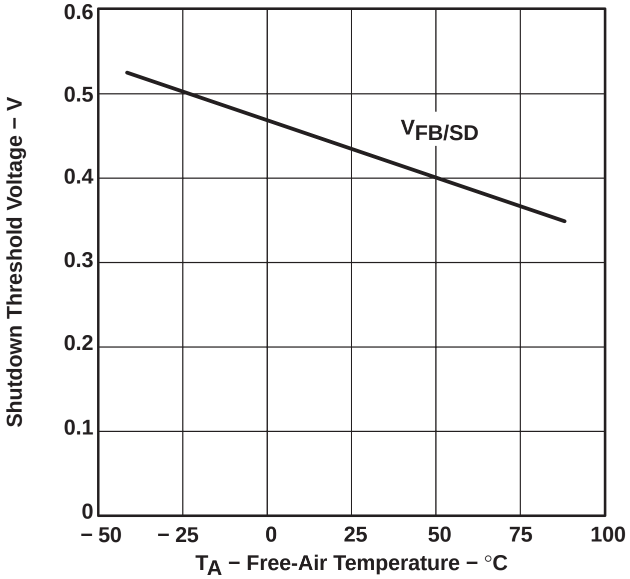

Figure 59

SUPPLY CURRENT vs INPUT VOLTAGE

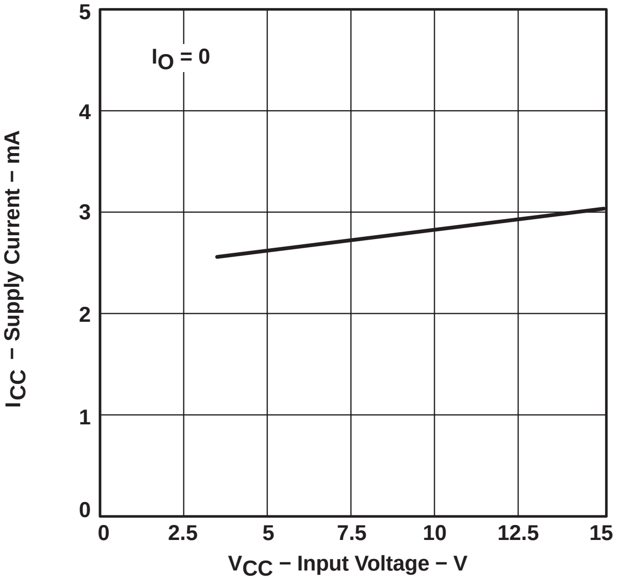

Figure 60

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

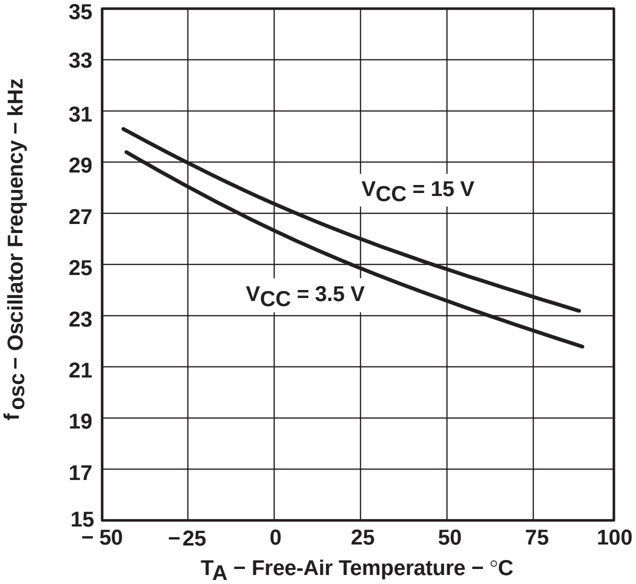

Figure 61

SUPPLY CURRENT IN SHUTDOWN vs INPUT VOLTAGE

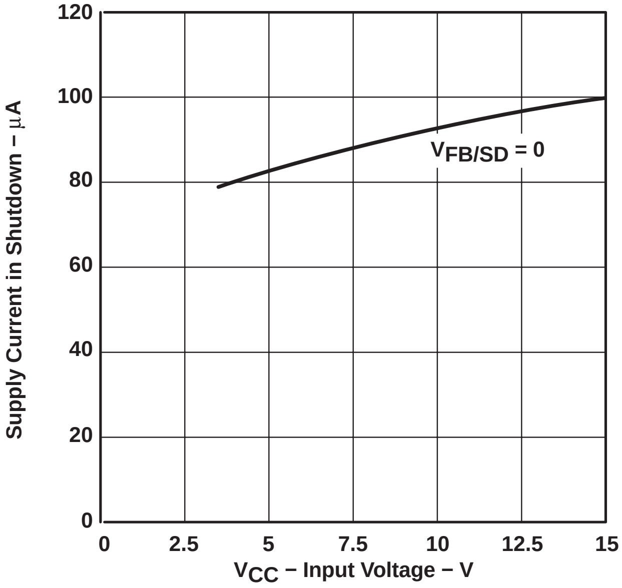

Figure 62

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† Data applies to the switched-capacitor block only. Amplifier block is not connected.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

AVERAGE SUPPLY CURRENT
vs
OUTPUT CURRENT

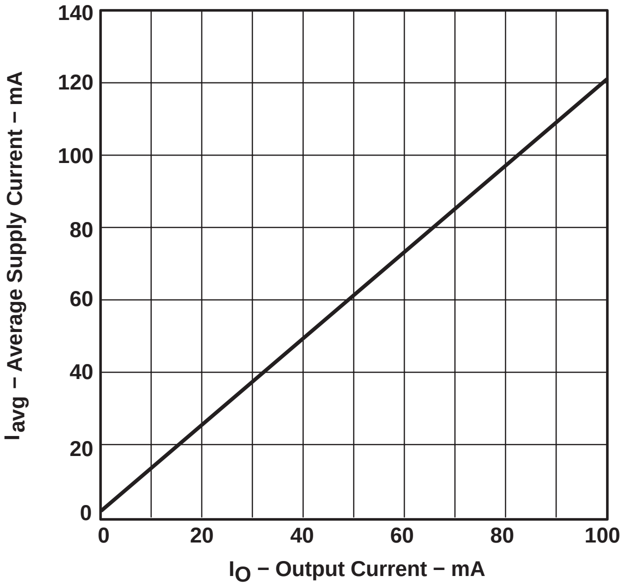

Figure 63

OUTPUT VOLTAGE LOSS
vs
INPUT CAPACITANCE

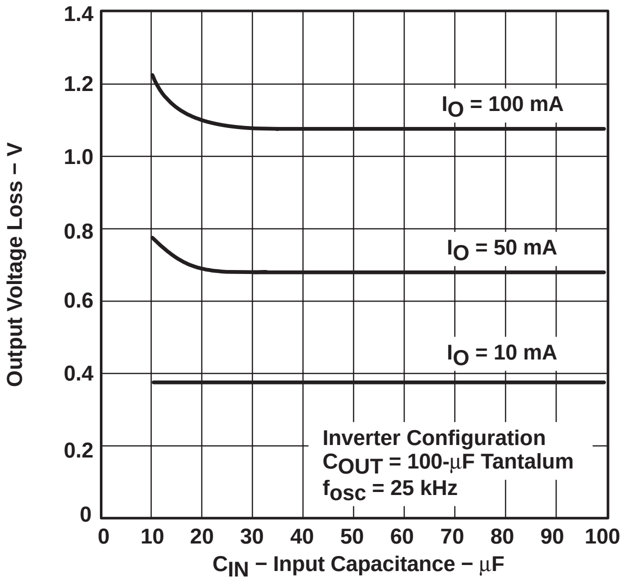

Figure 64

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

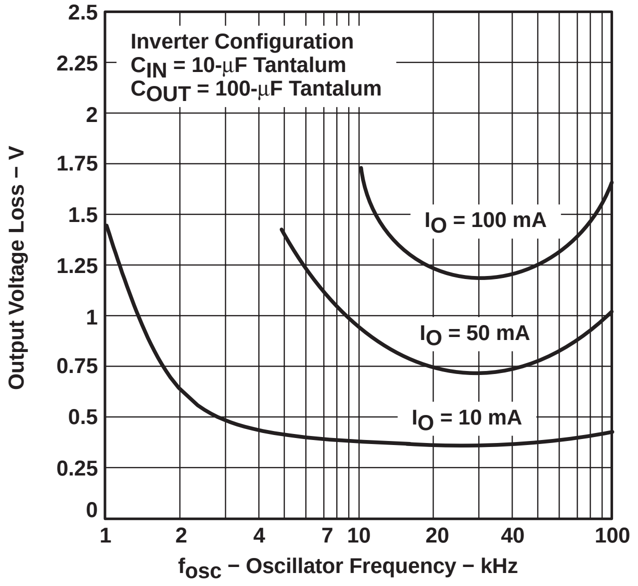

Figure 65

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

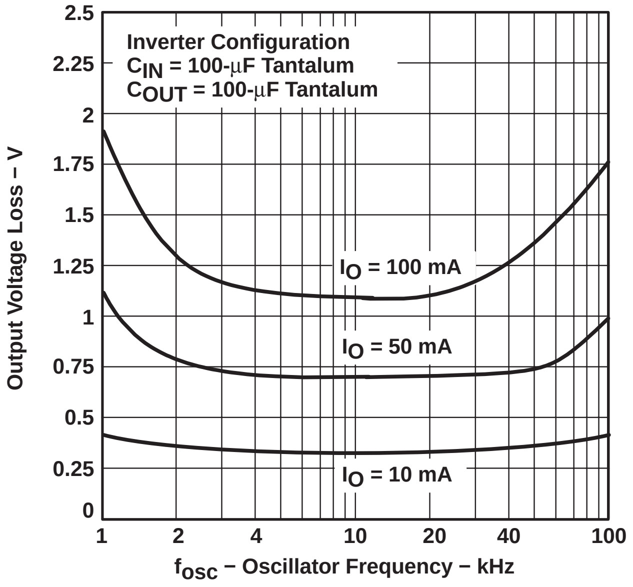

Figure 66

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† Data applies to the switched-capacitor block only. Amplifier block is not connected.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

REGULATED OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

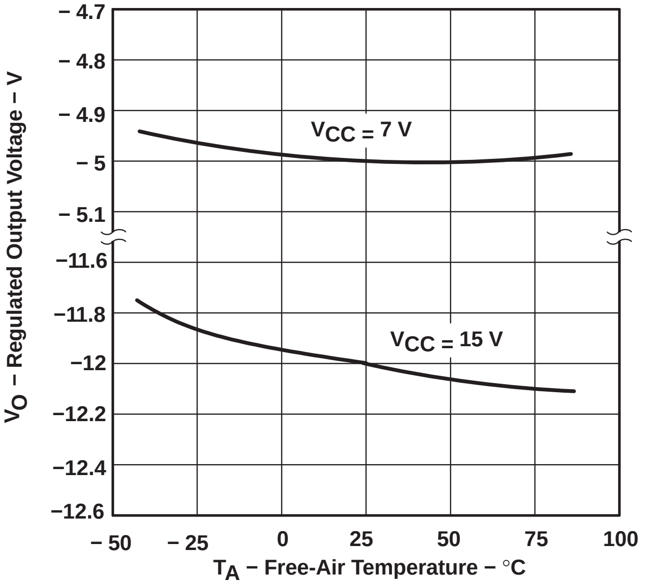

Figure 67

REFERENCE VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

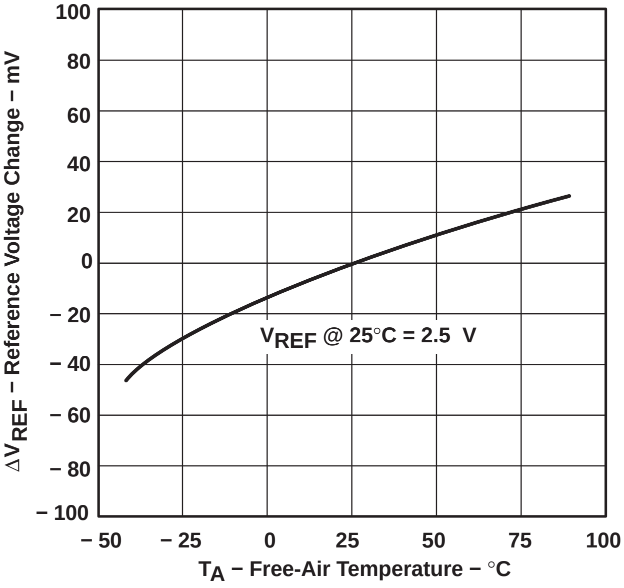

Figure 68

VOLTAGE LOSS
vs
OUTPUT CURRENT

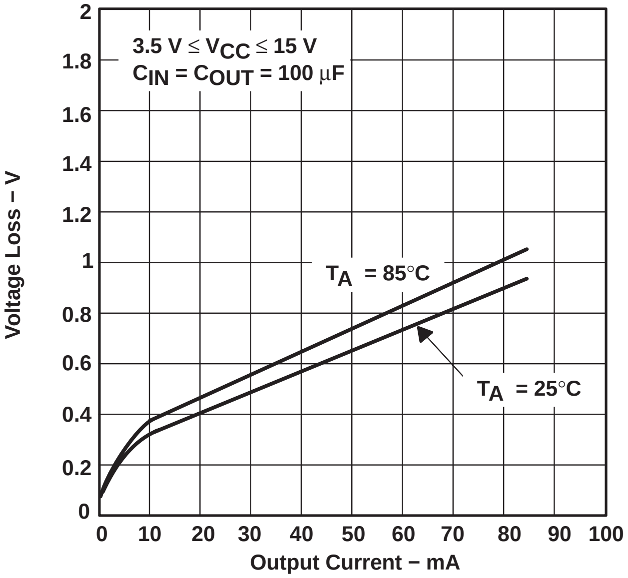

Figure 69

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† Data applies to the switched-capacitor block only. Amplifier block is not connected.

APPLICATION INFORMATION

amplifier section

input characteristics

The TLE2682 is specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2682 operational amplifier section is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 70). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded voltage followers to avoid potential oscillation.

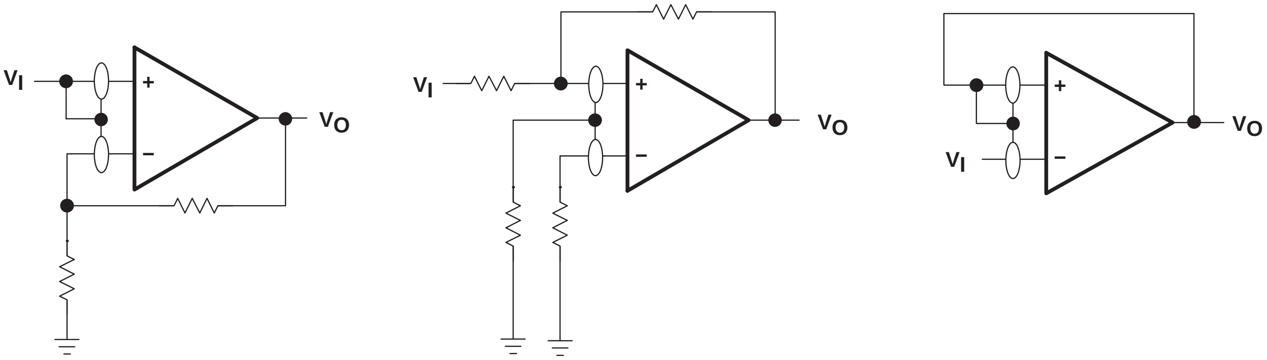
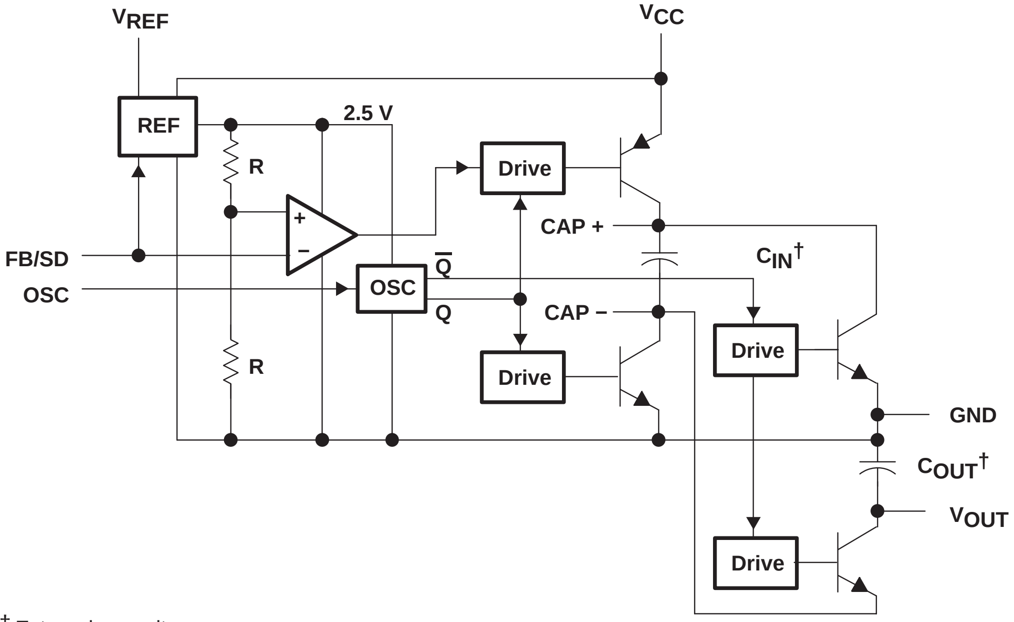


Figure 70. Use of Guard Rings

switched-capacitor section

Figure 71 shows the functional block diagram for the switched-capacitor block only.



† External capacitors

Figure 71. Functional Block Diagram for Switched-Capacitor Block Only

APPLICATION INFORMATION

The TLE2682 high-speed JFET-input amplifiers are ideal for conditioning fast signals from high-impedance sources. When interfacing with ADCs in single-supply 5-V systems, its on board charge pump provides the negative rail necessary for reliable operation of the JFET inputs and delivers a common-mode input voltage range that includes ground and the positive rail. The amplifiers can also drive resistive loads to 0.000 V while sinking 25 mA.

Figure 72 shows the switched-capacitor section configured as a voltage inverter generating approximately −5-V supply voltage from the single 5-V supply available. Three external components are necessary: the storage capacitors, C_{IN} and C_{OUT}, and a fast recovery Schottky diode to clamp V_{OUT} during start-up. The diode is necessary because the amplifiers present a load referenced to the positive rail and tend to pull V_{OUT} above ground, which may prevent the switched-capacitor section from starting (see section on pin functions). The amplifiers use the 5-V supply for V_{CC+} (pin 16) and the derived −5-V supply for V_{CC-} (pin 4). One amplifier is shown driving an ADC; the other is driving a resistive load (see Figure 73).

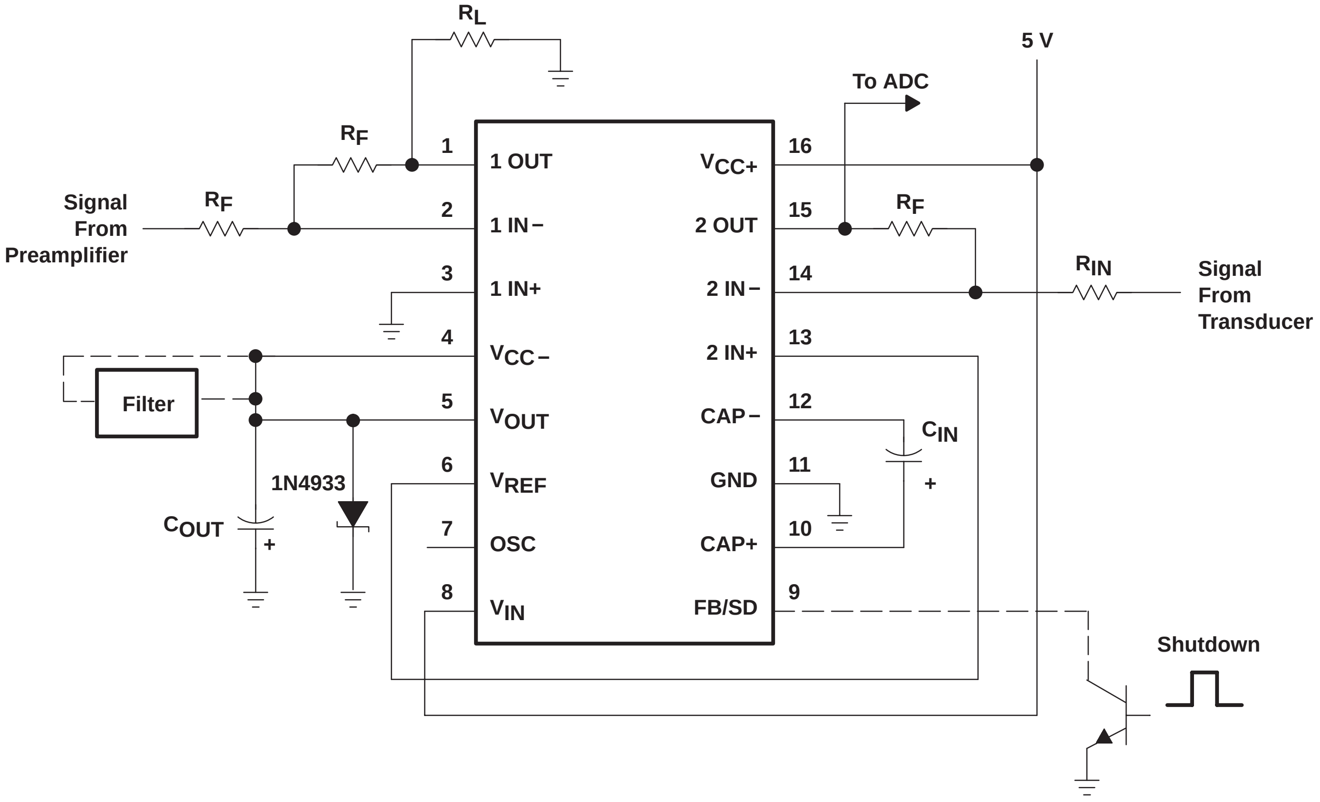


Figure 72. Switched-Capacitor Block Supplying Negative Rail for Amplifiers

APPLICATION INFORMATION

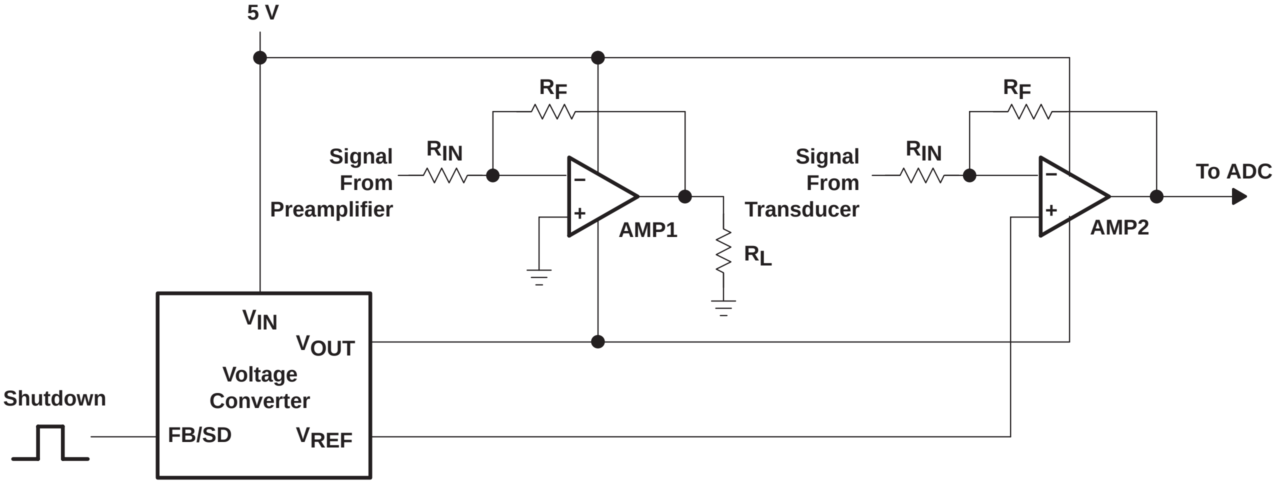


Figure 73. Equivalent Schematic: Amplifier 1 Driving Resistive Load, Amplifier 2 Interfacing to an ADC

Using the switched-capacitor network to generate the negative rail for the amplifiers (or other circuitry) requires special design considerations to minimize the effects of ripple and switching noise. Using larger values for C_{OUT} and selecting low-ESR capacitors reduces the ripple and noise present on V_{OUT}, the − 5-V rail (refer to the capacitor section and the output ripple discussion in the switched-capacitor section). Figure 74 and Figure 75 show the smoothing effect of changing C_{OUT} from 10 µF to 100 µF when V_{OUT} is supplying 1 mA. Figure 76 and Figure 77 demonstrate that at heavier loads the ripple and noise are more pronounced and while increasing the size of C_{OUT} helps, other steps may be necessary.

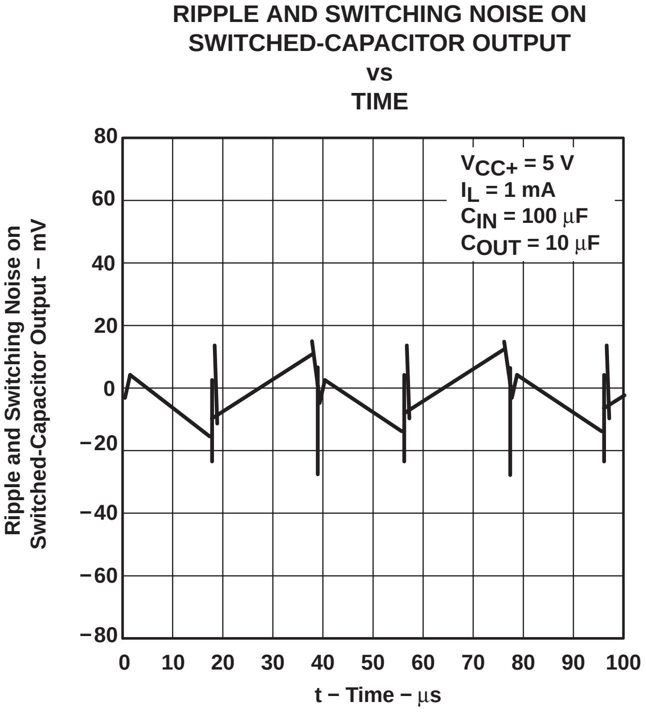


Figure 74

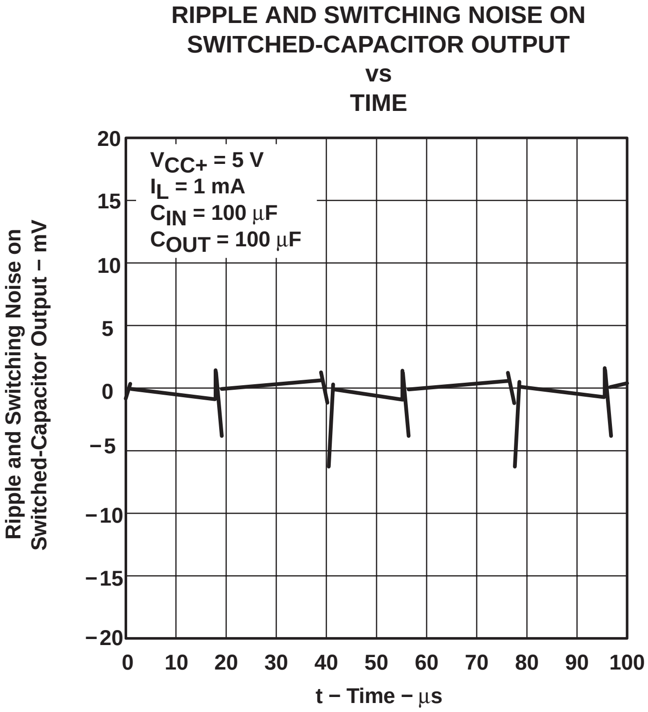


Figure 75

APPLICATION INFORMATION

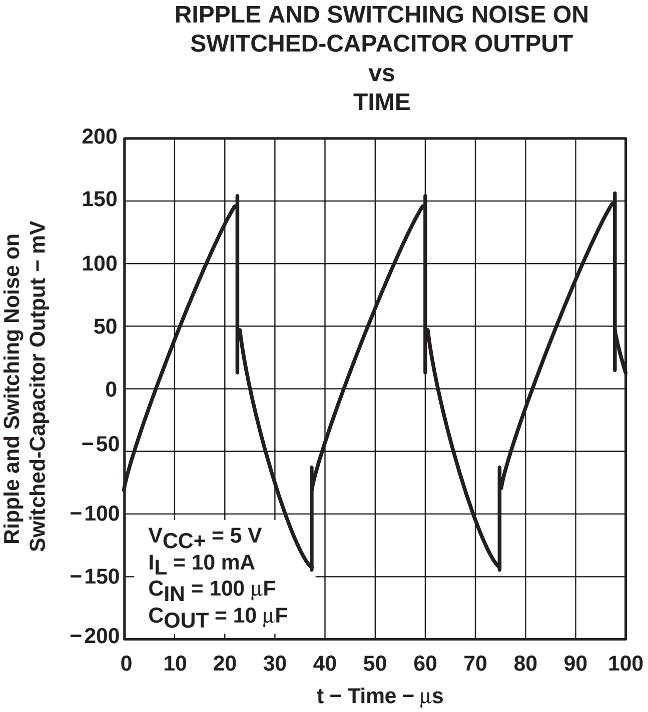


Figure 76

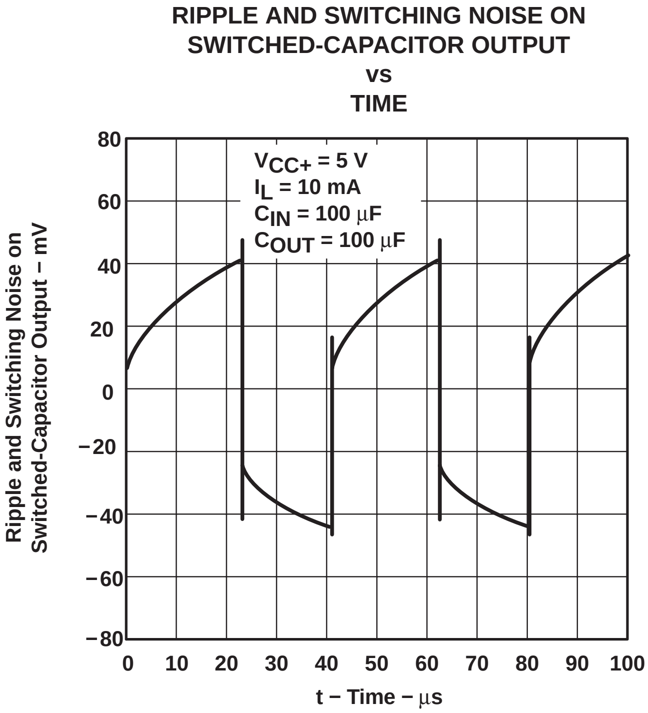


Figure 77

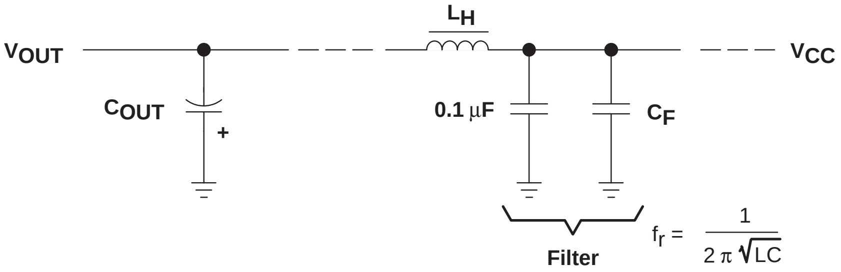


Figure 78. LC Filter Used to Reduce Ripple and Switching Noise, $f_r = 1/2\pi\sqrt{LC}$, A = −40 dB per Decade

A low-pass LC filter can be added to the circuit to further reduce ripple and noise. For example, adding a filter as shown in Figure 78, implemented using a 50-µH inductor and 200-µF capacitor (available in surface mount), achieves the following results (see Figure 79 through Figure 82).

APPLICATION INFORMATION

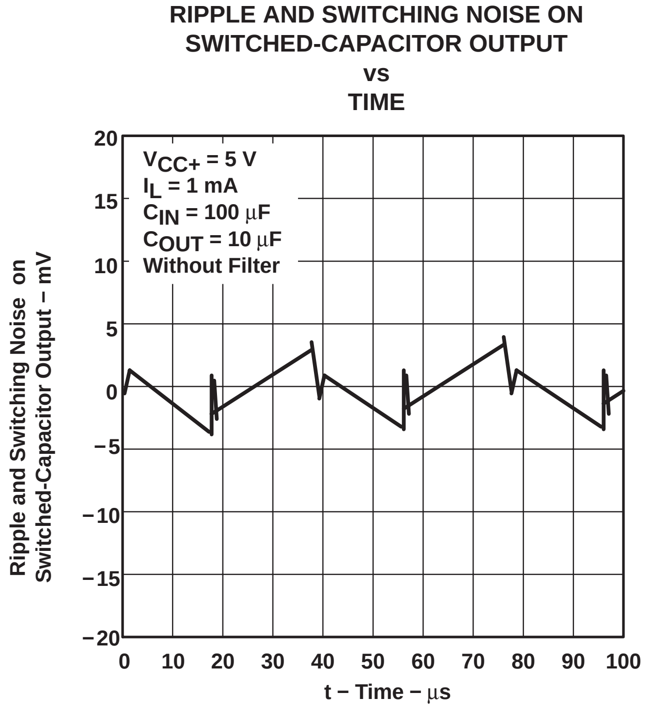

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

Figure 79

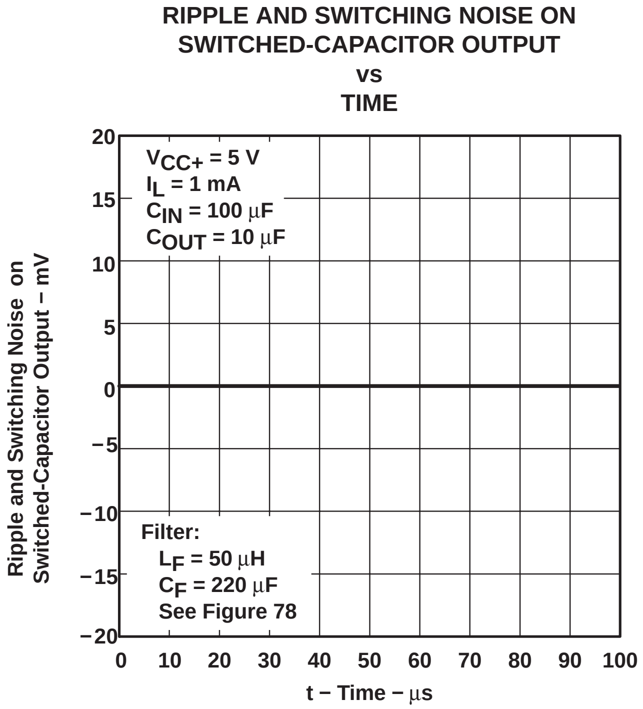

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

Figure 80

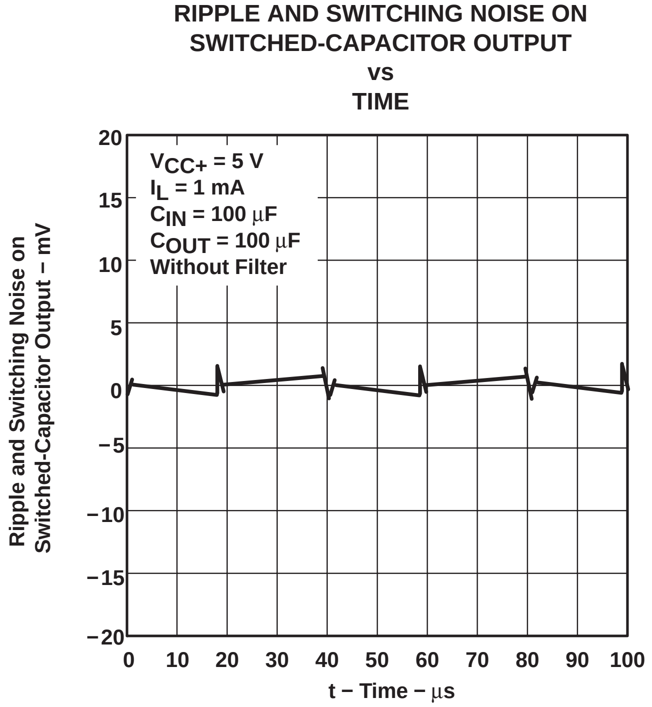

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

Figure 81

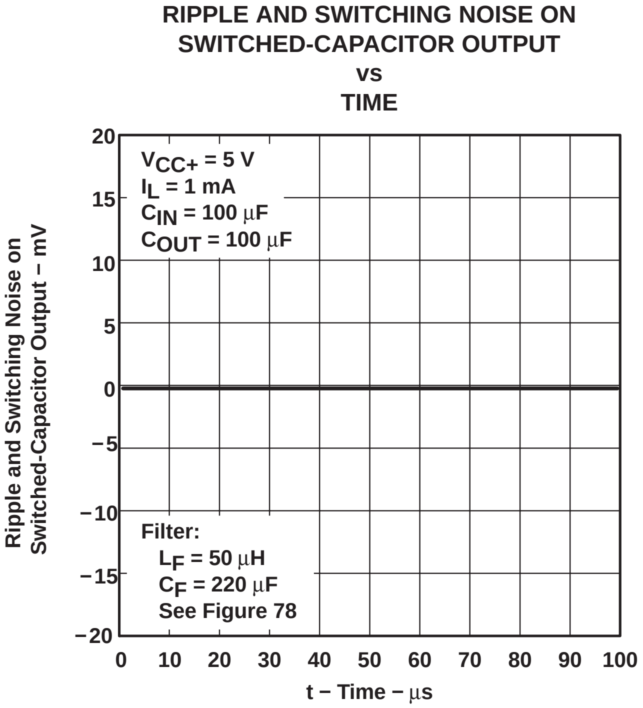

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

Figure 82

APPLICATION INFORMATION

As the load increases, filtering is still effective, but noise and ripple become more prominent (see Figure 83 through Figure 86):

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

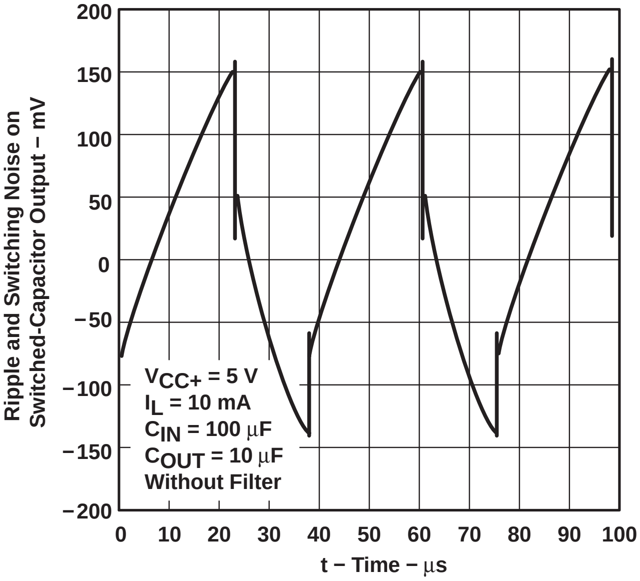


Figure 83

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

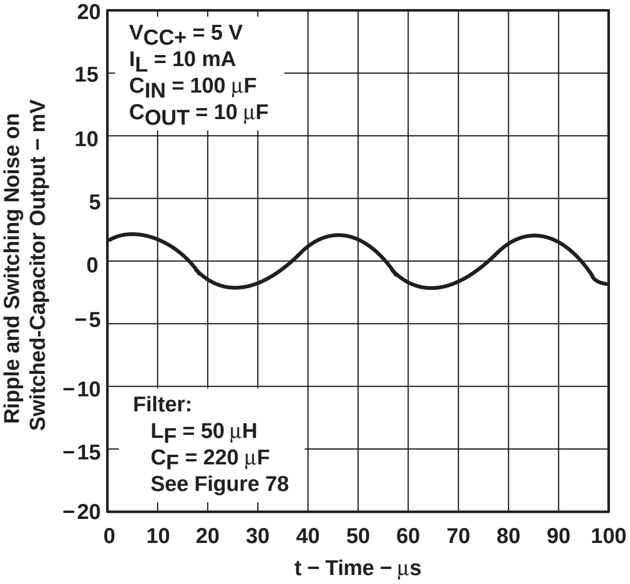


Figure 84

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

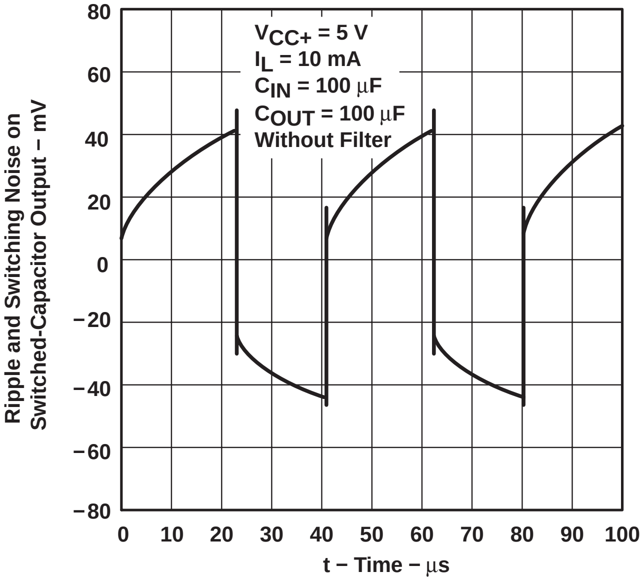


Figure 85

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

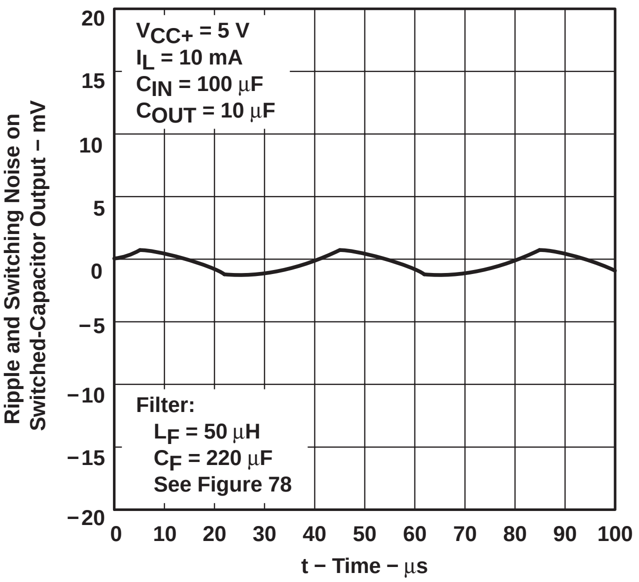


Figure 86

APPLICATION INFORMATION

Even with filtering, switching noise is coupled into the amplifier’s signal path through ground. An example of this is shown in Figure 87 and Figure 88. This cannot be avoided. In systems where high-precision measurement is necessary, the shutdown pin, FB/SD, can be used to temporarily disable the switched-capacitor section while a measurement is being taken.

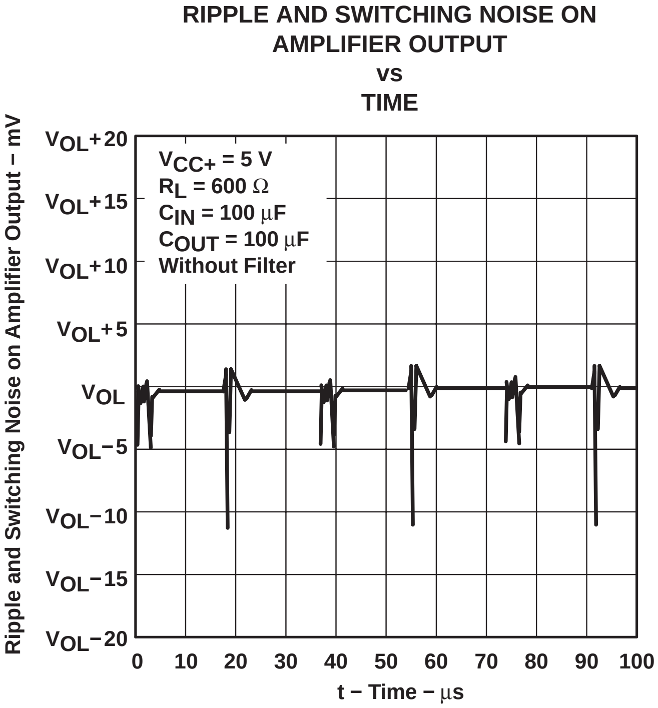


Figure 87

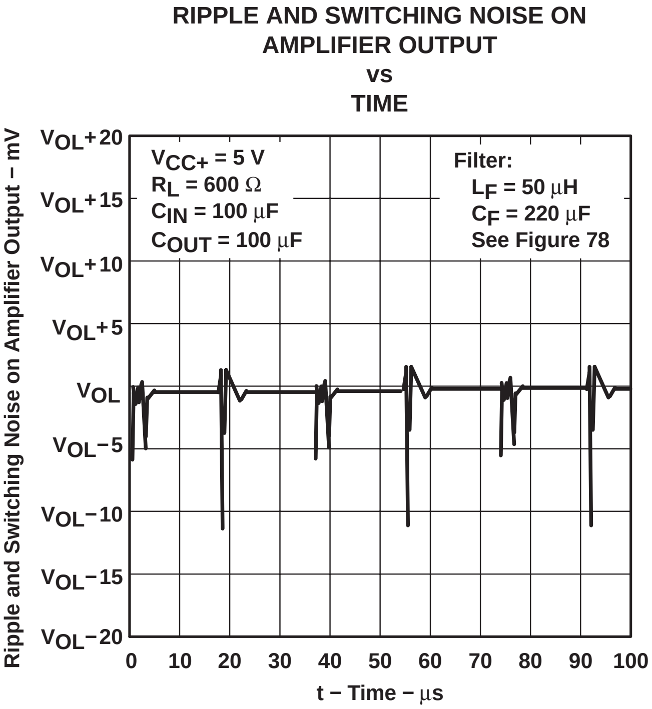


Figure 88

By applying a voltage of less than 0.45 V to FB/SD, the internal switches are set to dump any remaining charge onto C_{OUT}. The voltage at V_{OUT} decays to zero at a rate dependent on both the size of C_{OUT} and loading. During this time, the amplifier’s outputs are free of any switching-induced ripple and noise. Figure 89 and Figure 90 show the decay and charge times of the negative supply when the amplifier is driving a 100-Ω load.

APPLICATION INFORMATION

OFF-STATE VOLTAGE DECAY
AT SWITCHED-CAPACITOR OUTPUT
vs
TIME

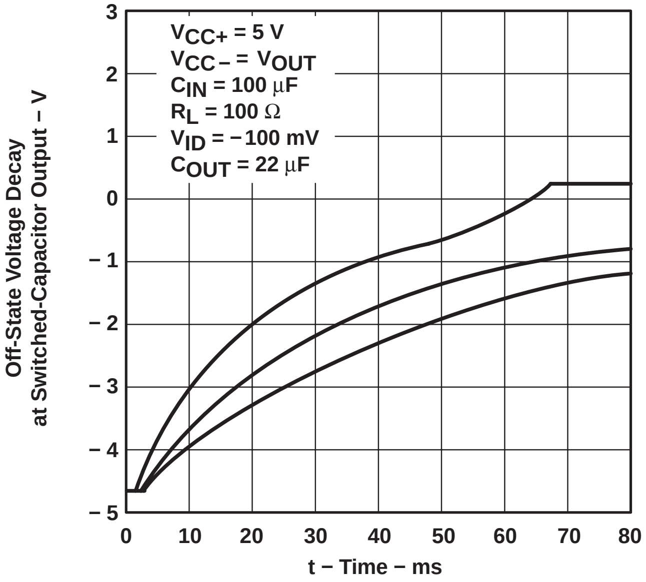


Figure 89

TURN-ON VOLTAGE RISE
AT SWITCHED-CAPACITOR OUTPUT
vs
TIME

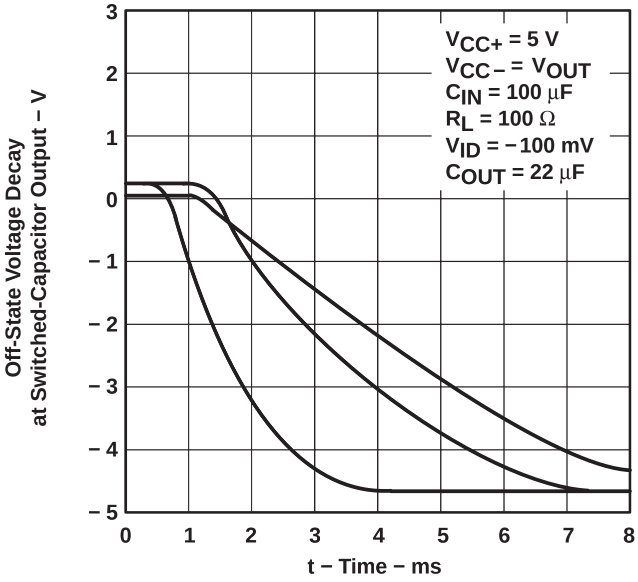


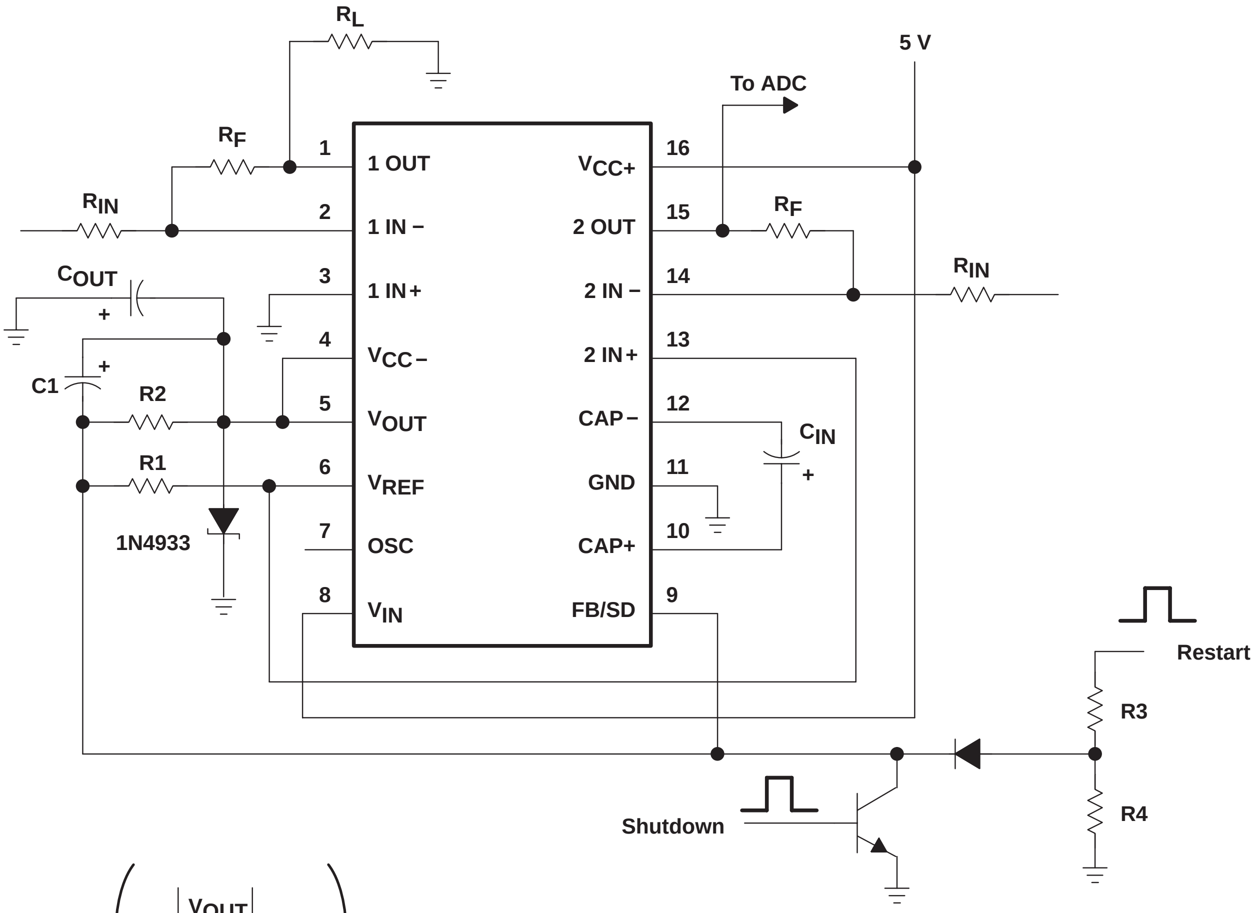
Figure 90

It is important to remember that the amplifier's negative common-mode input voltage limit (V_{ICR-}) is specified as an offset from the negative rail. Care should be taken to ensure that the input signal does not violate this limit as V_{OUT} decays. The negative output voltage swing is similarly affected by the gradual loss of the negative rail.

This application takes advantage of the otherwise unused V_{REF} output of the switched-capacitor block to bias one amplifier to 2.5 V. This is especially useful when the amplifier is followed by an ADC, keeping the signal centered in the middle of the converter's dynamic range. Other biasing methods may be necessary in precision systems.

In Figure 91, V_{REF}, R1, and R2 are used to generate a feedback voltage to the TLE2682's error amplifier. This voltage, fed into FB/SD, is used to regulate the voltage at V_{OUT}, thereby further reducing output ripple. When used this way, there is a higher voltage loss (V_{IN} − |V_{OUT}|) associated with the regulation. For example, the inverter generates an unregulated voltage of approximately −4.5 V from a positive 5-V source; it can achieve a regulated output voltage of only about −3.5 V. Though this reduces the amplifier's input and output dynamic range, both V_{ICR-} and V_{OL} still extends to below ground.

APPLICATION INFORMATION



$$R2 = R1\left(\frac{\left|V_{OUT}\right|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right)$$

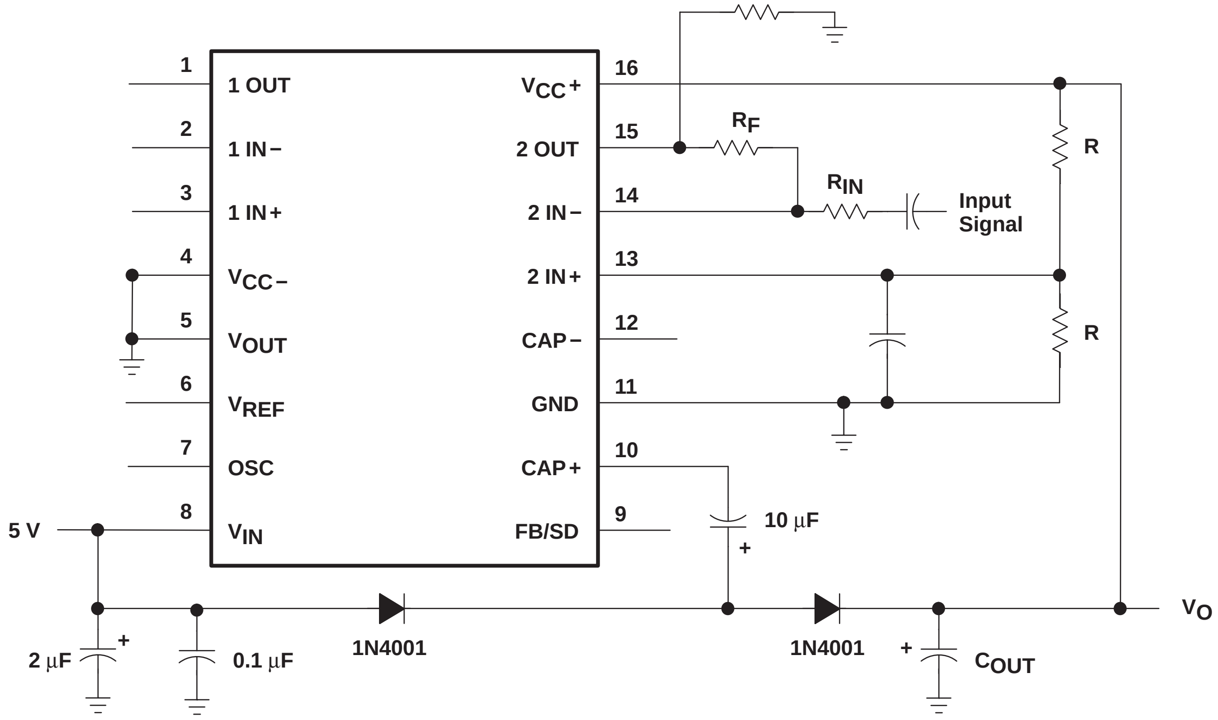
Where: V_{REF} = 2.5 V Nominal

Figure 91. Switched Capacitor Configured as Regulated Inverter

The reference voltage, though being used as part of the regulation circuitry, is still available for other uses if total current drawn from it is limited to under 60 μA. The shutdown feature remains available, though a restart pulse may be necessary to start the switched capacitor if the voltage on C_{OUT} is not fully discharged. This restart pulse is isolated from the feedback loop using a blocking diode. A more detailed discussion of this configuration can be found in the switched-capacitor section.

The TLE2682s switched-capacitor building block can also be configured as a positive doubler, extending the range of single-supply systems. This configuration is shown in Figure 92. As with the inverting configuration, noise and ripple components show up at the doubled output voltage and vary in magnitude with load. As before, filtering can be used to improve the output waveform; but unlike the voltage inverter, changing the size of C_{OUT} has little effect. Figure 93 through Figure 98 illustrate the effects of loading and filtering.

APPLICATION INFORMATION



V_{IN} = 3.5 V through 15 V
$V_O \approx 2\,V_{IN} - \left(V_L + 2\,V_{Diode}\right)$
V_L = voltage loss switched-capacitor voltage converter

Figure 92. Voltage Converter Configured as Positive Doubler

APPLICATION INFORMATION

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

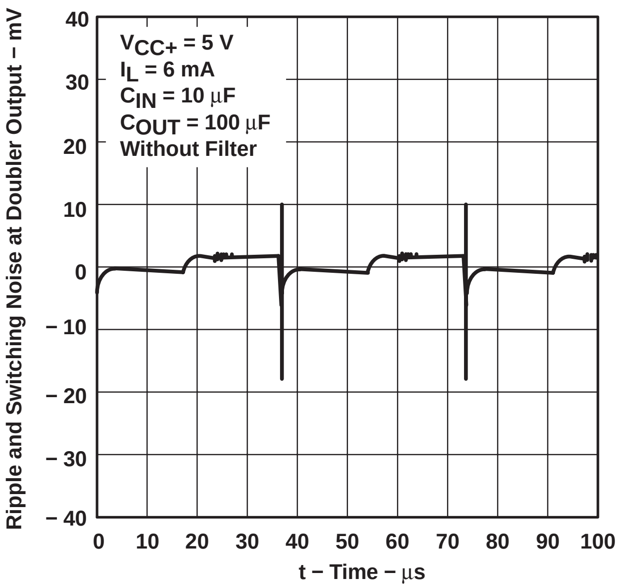


Figure 93

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

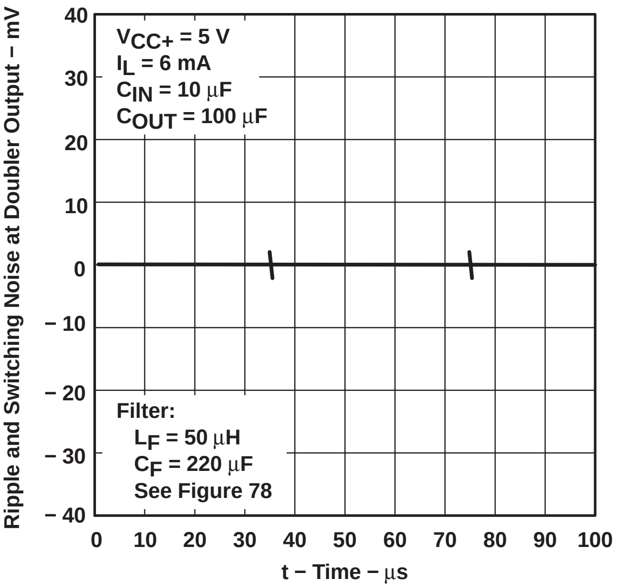


Figure 94

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

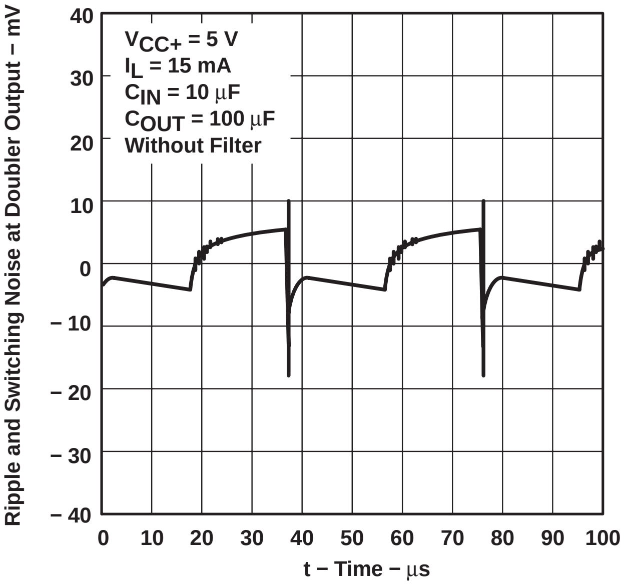


Figure 95

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

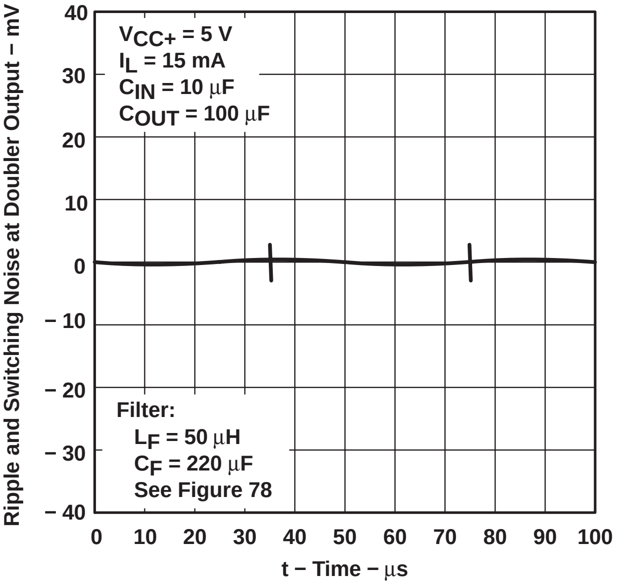


Figure 96

APPLICATION INFORMATION

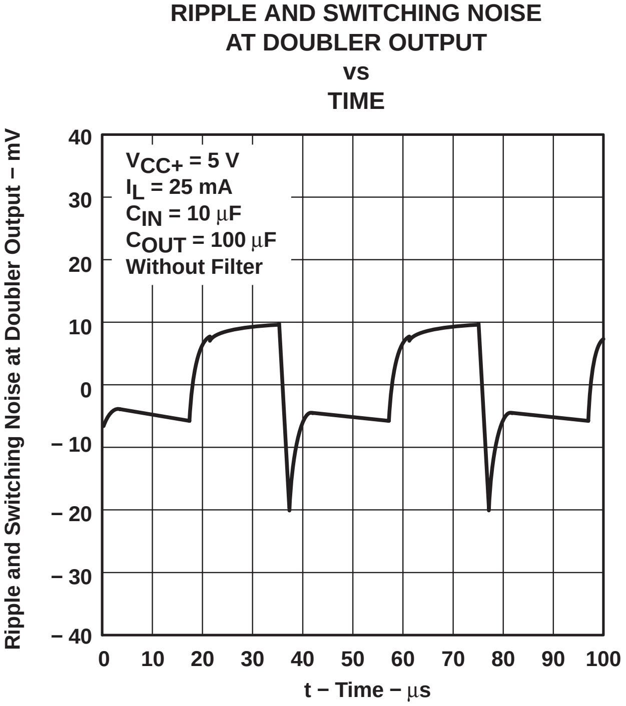


Figure 97

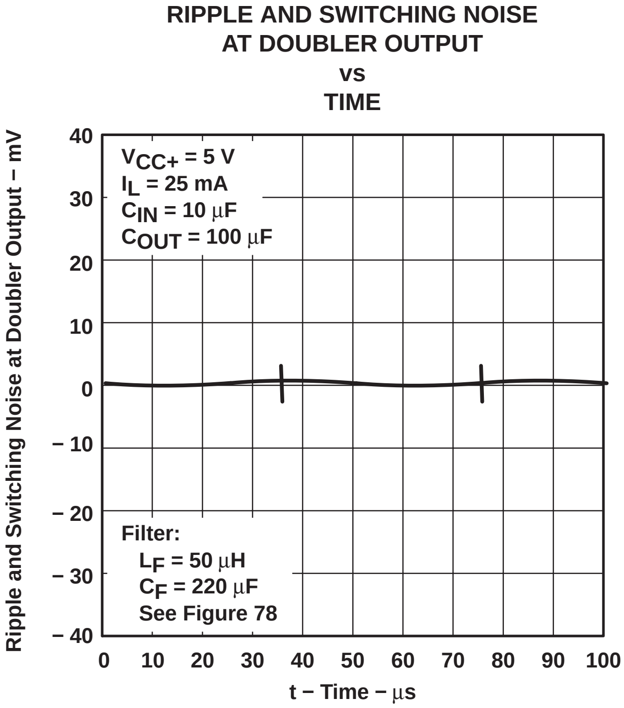


Figure 98

As with the inverter configuration, when the operational amplifiers are supplied using the voltage converter block, switching noise are coupled into the signal path through ground. Using the shutdown pin allows precision measurement of the output signal by an ADC by temporarily disabling the switching mechanism. Figure 99 and Figure 100 show the decay and charge times at the doubler output with the amplifier connected as shown.

APPLICATION INFORMATION

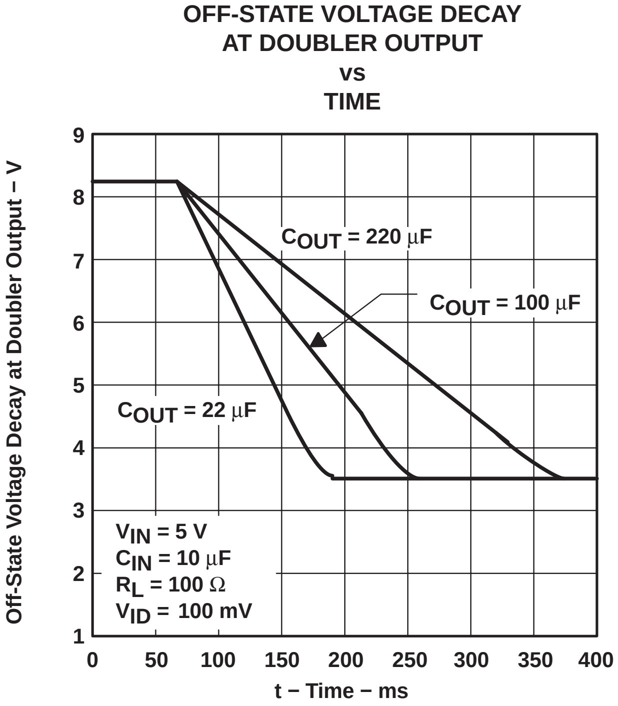


Figure 99

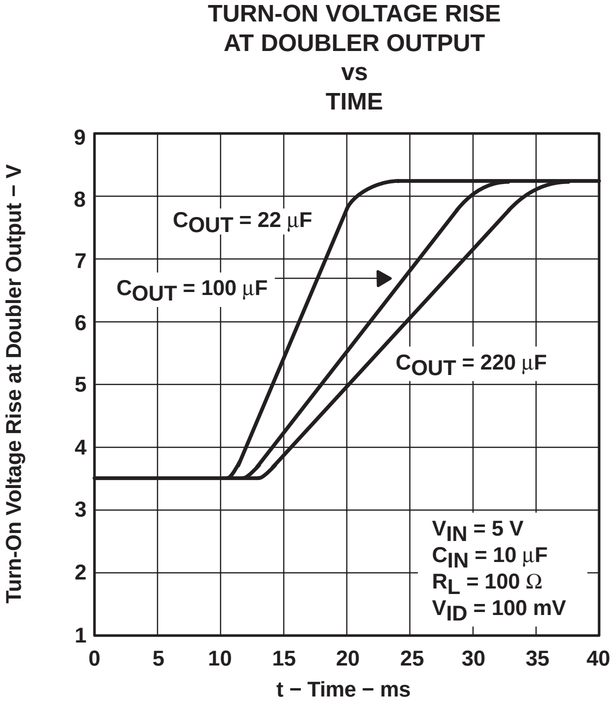


Figure 100

The circuit designer should be aware that the TLE2682 amplifier and switched-capacitor sections are tested and specified separately. Performance may differ from that shown in the Typical Characteristics section of this data sheet when they are used together. This is evident, for example, in the dependence of V_{ICR-} and V_{OL} on V_{CC-} as previously discussed. The impact of supplying the amplifier’s negative rail using the switched-capacitor block in each design should be considered and carefully evaluated.

The more esoteric features of the switched-capacitor building block, including external synchronization of the internal oscillator and power dissipation considerations, are covered in detail in the following switched-capacitor building block application information section.

APPLICATION INFORMATION

switched-capacitor section

A review of a basic switched-capacitor building block is helpful in understanding the operation of the TLE2682. When the switch shown in Figure 101 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is $q1 = C1 \times V1$. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is $q2 = C1 \times V2$. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is as shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \tag{1}$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(V1 - V2) \tag{2}$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/f \times C1)} = \frac{V1 - V2}{R_{EQUIV}} \tag{3}$$

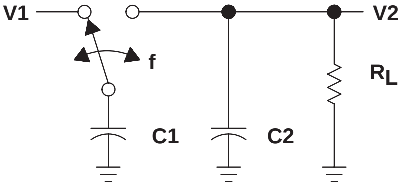


Figure 101. Switched-Capacitor Block

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div f \times C1$. The equivalent circuit for the switched-capacitor network is as shown in Figure 102. The TLE2682 has the same switching action as the basic switched-capacitor voltage converter. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 66). As oscillator frequency is decreased, the output impedance is eventually dominated by the $1/f \times C1$ term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle when multiplied by the switching frequency becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the TLE2682 switched-capacitor section is designed to run in the frequency band where voltage losses are at a minimum.

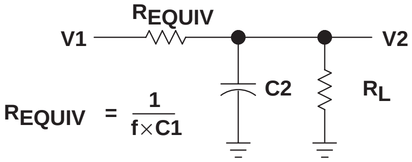


Figure 102. Switched-Capacitor Equivalent Circuit

APPLICATION INFORMATION

pin functions (see functional block diagram − converter)

Supply voltage (V_{IN}) alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the TLE2682 switched-capacitor section and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 µF, preferably tantalum or some other low-ESR type, is recommended. A larger capacitor is desirable in some cases. An example is when the actual input supply is connected to the TLE2682 through long leads or when the pulse currents drawn by the TLE2682 might affect other circuits through supply coupling.

In addition to being the output pin, V_{OUT} is tied to the substrate of the device. Special care must be taken in TLE2682 circuits to avoid making V_{OUT} positive with respect to any of the other pins. For circuits with the output load connected from V_{CC+} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external Schottky diode must be added (see Figure 103). This diode prevents V_{OUT} from being pulled above the GND during start up. A fast recovery diode such as IN4933 with low forward voltage ($V_f \approx 0.2$ V) can be used.

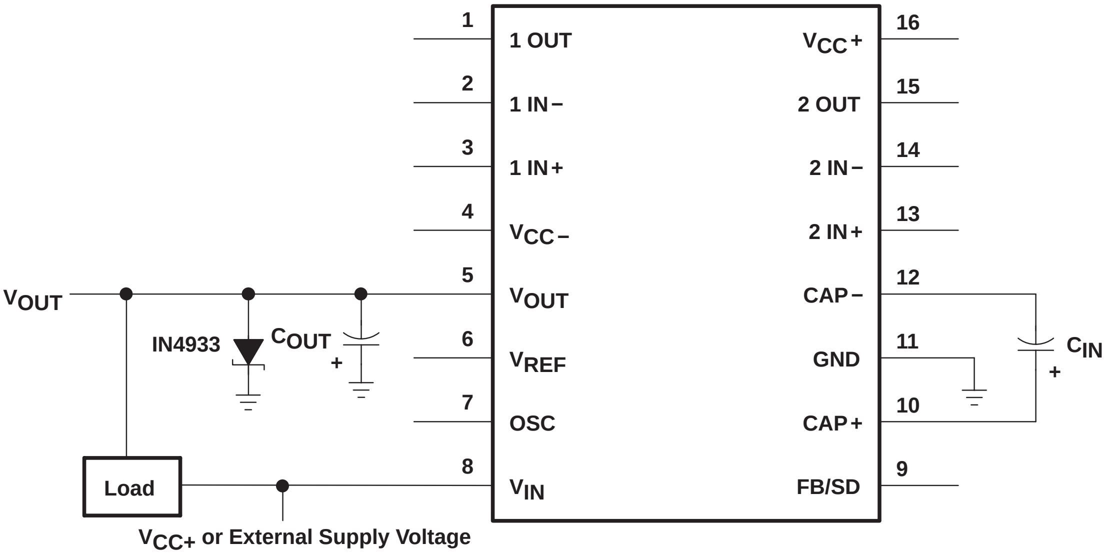


Figure 103. Circuit With Load Connected From V_{CC} to V_{OUT}

The voltage reference (V_{REF}) output provides a 2.5-V reference point for use in TLE2682-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 µA. V_{REF} draws approximately 100 µA when shorted to ground and does not affect the internal reference/regulator. This pin can also be used as a pullup for TLE2682 circuits that require synchronization.

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pin functions (continued)

CAP+ is the positive side of input capacitor C_{IN} and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP− is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP− sinks current to ground. When driven to V_{OUT}, CAP− sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional as should be expected when using bipolar switches.

OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 µA so that the duty cycle is approximately 50%. The TLE2682 switched-capacitor section oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 104) in the range of 5 pF − 20 pF from CAP+ to OSC. This capacitor couples a charge into C_t as the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{REF}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an npn transistor can then be used to drive OSC at the external clock frequency as shown in Figure 104.

The frequency can be lowered by adding an external capacitor (C1 in Figure 104) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

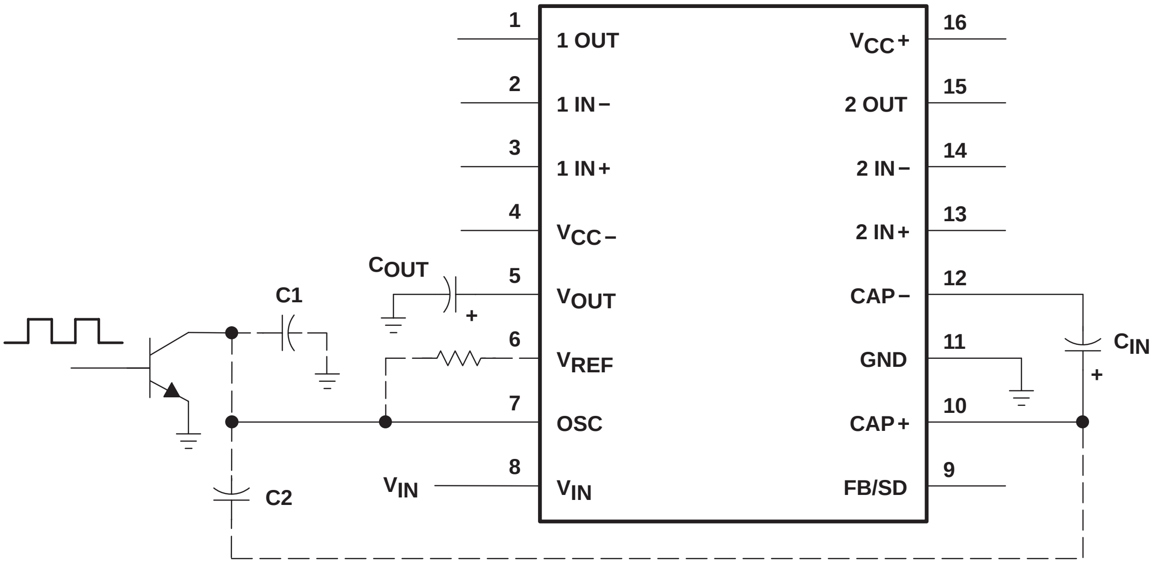

Figure 104. External Clock System

The feedback/shutdown (FB/SD) pin has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 µA. Any open-collector gate can be used to put the TLE2682 into shutdown. For normal (unregulated) operation, the device restarts when the external gate is shut off. In TLE2682 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where

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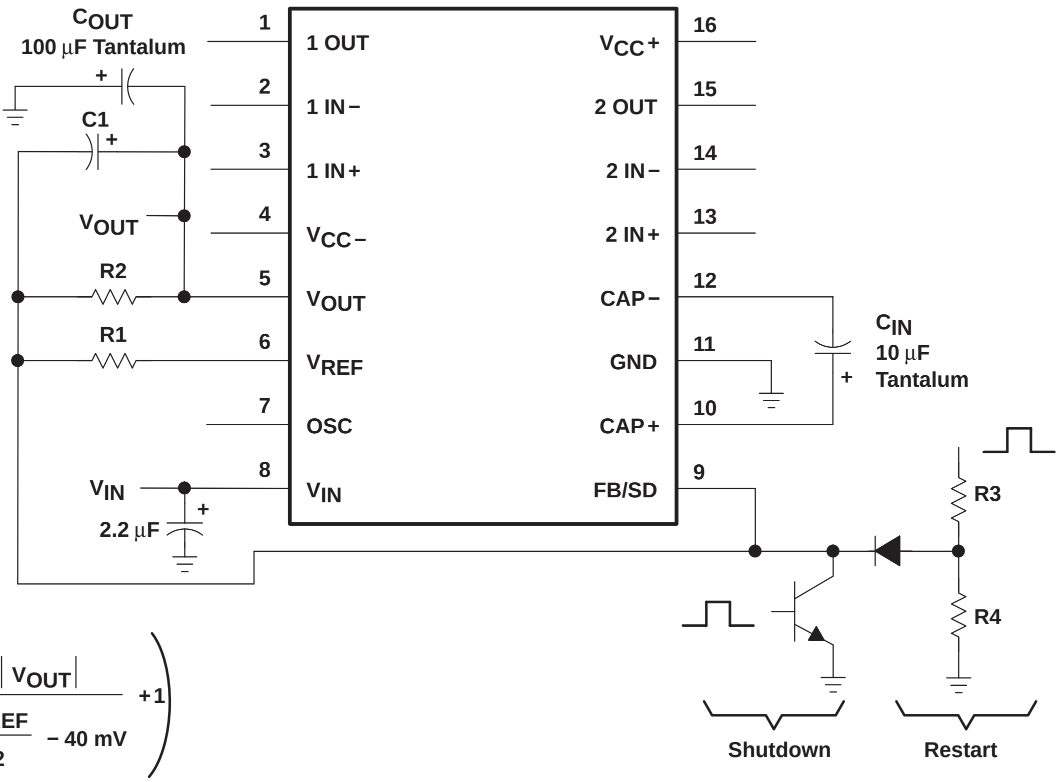
the TLE2682 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the TLE2682.

Using the circuit shown in Figure 105, the restart signal can be either a pulse ($t_p > 100\ \mu s$) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 105 should be chosen to provide a signal level at FB/SD of 0.7 V−1.1 V. FB/SD is also the inverting input of the TLE2682 switched-capacitor section error amplifier and, as such, can be used to obtain a regulated output voltage.



$$R2 = R1\left(\frac{\left|V_{OUT}\right|}{\frac{V_{REF}}{2} - 40\ \text{mV}} + 1\right)$$

Where: V_{REF} = 2.5 V Nominal

Figure 105. Basic Regulation Configuration

regulation

The error amplifier of the TLE2682 switched-capacitor section drives the npn switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the TLE2682 is used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 105 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 µA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}. For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 µF for all output voltages.

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regulation (continued)

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referenced to GND of the TLE2682 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves.

capacitor selection

While the exact values of C_{IN} and C_{OUT} are noncritical, good-quality low-ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the equivalent series resistance (ESR) of the capacitor is multiplied by four since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the switched-capacitor section by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A smaller tantalum capacitor can be connected in parallel with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown in equation 4:

$$\Delta V = \frac{I_{OUT}}{2\,f \times C_{OUT}} \qquad (4)$$

where:

ΔV = peak-to-peak ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})\ (\text{ESR of } C_{OUT}) \qquad (5)$$

power dissipation (switched-capacitor section only)

The power dissipation of any TLE2682 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components: the power loss due to voltage drops in the switches and the power loss due to drive current losses. The total power dissipated by the TLE2682 is calculated as shown in equation 6:

$$P \approx (V_{CC} - |V_{OUT}|)\ I_{OUT} + (V_{CC})\ (I_{OUT})\ (0.2) \qquad (6)$$

where both V_{CC} and V_{OUT} refer to GND. The power dissipation is equivalent to that of a linear regulator. Due to limitations of the DW package, steps must be taken to dissipate power externally for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 106. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor value is calculated as follows:

$$R_X = V_X/(4.4\ I_{OUT})$$

where:

$$V_X \approx V_{CC} - \left[(\text{TLE2682 voltage loss})\ (1.3) + |V_{OUT}|\right] \qquad (7)$$

I_{OUT} = maximum required output current

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power dissipation (continued)

The factor of 1.3 allows some operating margin for the TLE2682.

When using a 12-V to −5-V converter at 100-mA output current, calculate the power dissipation without an external resistor:

$$P = (12\text{ V} - |-5\text{ V}|)(100\text{ mA}) + (12\text{ V})(100\text{ mA})(0.2) \qquad (8)$$
$$P = 700\text{ mW} + 240\text{ mW} = 940\text{ mW}$$

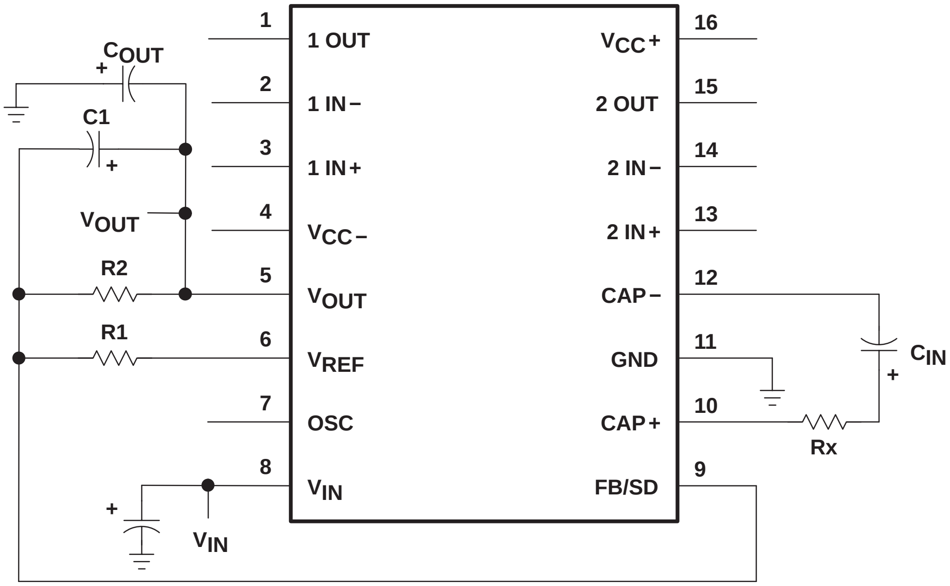

Figure 106. Power-Dissipation-Limiting Resistor in Series With C_{IN}

At θ_{JA} of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the TLE2682 in the standard regulator configuration at 100 mA output current is 1.6 V.

$$V_X = 12\text{ V} - [(1.6\text{ V})(1.3) + |-5\text{ V}|] = 4.9\text{ V} \quad \text{and} \qquad (9)$$
$$R_X = 4.9\text{ V}/(4.4)(100\text{ mA}) = 11\ \Omega$$

The resistor reduces the power dissipated by the TLE2682 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the TLE2682 is equal to (940 mW − 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the TLE2682 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the TLE2682 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the TLE2682 leads help to remove heat from the device. This is especially true for plastic packages.

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