High Speed CMOS Multilevel Pipeline Registers

QS29FCT520T
QS29FCT521T

QS29FCT2520T
QS29FCT2521T

FEATURES/BENEFITS

- Pin and function compatible to the Am29520
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in DIP, ZIP, SOIC, QSOP, HQSOP
- TTL-compatible input and output levels
- CMOS power levels: <7.5 mW static
- Undershoot clamp diodes on all inputs
- Military product compliant to MIL-STD-883

FCT-T520T/1T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- A, B, and C speed grades with 6 ns t_{PD} for C
- I_{OL} = 48 mA Com., 32 mA Mil.

FCT-T 2520T/1T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 6 ns t_{PD} for C
- I_{OL} = 12 mA Com.

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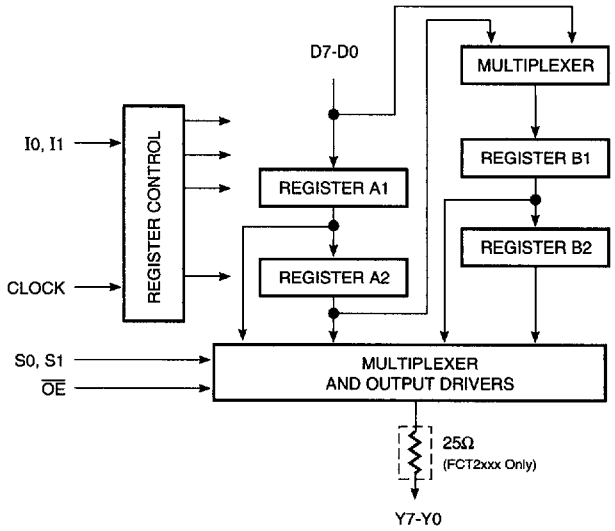
DESCRIPTION

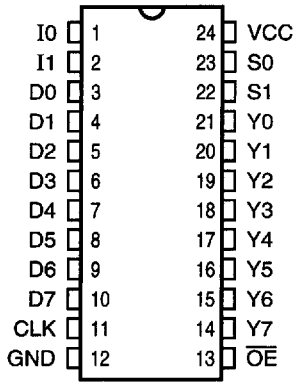
The QS29FCT520AT/BT and QS29FCT521AT/BT provide four 8-bit registers useful for temporary storage and for stage delays in pipelined systems. The four registers may be configured as a dual 2-level or single 4-level shift register pipeline. A single 8-bit input is provided, and any of the four registers may be selected for gating to the single 8-bit output. The 520 and 521 differ only in how the registers are loaded in the dual 2-rank mode, as shown in the function tables. The QS29FCT520/1 are pin and function compatible with the Am29520/1 bipolar parts, except for higher speed and significantly lower power.

FUNCTIONAL BLOCK DIAGRAM

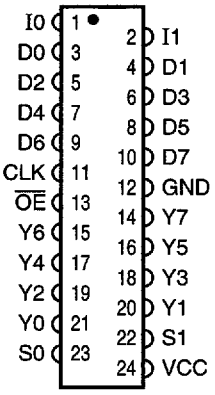


PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP

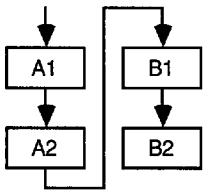
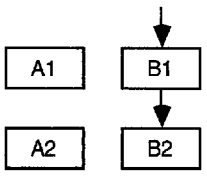
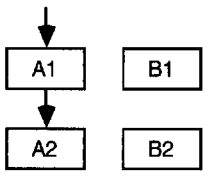
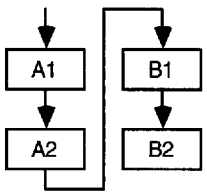
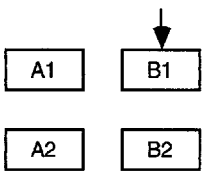
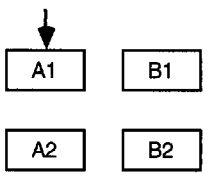


PIN DESCRIPTION

Name	I/O	Description
D7-D0	I	Data Inputs
Y7-Y0	O	Data Outputs - Three State
I0, I1	I	Register Load Control
S0, S1	I	Register Output Select
CLK	I	Clock Pulse
$\overline{OE}$	I	Output Enable

FUNCTION TABLES

REGISTER LOAD CONTROL

PART NO	Register Control Code			
	I1,0 = LL = 0	I1,0 = LH = 1	I1,0 = HL = 2	I1,0 = HH = 3
FCT520				Hold Data
FCT521				Hold Data

REGISTER OUTPUT SELECTION

S1	S0	$\overline{OE}$	Y1	Register to Y7-Y0
L	L	L	Data	B2
L	H	L	Data	B1
H	L	L	Data	A2
H	H	L	Data	A1
X	X	H	Hi-Z	Outputs Disabled

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20 mA
DC Output Diode Current with $V_{OUT} < 0$	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13, 22, 23	4	4	5	7	pF
14-21	6	6	7	9	pF
—	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Qccd	Supply Current per Input per MHz	Vcc = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., 0 ≤ V_{IN} < V_{CC}	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., 0 ≤ V_{IN} ≤ V_{CC}	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	V_{CC} = Max., V_{OUT} = GND[2,3]	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	V_{CC} = Min., V_{OUT} = 2.0V[3]	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA, T_A = 25°C[3]	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	V_{CC} = Min., I_{OL} = 32 mA (MIL) I_{OL} = 48 mA (COM)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX – 25Ω)	V_{CC} = Min., I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX – 25Ω)	V_{CC} = Min., I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		29FCT 520/1A 2520/1A Min	29FCT 520/1A 2520/1A Max	29FCT 520/1B 2520/1B Min	29FCT 520/1B 2520/1B Max	29FCT 520/1C 2520/1C Min	29FCT 520/1C 2520/1C Max	Unit
t_{CPD}	Clock to Y Delay(1)	Com	2	14	2	7.5	2	6	ns
		Mil	2	16	2	8	2	7	
t_{DY}	S0, S1 to Y Delay(1)	Com	5	13	2.5	7.5	2	6	ns
		Mil	6	15	2	8	2	7	
t_{DS}	Data to CLK Setup Time	Com	5	—	2.5	—	2.5	—	ns
		Mil	6	—	2.8	—	2.8	—	
t_{DH}	Data to CLK Hold Time	Com	2	—	2	—	2	—	ns
		Mil	2	—	2	—	2	—	
t_{IS}	I0, I1 to CLK Setup Time	Com	5	—	4	—	4	—	ns
		Mil	6	—	4.5	—	4.5	—	
t_{IH}	I0, I1 to CLK Hold Time	Com	2	—	2	—	2	—	ns
		Mil	2	—	2	—	2	—	
t_{OZ}	Output Disable Time(2)	Com	1.5	12	1.5	7	1.5	6	ns
	$\overline{OE}$ to Y	Mil	1.5	13	1.5	7.5	1.5	6	
t_{OE}	Output Enable Time(1)	Com	1.5	15	1.5	7.5	1.5	6	ns
	$\overline{OE}$ to Y	Mil	1.5	16	1.5	8	1.5	7	
t_{CW}	CLK Pulse Width,(2)	Com	7	—	5.5	—	5.5	—	ns
	HIGH or LOW	Mil	8	—	6	—	6	—	

Notes:
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.