PRELIMINARY

FullFlex™ Synchronous SDR Dual-Port SRAM

Features

- True dual-ported memory allows simultaneous access to the shared array from each port
- Synchronous pipelined operation with SDR operation on each port
  - Single Data Rate (SDR) interface at 250 MHz
  - Up to 36-Gb/s bandwidth (250 MHz * 72 bit * 2 ports)
- Selectable pipeline or flow-through mode
- Selectable 1.5V or 1.8V core power supply
- Commercial and Industrial temperature
- IEEE 1149.1 JTAG boundary scan
- Available in 484-ball PBGA Packages and 256-ball FBGA packages
- FullFlex72 family
  - 36-Mbit: 512K x 72 (CYD36S72V18)
  - 18-Mbit: 256K x 72 (CYD18S72V18)
  - 9-Mbit: 128K x 72 (CYD09S72V18)
  - 4-Mbit: 64K x 72 (CYD04S72V18)
- FullFlex36 family
  - 36-Mbit: 1M x 36 (CYD36S36V18)
  - 18-Mbit: 512K x 36 (CYD18S36V18)
  - 9-Mbit: 256K x 36 (CYD09S36V18)
  - 4-Mbit: 128K x 36 (CYD04S36V18)
- FullFlex18 family
  - 36-Mbit: 2M x 18 (CYD36S18V18)
  - 18-Mbit: 1M x 18 (CYD18S18V18)
  - 9-Mbit: 512K x 18 (CYD09S18V18)
  - 4-Mbit: 256K x 18 (CYD04S18V18)
- Built-in deterministic access control to manage address collisions
  - Deterministic flag output upon collision detection
  - Collision detection on back-to-back clock cycles
  - First Busy Address readback
- Advanced features for improved high-speed data transfer and flexibility
  - Variable Impedance Matching (VIM)
  - Echo clocks
  - Selectable LVTTL (3.3V), Extended HSTL (1.4V–1.9V), 1.8V LVCMOS, or 2.5V LVCMOS I/O on each port
  - Burst counters for sequential memory access
  - Mailbox with interrupt flags for message passing
  - Dual Chip Enables for easy depth expansion

Functional Description

The FullFlex™ Dual-Port SRAM families consist of 4-Mbit, 9-Mbit, 18-Mbit, and 36-Mbit synchronous, true dual-port static RAMs that are high-speed, low-power 1.8V/1.5V CMOS. Two ports are provided, allowing the array to be accessed simultaneously. Simultaneous access to a location triggers deterministic access control. For FullFlex72 these ports can operate independently with 72-bit bus widths and each port can be independently configured for two pipeline stages. Each port can also be configured to operate in pipeline or flow-through mode.

Advanced features include built-in deterministic access control to manage address collisions during simultaneous access to the same memory location, variable impedance matching (VIM) to improve data transmission by matching the output driver impedance to the line impedance, and echo clocks to improve data transfer.

To reduce the static power consumption, chip enables can be used to power down the internal circuitry. The number of cycles of latency before a change in $\overline{CE0}$ or CE1 will enable or disable the databus matches the number of cycles of read latency selected for the device. In order for a valid write or read to occur, both chip enable inputs on a port must be active.

Each port contains an optional burst counter on the input address register. After externally loading the counter with the initial address, the counter will increment the address internally.

Additional features of this device include a mask register and a mirror register to control counter increments and wrap-around, counter-interrupt ($\overline{CNTINT}$) flags to notify that the counter will reach the maximum value on the next clock cycle, readback of the burst-counter internal address, mask register address, and BUSY address on the address lines, retransmit functionality, mailbox interrupt flags for message passing, JTAG for boundary scan, and asynchronous Master Reset ($\overline{MRST}$). The logic block diagram in *Figure 1* displays these features.

The FullFlex72 is offered in a 484-ball plastic BGA package. The FullFlex36 and FullFlex18 are offered in a 256-ball fine pitch BGA package.

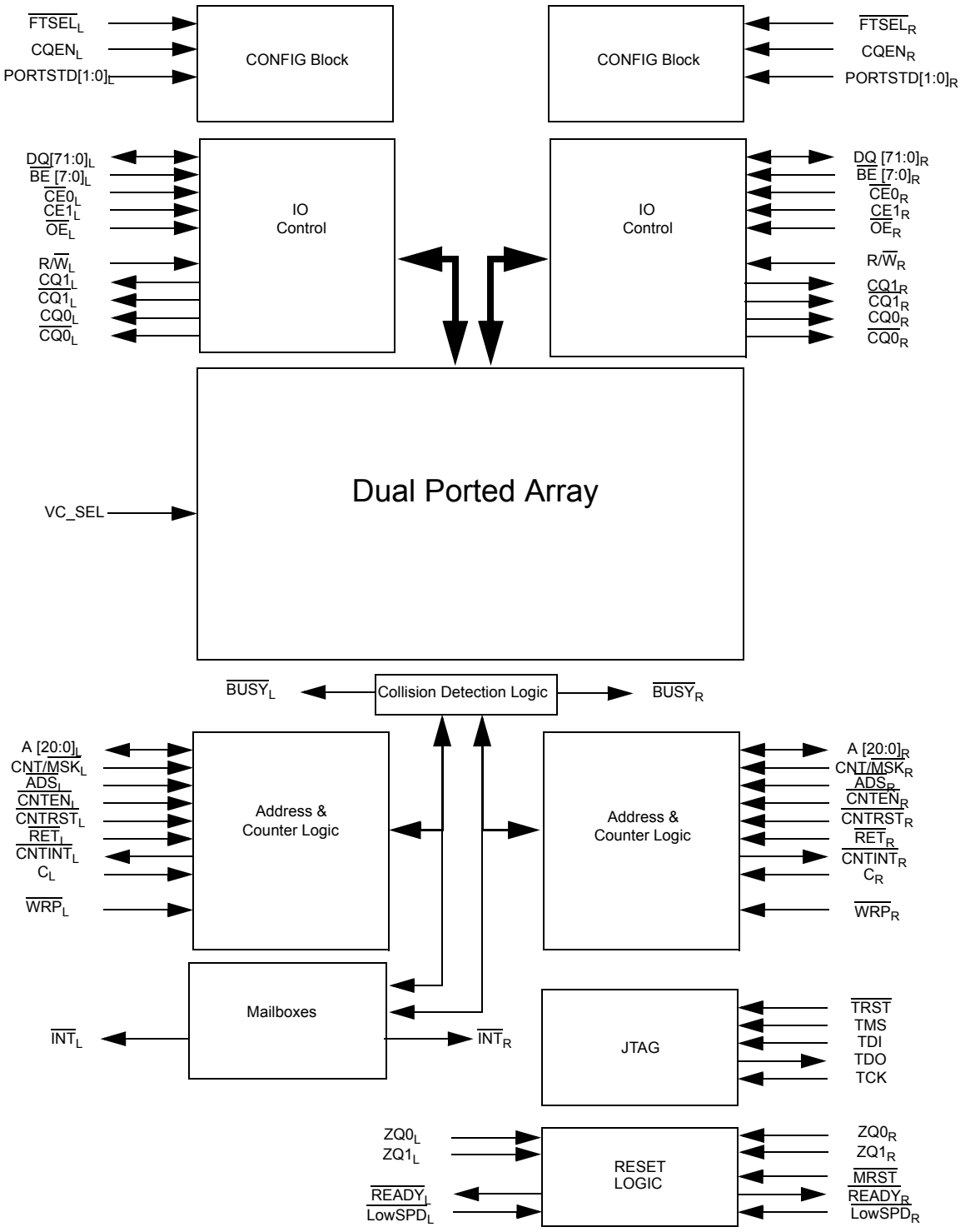


Figure 1. FullFlex72 18-Mbit (CYD18S72V18) Block Diagram[1, 2, 3]

Notes:
1. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and the CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and the CYD09S18V18 devices have 19 address bits. The CYD18S72V18, CYD09S36V18, and the CYD04S18V18 devices have 18 address bits. The CYD09S72V18 and the CYD04S36V18 devices have 17 address bits. The CYD04S72V18 has 16 address bits.
2. The FullFlex72 family of devices has 72 data lines. The FullFlex36 family of devices has 36 data lines. The FullFlex18 family of devices has 18 data lines.
3. The FullFlex72 family of devices has eight byte enables. The FullFlex36 family of devices has four byte enables. The FullFlex18 family of devices has two byte enables.

FullFlex72 SDR 484-ball BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	NC	DQ61L	DQ59L	DQ57L	DQ54L	DQ51L	DQ48L	DQ45L	DQ42L	DQ39L	DQ36L	DQ36R	DQ39R	DQ42R	DQ45R	DQ48R	DQ51R	DQ54R	DQ57R	DQ59R	DQ61R	NC
B	DQ63L	DQ62L	DQ60L	DQ58L	DQ55L	DQ52L	DQ49L	DQ46L	DQ43L	DQ40L	DQ37L	DQ37R	DQ40R	DQ43R	DQ46R	DQ49R	DQ52R	DQ55R	DQ58R	DQ60R	DQ62R	DQ63R
C	DQ65L	DQ64L	VSS	VSS	DQ56L	DQ53L	DQ50L	DQ47L	DQ44L	DQ41L	DQ38L	DQ38R	DQ41R	DQ44R	DQ47R	DQ50R	DQ53R	DQ56R	VSS	VSS	DQ64R	DQ65R
D	DQ67L	DQ66L	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	VSS	$\overline{LOW}$/SPDL	PORTSTD0L	ZQ0L[4]	$\overline{BUSY}$L	$\overline{CNTI}$NTL	PORTSTD1L	NC	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	DQ66R	DQ67R
E	DQ69L	DQ68L	VDDIOL	VSS	VSS	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	NC	VSS	VDDIOR	DQ68R	DQ69R
F	DQ71L	DQ70L	CE1L	$\overline{CE0L}$	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{CE0R}$	CE1R	DQ70R	DQ71R
G	A0L	A1L	$\overline{RETL}$	$\overline{BE4L}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{BE4R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRP}$L	$\overline{BE5L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE5R}$	$\overline{WRP}$R	A3R	A2R
J	A4L	A5L	$\overline{READ}$YL	$\overline{BE6L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE6R}$	$\overline{READ}$YR	A5R	A4R
K	A6L	A7L	ZQ1L[4]	$\overline{BE7L}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	$\overline{BE7R}$	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	VSS	$\overline{BE3L}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{BE3R}$	VSS	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	$\overline{BE2L}$	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{BE2R}$	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	$\overline{CNT}$MSKL	$\overline{BE1L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE1R}$	$\overline{CNT}$MSKR	A15R	A14R
R	A16L[7]	A17L[6]	$\overline{CNTE}$NL	$\overline{BE0L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE0R}$	$\overline{CNTE}$NR	A17R[6]	A16R[7]
T	A18L[5]	NC	$\overline{CNTR}$STL	$\overline{INTL}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{INTR}$	$\overline{CNTR}$STR	NC	A18R[5]
U	DQ35L	DQ34L	R/$\overline{WL}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{WR}$	DQ34R	DQ35R
V	DQ33L	DQ32L	$\overline{FTSE}$LL	VDDIOL	NC	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{TRST}$	VDDIOR	$\overline{FTSE}$LR	DQ32R	DQ33R
W	DQ31L	DQ30L	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	VC_SEL	PORTSTD1R	$\overline{CNTI}$NTR	$\overline{BUSY}$R	ZQ0R[4]	PORTSTD0R	$\overline{LOW}$/SPDR	VSS	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	DQ30R	DQ31R
Y	DQ29L	DQ28L	VSS	VSS	DQ20L	DQ17L	DQ14L	DQ11L	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DQ11R	DQ14R	DQ17R	DQ20R	TMS	TCK	DQ28R	DQ29R
AA	DQ27L	DQ26L	DQ24L	DQ22L	DQ19L	DQ16L	DQ13L	DQ10L	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DQ10R	DQ13R	DQ16R	DQ19R	DQ22R	DQ24R	DQ26R	DQ27R
AB	NC	DQ25L	DQ23L	DQ21L	DQ18L	DQ15L	DQ12L	DQ9L	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DQ9R	DQ12R	DQ15R	DQ18R	DQ21R	DQ23R	DQ25R	NC

Notes:
4. Leaving this pin NC disables VIM
5. Leave this ball unconnected for CYD18S72V18, CYD09S72V18 and CYD04S72V18.
6. Leave this ball unconnected for CYD09S72V18 and CYD04S72V18
7. Leave this ball unconnected for CYD04S72V18

FullFlex36 SDR 484-ball BGA Pinout (Top View)[8]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	NC	NC	NC	NC	NC	DQ33L	DQ30L	DQ27L	DQ24L	DQ21L	DQ18L	DQ18R	DQ21R	DQ24R	DQ27R	DQ30R	DQ33R	NC	NC	NC	NC	NC
B	NC	NC	NC	NC	NC	DQ34L	DQ31L	DQ28L	DQ25L	DQ22L	DQ19L	DQ19R	DQ22R	DQ25R	DQ28R	DQ31R	DQ34R	NC	NC	NC	NC	NC
C	NC	NC	VSS	VSS	NC	DQ35L	DQ32L	DQ29L	DQ26L	DQ23L	DQ20L	DQ20R	DQ23R	DQ26R	DQ29R	DQ32R	DQ35R	NC	VSS	VSS	NC	NC
D	NC	NC	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	VSS	$\overline{LOW}$/SPDL	PORTSTD0L	ZQ0L[4]	$\overline{BUSY}$L	$\overline{CNTI}$NTL	PORTSTD1L	NC	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	NC	NC
E	NC	NC	VDDIOL	VSS	VSS	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	NC	VSS	VDDIOR	NC	NC
F	NC	NC	CE1L	$\overline{CE0L}$	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{CE0R}$	CE1R	NC	NC
G	A0L	A1L	$\overline{RETL}$	$\overline{BE2L}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{BE2R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRPL}$	$\overline{BE3L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE3R}$	$\overline{WRPR}$	A3R	A2R
J	A4L	A5L	$\overline{READYL}$	NC	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	NC	$\overline{READYR}$	A5R	A4R
K	A6L	A7L	ZQ1L[4]	NC	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	NC	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	VSS	NC	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	NC	VSS	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	NC	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	NC	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	$\overline{CNTMSKL}$	$\overline{BE1L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE1R}$	$\overline{CNTMSKR}$	A15R	A14R
R	A16L	A17L	$\overline{CNTENL}$	$\overline{BE0L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE0R}$	$\overline{CNTENR}$	A17R	A16R
T	A18L	A19L	$\overline{CNTRSTL}$	$\overline{INTL}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{INTR}$	$\overline{CNTRSTR}$	A19R	A18R
U	NC	NC	R/$\overline{WL}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{WR}$	NC	NC
V	NC	NC	$\overline{FTSELL}$	VDDIOL	NC	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{TRST}$	VDDIOR	$\overline{FTSELR}$	NC	NC
W	NC	NC	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	VC_SEL	PORTSTD1R	$\overline{CNTINTR}$	$\overline{BUSY}$R	ZQ0R[4]	PORTSTD0R	$\overline{LOW}$/SPDR	VSS	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	NC	NC
Y	NC	NC	VSS	VSS	NC	DQ17L	DQ14L	DQ11L	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	DQ11R	DQ14R	DQ17R	NC	TMS	TCK	NC	NC
AA	NC	NC	NC	NC	NC	DQ16L	DQ13L	DQ10L	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	DQ10R	DQ13R	DQ16R	NC	NC	NC	NC	NC
AB	NC	NC	NC	NC	NC	DQ15L	DQ12L	DQ9L	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	DQ9R	DQ12R	DQ15R	NC	NC	NC	NC	NC

Note:
8. Use this pinout only for device CYD36S36V18 of the FullFlex36 famiy.

FullFlex18 SDR 484-ball BGA Pinout (Top View)[9]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	NC	NC	NC	NC	NC	NC	NC	NC	DQ15L	DQ12L	DQ9L	DQ9R	DQ12R	DQ15R	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	NC	NC	NC	NC	NC	DQ16L	DQ13L	DQ10L	DQ10R	DQ13R	DQ16R	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	NC	VSS	VSS	NC	NC	NC	NC	DQ17L	DQ14L	DQ11L	DQ11R	DQ14R	DQ17R	NC	NC	NC	NC	VSS	VSS	NC	NC
D	NC	NC	VSS	VSS	VSS	$\overline{CQ1L}$	CQ1L	VSS	$\overline{LOW}$/SPDL	PORTSTD0L	ZQ0L[4]	$\overline{BUSY}$L	$\overline{CNTI}$NTL	PORTSTD1L	NC	CQ1R	$\overline{CQ1R}$	VSS	VSS	VSS	NC	NC
E	NC	NC	VDDIOL	VSS	VSS	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	NC	VSS	VDDIOR	NC	NC
F	NC	NC	CE1L	$\overline{CE0L}$	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{CE0R}$	CE1R	NC	NC
G	A0L	A1L	$\overline{RETL}$	$\overline{BE1L}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{BE1R}$	$\overline{RETR}$	A1R	A0R
H	A2L	A3L	$\overline{WRP}$L	NC	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	NC	$\overline{WRP}$R	A3R	A2R
J	A4L	A5L	$\overline{READ}$YL	NC	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	NC	$\overline{READ}$YR	A5R	A4R
K	A6L	A7L	ZQ1L[4]	NC	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VDDIOR	NC	ZQ1R[4]	A7R	A6R
L	A8L	A9L	CL	$\overline{OEL}$	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	$\overline{OER}$	CR	A9R	A8R
M	A10L	A11L	VSS	NC	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	NC	VSS	A11R	A10R
N	A12L	A13L	$\overline{ADSL}$	NC	VDDIOL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	NC	$\overline{ADSR}$	A13R	A12R
P	A14L	A15L	$\overline{CNT}$MSKL	NC	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	NC	$\overline{CNT}$MSKR	A15R	A14R
R	A16L	A17L	$\overline{CNTE}$NL	$\overline{BE0L}$	VDDIOL	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	VDDIOR	$\overline{BE0R}$	$\overline{CNTE}$NR	A17R	A16R
T	A18L	A19L	$\overline{CNTR}$STL	$\overline{INTL}$	VDDIOL	VDDIOL	VREFL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VREFR	VDDIOR	VDDIOR	$\overline{INTR}$	$\overline{CNTR}$STR	A19R	A18R
U	A20L	NC	R/$\overline{WL}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{WR}$	NC	A20R
V	NC	NC	$\overline{FTSE}$LL	VDDIOL	NC	VDDIOL	VDDIOL	VDDIOL	VDDIOL	VTTL	VTTL	VTTL	VDDIOR	VDDIOR	VDDIOR	VDDIOR	VDDIOR	$\overline{TRST}$	VDDIOR	$\overline{FTSE}$LR	NC	NC
W	NC	NC	VSS	$\overline{MRST}$	VSS	$\overline{CQ0L}$	CQ0L	VC_SEL	PORTSTD1R	$\overline{CNTI}$NTR	$\overline{BUSY}$R	ZQ0R[4]	PORTSTD0R	$\overline{LOW}$/SPDR	VSS	CQ0R	$\overline{CQ0R}$	VSS	TDI	TDO	NC	NC
Y	NC	NC	VSS	VSS	NC	NC	NC	NC	DQ8L	DQ5L	DQ2L	DQ2R	DQ5R	DQ8R	NC	NC	NC	NC	TMS	TCK	NC	NC
AA	NC	NC	NC	NC	NC	NC	NC	NC	DQ7L	DQ4L	DQ1L	DQ1R	DQ4R	DQ7R	NC	NC	NC	NC	NC	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	DQ6L	DQ3L	DQ0L	DQ0R	DQ3R	DQ6R	NC	NC	NC	NC	NC	NC	NC	NC

Note:
9. Use this pinout only for device CYD36S18V18 of the FullFlex18 famiy.

FullFlex36 SDR 256-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DQ32L	DQ30L	DQ28L	DQ26L	DQ24L	DQ22L	DQ20L	DQ18L	DQ18R	DQ20R	DQ22R	DQ24R	DQ26R	DQ28R	DQ30R	DQ32R
B	DQ33L	DQ31L	DQ29L	DQ27L	DQ25L	DQ23L	DQ21L	DQ19L	DQ19R	DQ21R	DQ23R	DQ25R	DQ27R	DQ29R	DQ31R	DQ33R
C	DQ34L	DQ35L	$\overline{\text{RETL}}$	$\overline{\text{INTL}}$	CQ1L	$\overline{\text{CQ1L}}$	VC_SEL	$\overline{\text{TRST}}$	$\overline{\text{MRST}}$	ZQ0R[4]	$\overline{\text{CQ1R}}$	CQ1R	$\overline{\text{INTR}}$	$\overline{\text{RETR}}$	DQ35R	DQ34R
D	A0L	A1L	$\overline{\text{WRPL}}$	VREF	$\overline{\text{FTSELL}}$	$\overline{\text{LOWSPDL}}$	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPDR}}$	$\overline{\text{FTSELR}}$	VREF	$\overline{\text{WRPR}}$	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0L}}$	CE1L	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R	$\overline{\text{CE0R}}$	A3R	A2R
F	A4L	A5L	$\overline{\text{CNINTL}}$	$\overline{\text{BE3L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE3R}}$	$\overline{\text{CNINTR}}$	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSYL}}$	$\overline{\text{BE2L}}$	ZQ0L[4]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE2R}}$	$\overline{\text{BUSYR}}$	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	VSS	PORTSTD1L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R	VSS	A11R	A10R
K	A12L	A13L	$\overline{\text{OEL}}$	$\overline{\text{BE1L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1R}}$	$\overline{\text{OER}}$	A13R	A12R
L	A14L	A15L	$\overline{\text{ADSL}}$	$\overline{\text{BE0L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{ADSR}}$	A15R	A14R
M	A16L	A17L[11]	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	A17R[11]	A16R
N	A18L[10]	NC	$\overline{\text{CNTMSKL}}$	VREF	PORTSTD0L	$\overline{\text{READYL}}$	ZQ1L[4]	VTTL	VTTL	ZQ1R[4]	$\overline{\text{READYR}}$	PORTSTD0R	VREF	$\overline{\text{CNTMSKR}}$	NC	A18R[10]
P	DQ16L	DQ17L	$\overline{\text{CNTENL}}$	$\overline{\text{CNTRSTL}}$	CQ0L	$\overline{\text{CQ0L}}$	TCK	TMS	TDO	TDI	$\overline{\text{CQ0R}}$	CQ0R	$\overline{\text{CNTRSTR}}$	$\overline{\text{CNTENR}}$	DQ17R	DQ16R
R	DQ15L	DQ13L	DQ11L	DQ9L	DQ7L	DQ5L	DQ3L	DQ1L	DQ1R	DQ3R	DQ5R	DQ7R	DQ9R	DQ11R	DQ13R	DQ15R
T	DQ14L	DQ12L	DQ10L	DQ8L	DQ6L	DQ4L	DQ2L	DQ0L	DQ0R	DQ2R	DQ4R	DQ6R	DQ8R	DQ10R	DQ12R	DQ14R

Notes:
10. Leave this ball unconnected for CYD09S36V18 and CYD04S36V18.
11. Leave this ball unconnected for CYD04S36V18.

FullFlex18 SDR 256-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	DQ17L	DQ16L	DQ13L	DQ12L	DQ9L	DQ9R	DQ12R	DQ13R	DQ16R	DQ17R	NC	NC	NC
B	NC	NC	NC	NC	DQ15L	DQ14L	DQ11L	DQ10L	DQ10R	DQ11R	DQ14R	DQ15R	NC	NC	NC	NC
C	NC	NC	$\overline{\text{RETL}}$	$\overline{\text{INTL}}$	CQ1L	$\overline{\text{CQ1L}}$	VC_SEL	$\overline{\text{TRST}}$	$\overline{\text{MRST}}$	ZQ0R[4]	$\overline{\text{CQ1R}}$	CQ1R	$\overline{\text{INTR}}$	$\overline{\text{RETR}}$	NC	NC
D	A0L	A1L	$\overline{\text{WRPL}}$	VREF	$\overline{\text{FTSELL}}$	$\overline{\text{LOWSPDL}}$	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPDR}}$	$\overline{\text{FTSELR}}$	VREF	$\overline{\text{WRPR}}$	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0L}}$	CE1L	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R	$\overline{\text{CE0R}}$	A3R	A2R
F	A4L	A5L	$\overline{\text{CNINTL}}$	NC	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	NC	$\overline{\text{CNINTR}}$	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSYL}}$	NC	ZQ0L[4]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	NC	$\overline{\text{BUSYR}}$	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	VSS	PORTSTD1L	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R	VSS	A11R	A10R
K	A12L	A13L	$\overline{\text{OEL}}$	$\overline{\text{BE1L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1R}}$	$\overline{\text{OER}}$	A13R	A12R
L	A14L	A15L	$\overline{\text{ADSL}}$	$\overline{\text{BE0L}}$	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE0R}}$	$\overline{\text{ADSR}}$	A15R	A14R
M	A16L	A17L	R/$\overline{\text{WL}}$	CQENL	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CQENR	R/$\overline{\text{WR}}$	A17R	A16R
N	A18L[13]	A19L[12]	$\overline{\text{CNTMSKL}}$	VREF	PORTSTD0L	$\overline{\text{READYL}}$	ZQ1L[4]	VTTL	VTTL	ZQ1R[4]	$\overline{\text{READYR}}$	PORTSTD0R	VREF	$\overline{\text{CNTMSKR}}$	A19R[12]	A18R[13]
P	NC	NC	CNTENL	CNTRSTL	CQ0L	$\overline{\text{CQ0L}}$	TCK	TMS	TDO	TDI	$\overline{\text{CQ0R}}$	CQ0R	$\overline{\text{CNTRSTR}}$	$\overline{\text{CNTENR}}$	NC	NC
R	NC	NC	NC	NC	DQ6L	DQ5L	DQ2L	DQ1L	DQ1R	DQ2R	DQ5R	DQ6R	NC	NC	NC	NC
T	NC	NC	NC	DQ8L	DQ7L	DQ4L	DQ3L	DQ0L	DQ0R	DQ3R	DQ4R	DQ7R	DQ8R	NC	NC	NC

Notes:
12. Leave this ball unconnected for CYD09S18V18 and CYD04S18V18.
13. Leave this ball unconnected for CYD04S18V18.

Table 1. Selection Guide

	-250[14, 15]	-200[14]	-167[14]	-133[14]	Unit
f_{MAX}	250	200	167	133	MHz
Max. Access Time (Clock to Data)	2.64	3.3	4.0	4.5	ns
Typical Operating Current I_{CC}	TBD	TBD	TBD	TBD	mA
Typical Standby Current for I_{SB3} (Both Ports CMOS Level)	TBD	TBD	TBD	TBD	mA

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{20L}	A_{0R}–A_{20R}	**Address Inputs**.[1]
DQ_{0L}–DQ_{71L}	DQ_{0R}–DQ_{71R}	**Data Bus Input/Output**.[2]
$\overline{BE}_{0L}$–$\overline{BE}_{7L}$	$\overline{BE}_{0R}$–$\overline{BE}_{7R}$	**Byte Select Inputs**.[3] Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	**Port Busy Output**. When there is an address match and both chip enables are active for both ports, an external BUSY signal is asserted on the fifth clock cycles from when the collision occurs.
C_L	C_R	**Clock Signal**. Maximum clock input rate is f_{MAX}.
$\overline{CE0}_L$	$\overline{CE0}_R$	**Active LOW Chip Enable Input**.
$CE1_L$	$CE1_R$	**Active HIGH Chip Enable Input**.
$CQEN_L$	$CQEN_R$	**Echo Clock Enable Input**. Assert HIGH to enable echo clocking on respective port.
$CQ0_L$	$CQ0_R$	**Echo Clock Signal Output for DQ[35:0] for FullFlex72 devices**. Echo Clock Signal Output for DQ[17:0] for FullFlex36 devices. Echo Clock Signal Output for DQ[8:0] for FullFlex18 devices.
$\overline{CQ0}_L$	$\overline{CQ0}_R$	**Inverted Echo Clock Signal Output for DQ[35:0] for FullFlex72 devices**. Inverted Echo Clock Signal Output for DQ[17:0] for FullFlex36 devices. Inverted Echo Clock Signal Output for DQ[8:0] for FullFlex18 devices.
$CQ1_L$	$CQ1_R$	**Echo Clock Signal Output for DQ[71:36] for FullFlex72 devices**. Echo Clock Signal Output for DQ[35:18] for FullFlex36 devices. Echo Clock Signal Output for DQ[17:9] for FullFlex18 devices.
$\overline{CQ1}_L$	$\overline{CQ1}_R$	**Inverted Echo Clock Signal Output for DQ[71:36] for FullFlex72 devices**. Inverted Echo Clock Signal Output for DQ[35:18] for FullFlex36 devices. Inverted Echo Clock Signal Output for DQ[17:9] forFullFlex18 devices.
$ZQ[1:0]_L$[16]	$ZQ[1:0]_R$[16]	**VIM Output Impedance Matching Input**. To use, connect a calibrating resistor between ZQ and ground. The resistor must be five times larger than the intended line impedance driven by the dual-port. Assert HIGH to disable Variable Impedance Matching.
$\overline{OE}_L$	$\overline{OE}_R$	**Output Enable Input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INT}_L$	$\overline{INT}_R$	**Mailbox Interrupt Flag Output**. The mailbox permits communications between ports. The upper two memory locations can be used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$\overline{LowSPD}_L$	$\overline{LowSPD}_R$	**Port Low Speed Select Input**. Assert this pin LOW to disable the DLL. For operation at less than 100 MHz, assert this pin LOW.
$PORTSTD[1:0]_L$[17]	$PORTSTD[1:0]_R$[17]	**Port Clock/Address/Control/Data/Echo Clock/ I/O Standard Select Input**. Assert these pins LOW/LOW for LVTTL, LOW/HIGH for HSTL, HIGH/LOW for 2.5V LVCMOS, and HIGH/HIGH for 1.8V LVCMOS, respectively. Connect these pins to a VTTL supply.
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write Enable Input**. Assert this pin LOW to Write to, or HIGH to Read from the dual-port memory array.

Notes:
14. SDR mode with two pipeline stages.
15. 250 MHz for HSTL and 1.8V LVCMOS I/O standards only
16. Leaving pins K3, K20 of the 484-ball BGA package and pin C10 of the 256-ball BGA package disables VIM.
17. For FullFlex72, pins D14 and W9 have an internal pull-down resistor.

Pin Definitions (continued)

Left Port	Right Port	Description
$\overline{READY}_L$	$\overline{READY}_R$	**Port DLL Ready Output**. This signal will be asserted LOW when the DLL and Variable Impedance Matching circuits have completed calibration. This is a wired OR capable output.
CNT/$\overline{MSK}_L$	CNT/$\overline{MSK}_R$	**Port Counter/Mask Select Input**. Counter control input.
$\overline{ADS}_L$	$\overline{ADS}_R$	**Port Counter Address Load Strobe Input**. Counter control input.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	**Port Counter Enable Input**. Counter control input.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	**Port Counter Reset Input**. Counter control input.
$\overline{CNTINT}_L$	$\overline{CNTINT}_R$	**Port Counter Interrupt Output**. This pin is asserted LOW one cycle before the unmasked portion of the counter is incremented to all “1s”.
$\overline{WRP}_L$	$\overline{WRP}_R$	**Port Counter Wrap Input**. When the burst counter reaches the maximum count, on the next counter increment $\overline{WRP}$ can be set LOW to load the unmasked counter bits to 0 or set HIGH to load the counter with the value stored in the mirror register.
$\overline{RET}_L$	$\overline{RET}_R$	**Port Counter Retransmit Input**. Assert this pin LOW to reload the initial address for repeated access to the same segment of memory.
$VREF_L$	$VREF_R$	**Port External HSTL I/O Reference Input**.
$VDDIO_L$	$VDDIO_R$	**Port Data I/O Power Supply**.
$\overline{FTSEL}_L$	$\overline{FTSEL}_R$	**Port Flow-Through Mode Select Input**. Assert this pin LOW to select Flow-Through mode. Assert this pin HIGH to select Pipeline mode.
$\overline{MRST}$		**Master Reset Input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A $\overline{MRST}$ operation is required at power-up. This pin must be driven by a $VDDIO_L$ referenced signal.
VC_SEL		**Core Power Supply Select**. Assert this pin LOW to select 1.8V Core operation. Assert this pin HIGH to select 1.5V Core operation. This pin must be driven by a VTTL referenced signal.
TMS		**JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK. Operation for LVTTL or 2.5V LVCMOS.
TDI		**JTAG Test Data Input**. Data on the TDI input will be shifted serially into selected registers. Operation for LVTTL or 2.5V LVCMOS.
TRST		**JTAG Reset Input**. Operation for LVTTL or 2.5V LVCMOS.
TCK		**JTAG Test Clock Input**. Operation for LVTTL or 2.5V LVCMOS.
TDO		**JTAG Test Data Output**. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP. Operation for LVTTL or 2.5V LVCMOS.
VSS		**Ground Inputs**.
VCORE		**Device Core Power Supply**.
VTTL		**LVTTL Power Supply**.

Selectable I/O Standard

The FullFlex families of devices also offer the option of choosing one of four port standards for the device. Each port can independently select standards from single-ended HSTL class I, single-ended LVTTL, 2.5V LVCMOS, or 1.8V LVCMOS. The selection of the standard is determined by the PORTSTD pins for each port. These pins should be connected to either an LVTTL or 2.5V LVCMOS power suppy. This will determine the input clock, address, control, data, and Echo clock standard for each port as shown in *Table 2*.

Table 2. Port Standard Selection

PORTSTD1	PORTSTD0	I/O Standard
VSS	VSS	LVTTL
VSS	VTTL	HSTL
VTTL	VSS	2.5V LVCMOS
VTTL	VTTL	1.8V LVCMOS

Operating mode with different IO standards combined with different core power supply will result in different maximum speed as shown in *Table 3*.

Table 3. Speed vs. I/O Standard and Pipeline Stages

Maximum Speed (MHz)	Core Voltage (V)	I/O Standard	Latency Cycles
250[15]	1.8	HSTL/1.8V LVCMOS	2
200	1.8	LVTTL/2.5V LVCMOS	2
200	1.5	HSTL/LVTTL 2.5V LVCMOS 1.8V LVCMOS	2

Clocking

Separate clocks synchronize the operations on each port. Each port has one clock input C. In this mode, all the transactions on the address, control, and data will be on the C rising edge. All transactions on the address, control, data input, output, and byte enables will occur on the C rising edge.

Table 4. Data Pin Assignment

BE Pin Name	Data Pin Name
BE[7]	DQ[71:63]
BE[6]	DQ[62:54]
BE[5]	DQ[53:45]
BE[4]	DQ[44:36]
BE[3]	DQ[35:27]
BE[2]	DQ[26:18]
BE[1]	DQ[17:9]
BE[0]	DQ[8:0]

Selectable Pipeline/Flow-Through Mode

To meet data rate and throughput requirements, the FullFlex families offer selectable pipeline or flow-through mode. Echo clocks are not supported in flow-through mode and the DLL must be disabled.

Flow-Through mode is selected by the $\overline{\text{FTSEL}}$ pin. Strapping this pin HIGH selects pipeline mode. Strapping this pin LOW selects flow-through mode.

DLL

The FullFlex familes of devices have an on-chip DLL. Enabling the DLL reduces the clock to data valid time allowing more set-up time for the receiving device. For operation below 100 MHz, the DLL must be disabled. This is selectable by strapping LowSPD low. For information on DLL lock and reset time, please see the Master Reset section below.

Echo Clocking

As the speed of data increases, on-board delays caused by parasitics make providing accurate clock trees extremely difficult. To counter this problem, the FullFlex families incorporate Echo Clocks. Echo Clocks are enabled on a per port basis. The dual-port receives input clocks that are used to clock in the address and control signals for a read operation. The dual-port retransmits the input clocks relative to the data output. The buffered clocks are provided on the CQ1/$\overline{\text{CQ1}}$ and CQ0/$\overline{\text{CQ0}}$ outputs. Each port has a pair of Echo clocks. Each clock is associated with half the data bits. The output clock will match the corresponding ports I/O configuration.

To enable Echo clock outputs, tie CQEN HIGH. To disable Echo clock outputs, tie CQEN LOW.

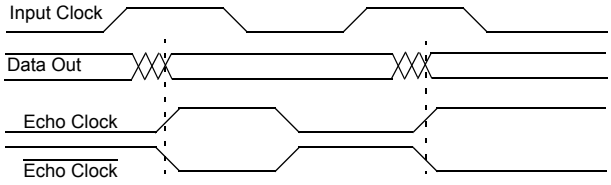


Figure 2. SDR Echo Clock Delay

Deterministic Access Control

Deterministic Access Control is provided for ease of design. The circuitry detects when both ports are accessing the same location and provides an external $\overline{\text{BUSY}}$ flag to the port on which data may be corrupted. The collision detection logic saves the address in conflict (Busy Address) to a readable register. In the case of multiple collisions, the first Busy address will be written to the Busy Address register.

If both ports are accessing the same location at the same time and only one port is doing a write, if t_{CCS} is met, then the data being written to and read from the address is valid data. For example, if the right port is reading and the left port is writing and the left ports clock meets t_{CCS}, then the data being read from the address by the right port will be the old data. In the same case, if the right ports clock meets t_{CCS}, then the data being read out of the address from the right port will be the new data. In the above case, if t_{CCS} is violated by the either ports clock with respect to the other port and the right port gets the external $\overline{\text{BUSY}}$ flag, the data from the right port is corrupted. *Table 5* shows the t_{CCS} timing that must be met to guarantee the data.

Table 6 shows that, in the case of the left port writing and the right port reading, when an external $\overline{\text{BUSY}}$ flag is asserted on the right port, the data read out of the device will not be guaranteed.

The value in the busy address register can be read back to the address lines. The required input control signals for this function are shown in *Table 9*. The value in the busy address register will be read out to the address lines t_{CA} after the same amount of latency as a data read operation. After an initial address match, the address under contention is saved in the busy address register. All following address matches cause the $\overline{\text{BUSY}}$ flag to be generated, however, none of the addresses are saved into the busy address register. Once a busy readback is performed, the address of the first match which happens at least two clocks cycles after the busy readback, is saved into the busy address register.

Table 5. t_{CCS} Timing for All Operating Modes

Port A—Early Arriving Port		Port B—Late Arriving Port		t_{CCS}	Unit
Mode	Active Edge	Mode	Active Edge	C Rise to Opposite C Rise Set-up Time for Non-corrupt Data	
SDR	C	SDR	C	$t_{CYC(min)} - 1$	ns

Table 6. Deterministic Access Control Logic

Left Port	Right Port	Left Clock	Right Clock	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Description
Read	Read	X	X	H	H	No Collision
Write	Read	$>t_{CCS}$	0	H	H	Read OLD Data
		0	$>t_{CCS}$	H	H	Read NEW Data
		$<t_{CCS}$	0	H	H	Read OLD Data
				H	L	Data Not Guaranteed
		0	$<t_{CCS}$	H	H	Read NEW Data
				H	L	Data Not Guaranteed
Read	Write	$>t_{CCS}$	0	H	H	Read NEW Data
		0	$>t_{CCS}$	H	H	Read OLD Data
		$<t_{CCS}$	0	H	H	Read NEW Data
				L	H	Data Not Guaranteed
		0	$<t_{CCS}$	H	H	Read OLD Data
				L	H	Data Not Guaranteed
Write	Write	0	$>-t_{CCS}$ & $<t_{CCS}$	L	L	Array Data Corrupted
		0	$>t_{CCS}$	L	H	Array Stores Right Port Data
		$>t_{CCS}$	0	H	L	Array Stores Left Port Data

Variable Impedance Matching (VIM)

Each port contains a Variable Impedance Matching circuit to set the impedance of the I/O driver to match the impedance of the on-board traces. The impedance is set for all outputs except JTAG and is done on a per port basis. To take advantage of the VIM feature, connect a calibrating resistor (RQ) that is five times the value of the intended line impedance from the ZQ pin to VSS. The output impedance is then adjusted to account for drifts in supply voltage and temperature every 1024 clock cycles. If a port's clock is suspended, the VIM circuit will retain its last setting until the clock is restarted where it will then resume periodic adjustment. In the case of a significant change in device temperature or supply voltage, the recalibration period is multiples of 1024 clock cycles. A Master Reset will initialize the VIM circuitry. *Table 7* shows the VIM parameters and *Table 8* describes the VIM operation modes.

In order to disable VIM, the ZQ pin must be connected to VDDIO of the relative supply for the I/Os before a Master Reset.

Table 7. Variable Impedance Matching Parameters

Parameter	Min.	Max.	Unit	Tolerance
RQ Value	100	275	Ω	± 2%
Output Impedance	20	55	Ω	± 15%
Reset Time	N/A	1024	Cycles	N/A
Update Time	N/A	1024	Cycles	N/A

Table 8. Variable Impedance Matching Operation

RQ Connection	Output Configuration
100Ω - 275Ω to VSS	Output Driver Impedance = RQ/5 ± 15% at Vout = VDDIO/2
ZQ to VDDIO	VIM Disabled. Rout ≤ 20Ω at Vout = VDDIO/2

Address Counter and Mask Register Operations[1]

Each port of the FullFlex family contains a programmable burst address counter. The burst counter contains four registers: a counter register, a mask register, a mirror register, and a busy address register.

The **counter register** contains the address used to access the RAM array. It is changed only by the master reset ($\overline{MRST}$), Counter Reset, Counter Load, Retransmit, and Counter Increment operations.

The **mask register** value affects the Counter Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output ($\overline{CNTINT}$). The mask register is only changed by Mask Reset, Mask Load, and $\overline{MRST}$. The Mask Load operation loads the value of the address bus into the mask register. The mask register defines the counting range of the counter register. It divides the counter register into two or three consecutive regions. Zero or more "0s" define the masked region and one or more "1s" define the unmasked portion of the counter register. The counter register may only be divided into up to three regions. The region containing the least significant bits must be no more than two bits. Bits one and zero may be "10" respectively, masking the least significant counter bit and causing the counter to increment by two instead of one. If bits one and zero are "00", the two least significant bits are masked and the counter will increment by four instead of one. For example, in the case of a 256Kx72

configuration, a mask register value of 003FC divides the mask register into three regions. With bit 0 being the least significant bit and bit 17 being the most significant bit, the two least significant bits are masked, the next eight bits are unmasked, and the remaining bits are masked.

The mirror register is used to reload the counter register on retransmit operations (see “retransmit” below) and wrap functions (see “counter increment” below). The last value loaded into the counter register is stored in the mirror register. The mirror register is only changed by master reset ($\overline{MRST}$), Counter Reset, and Counter Load.

Table 9 summarizes the operations of these registers and the required input control signals. All signals except $\overline{MRST}$ are synchronized to the ports clock.

Counter Load Operation[1]

The address counter and mirror registers are both loaded with the address value presented on the address lines. This value ranges from 0 to 1FFFFF.

Mask Load Operation[1]

The mask register is loaded with the address value presented on the address bus. This value ranges from 0 to 1FFFFF though not all values permit correct increment operations. Permitted values are in the form of 2^n–1, 2^n–2, or 2^n–4. The counter register can only be segmented in up to three regions. From the most significant bit to the least significant bit, permitted values have zero or more “0s”, one or more “1s”, and the least significant two bits can be “11”, “10”, or “00”. Thus 1FFFFE, 07FFFF, and 003FFC are permitted values but 02FFFF, 003FFA, and 07FFE4 are not.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. The address will be valid t_{CA} after the selected number of latency cycles configured by $\overline{FTSEL}$. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. *Figure 3* shows a block diagram of the operation.

Mask Readback Operation

The internal value of the mask register can be read out on the address lines. The address will be valid t_{CA} after the selected number of latency cycles configured by $\overline{FTSEL}$. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. *Figure 3* shows a block diagram of the operation.

Counter Reset Operation

All unmasked bits of the counter and mirror registers are reset to “0”. All masked bits remain unchanged. A mask reset followed by a counter reset will reset the counter and mirror registers to 00000.

Mask Reset Operation

The mask register is reset to all “1s”, which unmasks every bit of the burst counter.

Table 9. Burst Counter and Mask Register Control Operation (Any Port) [18, 19]

C	$\overline{\text{MRST}}$	$\overline{\text{CNTRST}}$	$\overline{\text{CNT/MSK}}$	$\overline{\text{CNTEN}}$	$\overline{\text{ADS}}$	$\overline{\text{RET}}$	Operation	Description
X	L	X	X	X	X	X	Master Reset	Reset address counter to all 0s, mask register to all 1s, and BUSY address to all 0's.
⎍	H	L	H	X	X	X	Counter Reset	Reset counter and mirror unmasked portion to all 0s.
⎍	H	L	L	X	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	H	H	L	L	X	Counter Load	Load burst counter and mirror with external address value presented on address lines.
⎍	H	H	L	L	L	X	Mask Load	Load mask register with value presented on the address lines.
⎍	H	H	H	L	H	L	Retransmit	Load counter with value in the mirror register
⎍	H	H	H	L	H	H	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
⎍	H	H	L	H	H	L	Busy Address Readback	Read out last busy address
⎍	H	H	L	L	H	X	Reserved	
⎍	H	H	L	H	L	L	Reserved	
⎍	H	H	L	H	H	H	Reserved	
⎍	H	H	H	H	L	L	Reserved	
⎍	H	H	H	H	H	L	Reserved	

Notes:
18. "X" = "Don't Care," "H" = HIGH, "L" = LOW.
19. Counter operation and mask register operation is independent of chip enables.

Increment Operation[1]

Once the address counter is initially loaded with an external address, the counter can internally increment the address value and address the entire memory array. Only the unmasked bits of the counter register are incremented. In order for a counter bit to change, the corresponding bit in the mask register must be “1”. If the two least significant bits of the mask register are “11”, the burst counter will increment by one. If the two least significant bits are “10”, the burst counter will increment by two, and if they are “00”, the burst counter will increment by four. If all unmasked counter bits are incremented to “1” and $\overline{WRP}$ is deasserted, the next increment will wrap the counter back to the initially loaded value. The cycle before an increment will result in the unmasked counter bits being “1s”, a counter interrupt flag ($\overline{CNTINT}$) is asserted if the counter is continuously incrementing. The next increment will cause the counter to reach its maximum value and the second increment will return the counter register to its initial value which was stored in the mirror register when $\overline{WRP}$ is deasserted. When $\overline{WRP}$ is asserted, the second increment after $\overline{CNTINT}$ is asserted will load the unmasked counter bits with “0”. The example shown in *Figure 4* shows an example of the CYDD36S18V18 device with the mask register loaded with a mask value of 00007F unmasking the seven least significant bits. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 000005 assuming $\overline{WRP}$ is deasserted. The masked bits, the seventh address through the twenty-first address, do not increment in an increment operation. The counter address will start at address 000005 and will increment its internal address value until it reaches the mask register value of 00007F. The counter wraps around the memory block to location 000005 at the next count. $\overline{CNTINT}$ is issued when the counter reaches the maximum –1 count.

Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Retransmit

Retransmit allows repeated access to the same block of memory without the need to reload the initial address. An internal mirror register stores the address counter value last loaded. When the burst counter reaches its maximum value set by the mask register, it wraps back to the initial value stored in the mirror register as long as $\overline{WRP}$ is deasserted. The unmasked counter bits will be loaded with “0” If $\overline{WRP}$ is asserted. If the counter is configured to continuously be in increment mode, it increments once again to the maximum value and wraps back to the value initially stored in the mirror register as long as $\overline{WRP}$ is deasserted. While $\overline{RET}$ is asserted low, the counter will continue to wrap back to the value in the mirror register independent of the state of $\overline{WRP}$.

Counter Interrupt

The counter interrupt ($\overline{CNTINT}$) is asserted LOW one clock cycle before an increment operation that results in the unmasked portion of the counter register being all “1s”. It is deasserted by counter reset, counter load, mask reset, mask load, and $\overline{MRST}$.

Counting by Two

When the two least significant bits of the mask register are “10,” the counter increments by two.

Counting by Four

When the two least significant bits of the mask register are “00”, the counter increments by four.

Mailbox Interrupts

The upper two memory locations can be used for message passing and permit communications between ports. *Table 10* shows the interrupt operation for both ports. The highest memory location is the mailbox for the right port and the maximum address – 1 is the mailbox for the left port.

When one port Writes to the other port’s mailbox, the $\overline{INT}$ flag of the port that the mailbox belongs to is asserted LOW. The $\overline{INT}$ flag remains asserted until the mailbox location is read by the other port. When a port reads its mailbox, the $\overline{INT}$ flag is deasserted high after one cycle of latency with respect to the input clock of the port to which the mailbox belongs and is independent of $\overline{OE}$.

Table 10 shows that in order to set the $\overline{INT}_R$ flag, a Write operation by the left port to address 1FFFFF will assert $\overline{INT}_R$ LOW. A valid Read of the 1FFFFF location by the right port will reset $\overline{INT}_R$ HIGH after one cycle of latency with respect to the right port’s clock. At least one byte enable has to be activated to set or reset the mailbox interrupt.

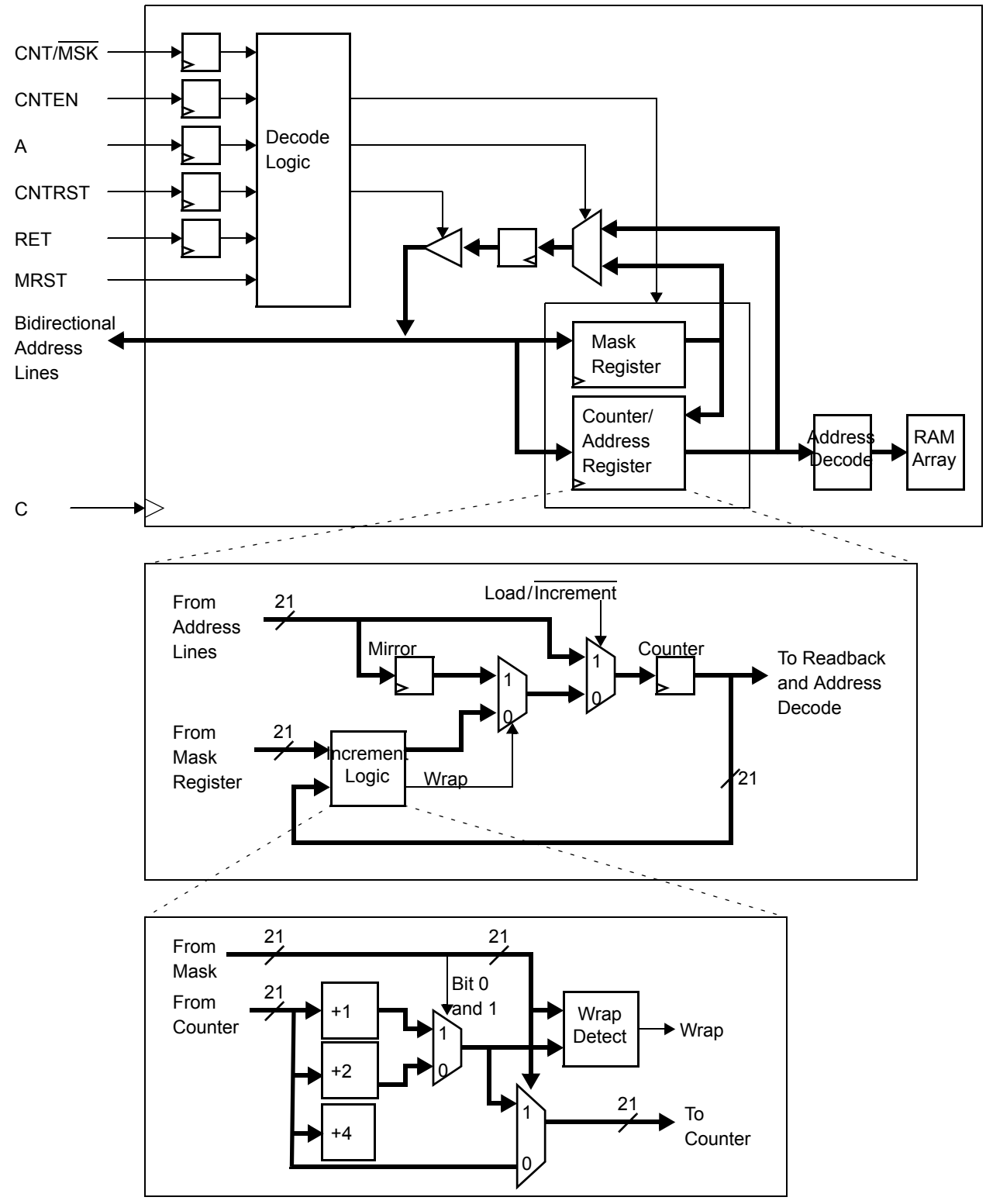


Figure 3. Counter, Mask, and Mirror Logic Block Diagram[1]

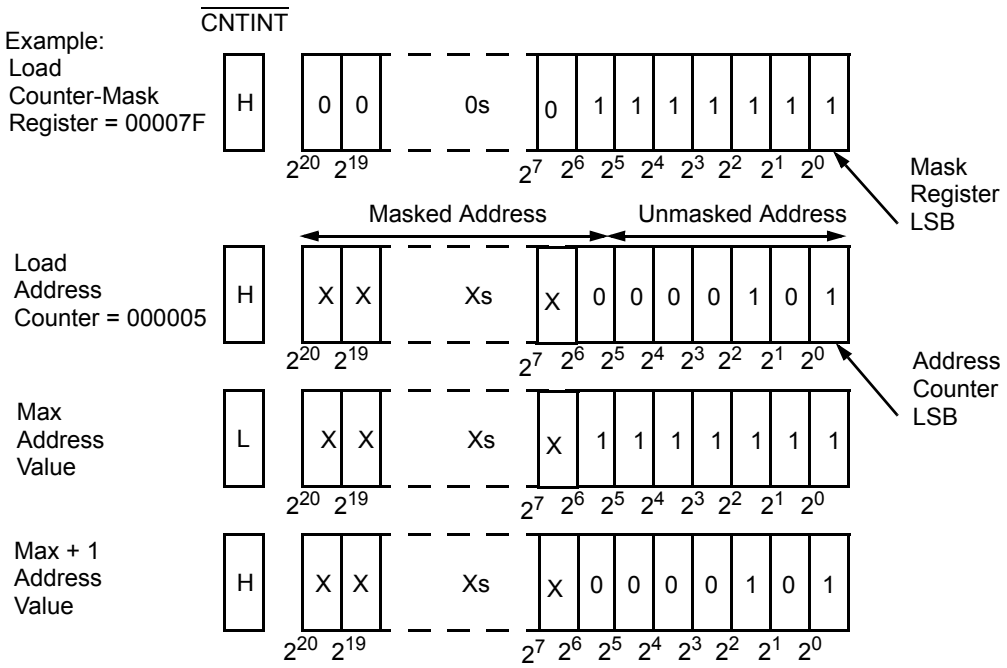


Figure 4. Programmable Counter-Mask Register Operation[1, 23]

Table 10.Interrupt Operation Example[1, 19, 20, 21, 22]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L-21L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R-21R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	Max. Address	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	Max. Address	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	Max. Address–1	X
Reset Left $\overline{INT}_L$ Flag	H	L	Max. Address–1	H	X	X	X	X

Master Reset

The FullFlex family of Dual-Ports undergo a complete reset by asserting MRST. The MRST can be asserted asynchronously to the clocks and must remain asserted for at least t_{RS}. Once asserted MRST deasserts READY, initializes the internal burst counters, internal mirror registers, and internal Busy Addresses to zero, and initializes the internal mask register to all “1s”. All mailbox interrupts ($\overline{INT}$), Busy Address Outputs (BUSY), and burst counter interrupts (CNTINT) are deasserted upon master reset. Releasing MRST also signifies that the power supplies and all port clocks are stable. This begins calibration of the DLL and VIM circuits. READY will be asserted within 1024 clock cycles. READY is a wired OR capable output with a strong pull-up and weak pull-down. Up to four outputs may be connected together. For faster pull-down of the signal, connect a 250 Ohm resistor to VSS. If the DLL and VIM circuits are disabled for a port, the port will be operational within five clock cycles. However, the READY will be asserted within 160 clock cycles.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The FullFlex families incorporate an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels depending on the VTTL power supply. It is composed of four input connections and one output connection required by the test logic defined by the standard.

Notes:
20. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the C and can be deasserted after that. Data will be out after the following C edge and will be tri-stated after the next C edge.
21. $\overline{OE}$ is “Don’t Care” for mailbox operation.
22. At least one of $\overline{BE0}$, $\overline{BE1}$, $\overline{BE2}$, $\overline{BE3}$, $\overline{BE4}$, $\overline{BE5}$, $\overline{BE6}$, or $\overline{BE7}$ must be LOW.
23. The “X” in this diagram represents the counter upper bits.

Table 11.Identification Register Definitions

Part Number	Configuration	Value
CYD36S72V18	512Kx72	0C022069h
CYD36S36V18	1024Kx36	0C023069h
CYD36S18V18	2048Kx36	0C024069h
CYD18S72V18	256Kx72	0C025069h
CYD18S36V18	512Kx36	0C026069h
CYD18S18V18	1024Kx18	0C027069h
CYD09S72V18	128Kx72	0C028069h
CYD09S36V18	256Kx36	0C029069h
CYD09S18V18	1024Kx18	0C02A069h
CYD04S72V18	64Kx72	0C02B069h
CYD04S36V18	128Kx36	0C02C069h
CYD04S18V18	256Kx18	0C02D069h

Table 12.Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n[24]

Table 13.Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all FullFlex72 and FullFlex36 output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Note:
24. Details of the boundary scan length can be found in the BSDL file for the device.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to + 4.1V

DC Voltage Applied to Outputs in High-Z State.....–0.5V to V_{CORE} + 0.5V

DC Input Voltage..... –0.5V to V_{CORE} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage .....> 2200V

(JEDEC JESD8-6, JESD8-B)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	VCORE
Commercial	0°C to +70°C	1.8V ± 100 mV 1.5V ± 80 mV
Industrial	–40°C to +85°C	1.8V ± 100 mV 1.5V ± 80 mV

Power Supply Requirements

	Min.	Typ.	Max.
LVTTL VDDIO	3.0V	3.3V	3.6V
2.5V LVCMOS VDDIO	2.3V	2.5V	2.7V
HSTL VDDIO	1.4V	1.5V	1.9V
1.8V LVCMOS VDDIO	1.7V	1.8V	1.9V
3.3V VTTL	3.0V	3.3V	3.6V
2.5V VTTL	2.3V	2.5V	2.7V
HSTL VREF	0.68V	0.75V	0.95V

Electrical Characteristics Over the Operating Range

Parameter	Description	Configuration	-250[15]			-200			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{CORE}=Min., I_{OH}=-8 mA)	LVTTL	2.4[25]			2.4 [25]			V
	(V_{CORE}=Min., I_{OH}=-4 mA)	HSTL (DC)[26]	VDDIO – 0.4[25]			VDDIO – 0.4[25]			V
	(V_{CORE}=Min., I_{OH}=-4 mA)	HSTL (AC)[26]	VDDIO – 0.5[25]			VDDIO – 0.5[25]			V
	(V_{CORE}=Min., I_{OH}=-6 mA)	2.5V LVCMOS	1.7[25]			1.7[25]			V
	(V_{CORE}=Min., I_{OH}=-4 mA)	1.8V LVCMOS	VDDIO – 0.45[25]			VDDIO – 0.45[25]			V
V_{OL}	Output HIGH Voltage (V_{CORE}=Min., I_{OL}= 8 mA)	LVTTL			0.4[25]			0.4[25]	V
	(V_{CORE}=Min., I_{OL}= 4 mA)	HSTL (DC)[26]			0.4[25]			0.4[25]	V
	(V_{CORE}=Min., I_{OL}= 4 mA)	HSTL (AC)[26]			0.5[25]			0.5[25]	V
	(V_{CORE}=Min., I_{OL}= 6 mA)	2.5V LVCMOS			0.7[25]			0.7[25]	V
	(V_{CORE}=Min., I_{OL}= 4 mA)	1.8V LVCMOS			0.2[25]			0.2[25]	V
V_{IH}	Input HIGH Voltage	LVTTL	2		VDDIO + 0.3	2		VDDIO + 0.3	V
		HSTL (DC)[26]	VREF + 0.1		VDDIO + 0.3	VREF + 0.1		VDDIO + 0.3	V
		HSTL (AC)[26]	VREF + 0.2			VREF + 0.2			V
		2.5V LVCMOS	1.7			1.7			V
		1.8V LVCMOS	1.26			1.26			V
V_{IL}	Input LOW Voltage	LVTTL	–0.3		0.8	–0.3		0.8	V
		HSTL (DC)[26]	–0.3		VREF – 0.1	–0.3		VREF – 0.1	V
		HSTL (AC)[26]			VREF – 0.2			VREF – 0.2	V
		2.5V LVCMOS	0.7			0.7			V
		1.8V LVCMOS	0.36			0.36			V

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration	-250[15]			-200			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{READY}$ V_{OH}	Output HIGH Voltage (V_{CORE} = Min., I_{OH} = –24 mA)	LVTTL	2.7[25]			2.7[25]			V
	(V_{CORE} = Min., I_{OH} = –12 mA)	HSTL (DC)[26]	VDDIO – 0.4[25]			VDDIO – 0.4[25]			V
	(V_{CORE} = Min., I_{OH} = –12 mA)	HSTL (AC)[26]	VDDIO – 0.5[25]			VDDIO – 0.5[25]			V
	(V_{CORE} = Min., I_{OH} = –15 mA)	2.5V LVCMOS	2.0[25]			2.0[25]			V
	(V_{CORE} = Min., I_{OH} = –12 mA)	1.8V LVCMOS	VDDIO – 0.45[25]			VDDIO – 0.45[25]			V
$\overline{READY}$ V_{OL}	Output HIGH Voltage (V_{CORE} = Min., I_O = 0.12 mA)	LVTTL			0.4[25]			0.4[25]	V
	(V_{CORE} = Min., I_{OL} = 0.12 mA)	HSTL (DC)			0.4[25]			0.4[25]	V
	(V_{CORE} = Min., I_{OL} = 0.12 mA)	HSTL (AC)			0.5[25]			0.5[25]	V
	(V_{CORE} = Min., I_{OL} = 0.15 mA)	2.5V LVCMOS			0.7[25]			0.7[25]	V
	(V_{CORE} = Min., I_{OL} = 0.08 mA)	1.8V LVCMOS			0.2[25]			0.2[25]	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, MRST		–10		10	–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, MRST		–300		10	–300		10	µA
I_{IX3}	Input Leakage Current PORTSTD, DDRON, VC_SEL		–10		300	–10		300	µA
I_{CC}	Operating Current (V_{CORE} = Max.,I_{OUT} = 0 mA) Outputs Disabled	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA

Notes:
25. These parameters are met with VIM disabled.
26. The (DC) specifications are measured under steady state conditions. The (AC) specifications are measured while switching at speed.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration	-250[15]			-200			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CORE} - 0.2V$, f = 0	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration	-250[15]			-200			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA

Electrical Characteristics Over the Operating Range

Parameter	Description	Configuration	-167			-133			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{CORE} = Min., I_{OH} = –8 mA)	LVTTL	2.4[25]			2.4 [25]			V
	(V_{CORE} = Min., I_{OH} = –4 mA)	HSTL (DC)	VDDIO – 0.4[25]			VDDIO – 0.4[25]			V
	(V_{CORE} = Min., I_{OH} = –4 mA)	HSTL (AC)	VDDIO – 0.5[25]			VDDIO – 0.5[25]			V
	(V_{CORE} = Min., I_{OH} = –6 mA)	2.5V LVCMOS	1.7[25]			1.7[25]			V
	(V_{CORE} = Min., I_{OH} = –4 mA)	1.8V LVCMOS	VDDIO – 0.45[25]			VDDIO – 0.45[25]			V
V_{OL}	Output HIGH Voltage (V_{CORE} = Min., I_{OH} = –8 mA)	LVTTL			0.4[25]			0.4[25]	V
	(V_{CORE} = Min., I_{OH} = –4 mA)	HSTL (DC)			0.4[25]			0.4[25]	V
	(V_{CORE} = Min., I_{OH} = –4 mA)	HSTL (AC)			0.5[25]			0.5[25]	V
	(V_{CORE} = Min., I_{OH} = –6 mA)	2.5V LVCMOS			0.7[25]			0.7[25]	V
	(V_{CORE} = Min., I_{OH} = –4 mA)	1.8V LVCMOS			0.2[25]			0.2[25]	V
V_{IH}	Input HIGH Voltage	LVTTL	2		VDDIO + 0.3	2		VDDIO + 0.3	V
		HSTL (DC)	VREF + 0.1		VDDIO + 0.3	VREF + 0.1		VDDIO + 0.3	V
		HSTL (AC)	VREF + 0.2			VREF + 0.2			V
		2.5V LVCMOS	1.7			1.7			V
		1.8V LVCMOS	1.26			1.26			V
V_{IL}	Input LOW Voltage	LVTTL	–0.3		0.8	–0.3		0.8	V
		HSTL (DC)	–0.3		VREF – 0.1	–0.3		VREF – 0.1	V
		HSTL (AC)			VREF – 0.2			VREF – 0.2	V
		2.5V LVCMOS	0.7			0.7			V
		1.8V LVCMOS	0.36			0.36			V

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration	-167			-133			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{READY}$ V_{OH}	Output HIGH Voltage (V_{CORE} = Min., I_{OH} = –24 mA)	LVTTL	2.7[25]			2.7[25]			V
	(V_{CORE} = Min., I_{OH} = –12 mA)	HSTL (DC)[26]	VDDIO – 0.4[25]			VDDIO – 0.4[25]			V
	(V_{CORE} = Min., I_{OH} = –12 mA)	HSTL (AC)[26]	VDDIO – 0.5[25]			VDDIO – 0.5[25]			V
	(V_{CORE} = Min., I_{OH} = –15 mA)	2.5V LVCMOS	2.0[25]			2.0[25]			V
	(V_{CORE} = Min., I_{OH} = –12 mA)	1.8V LVCMOS	VDDIO – 0.45[25]			VDDIO – 0.45[25]			V
$\overline{READY}$ V_{OL}	Output HIGH Voltage (V_{CORE} = Min., I_{OL} = 0.12 mA)	LVTTL			0.4[25]			0.4[25]	V
	(V_{CORE} = Min., I_{OL} = 0.12 mA)	HSTL (DC)			0.4[25]			0.4[25]	V
	(V_{CORE} = Min., I_{OL} = 0.12 mA)	HSTL (AC)			0.5[25]			0.5[25]	V
	(V_{CORE} = Min., I_{OL} = 0.15 mA)	2.5V LVCMOS			0.7[25]			0.7[25]	V
	(V_{CORE} = Min., I_{OL} = 0.08 mA)	1.8V LVCMOS			0.2[25]			0.2[25]	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, $\overline{MRST}$		–10		10	–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, $\overline{MRST}$		–300		10	–300		10	µA
I_{IX3}	Input Leakage Current PORTSTD, DDRON, VC_SEL		–10		300	–10		300	µA
I_{CC}	Operating Current (V_{CORE} = Max., I_{OUT} = 0 mA) Outputs Disabled	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration	-167			-133			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CORE} - 0.2V$, f = 0	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Configuration	-167			-133			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}	512Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		2048Kx18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		1024x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		512x18	TBD	TBD	TBD	TBD	TBD	TBD	mA
		64Kx72	TBD	TBD	TBD	TBD	TBD	TBD	mA
		128Kx36	TBD	TBD	TBD	TBD	TBD	TBD	mA
		256x18	TBD	TBD	TBD	TBD	TBD	TBD	mA

Table 14.Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}[27]	Input Capacitance	T_A = °C, f = MHz, V_{CORE} = 3 dV[28]	10	pF
C_{OUT}[27, 29]	Output Capacitance		12	pF

AC Test Load and Waveforms

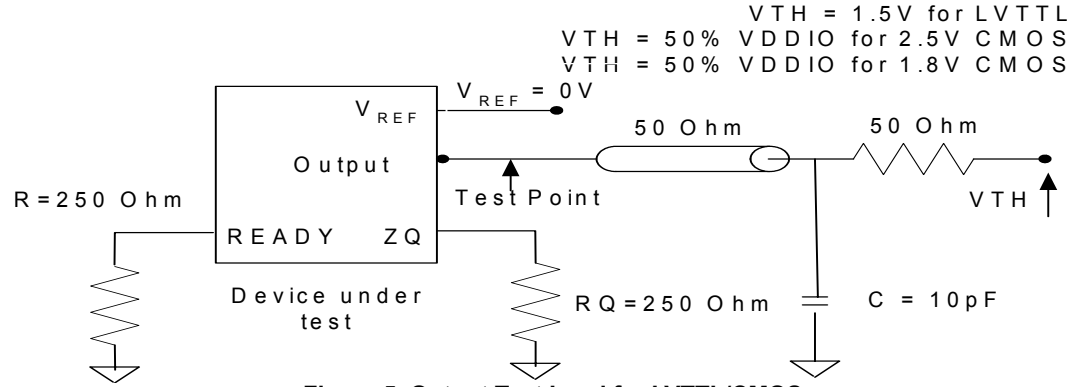


Figure 5. Output Test Load for LVTTL/CMOS

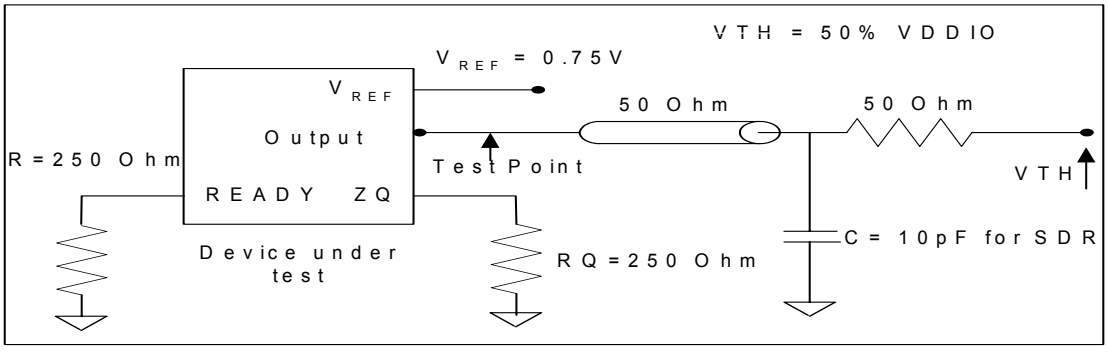


Figure 6. Output Test Load for HSTL

Notes:
27. Capacitance for the 36M x18 device is 20 pF, capacitance for all other 36M or x18 devices is 12 pF.
28. Input and Output switch from 0V to 3V or from 3V to 0V.
29. C_{out} also references to $C_{I/O}$.

Switching Characteristics Over the Operating Range

Table 15.SDR Mode with DLL Enabled ($\overline{\text{LOWSPD}}$-HIGH)[32]

Parameter	Description	-250[15]		-200		-167		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (PIPELINED)	Maximum Operating Frequency for Pipelined mode	100	250	100	200	100	167	100	133	MHz
f_{MAX}[33] (FLOW-THROUGH)	Maximum Operating Frequency for Flow-through mode		100		77		66.7		55.6	MHz
t_{CYC} (PIPELINED)	C Clock Cycle Time for Pipelined mode	4.00	10.00	5.00	10.00	6.00	10.00	7.00	10.00	ns
t_{CYC} (FLOW-THROUGH)	C Clock Cycle Time for Flow-through mode	10.00		13.00		15.00		18.00		ns
t_{CKD}	C Clock Duty Time	45	55	45	55	45	55	45	55	%
t_{SD}	Data Input Set-up Time to C Rise	1.20[31]		1.50[31]		1.70[31]		1.80[31]		ns
t_{HD}	Data Input Hold Time after C Rise	0.50[31]		0.50[31]		0.50[31]		0.50[31]		ns
t_{SAC}	Address & Control Input Setup Time to C Rise	1.20		1.50		1.70		1.80		ns
t_{HAC}	Address & Control Input Hold Time after C Rise	0.50		0.50		0.60		0.70		ns
t_{OE}	Output Enable to Data Valid		3.40[31]		4.40[31]		5.00[31]		5.50[31]	ns
t_{OLZ}[30]	OE to Low Z	1.00		1.00		1.00		1.00		ns
t_{OHZ}[30]	OE to High Z	1.00[31]	3.40[31]	1.00[31]	4.40[31]	1.00[31]	5.00[31]	1.00[31]	5.50[31]	ns
t_{CD1}	C Rise to DQ Valid for Flow-through Mode ($\overline{\text{LowSPD}}$ = 1)		7.20		9.00		11.00		13.00	ns
t_{CD2}	C Rise to DQ Valid for Pipelined mode ($\overline{\text{LowSPD}}$ = 1)		2.64[31]		3.30[31]		4.00[31]		4.50[31]	ns
t_{CA1}	C Rise to Address Readback Valid for flow-through mode		7.20		9.00		11.00		13.00	ns
t_{CA2}	C Rise to Address Readback Valid for pipelined mode		4.00		5.00		6.00		7.50	ns
t_{DC}	DQ Output Hold after C Rise	1.00		1.00		1.00		1.00		ns
t_{CCQ}	C Rise to CQ Rise	1.00	2.64	1.00	3.30	1.00	4.00	1.00	4.50	ns
t_{CQHQV}	Echo Clock (CQ) High to Output Valid		0.70[31]		0.76[31]		0.80[31]		0.90[31]	ns
t_{CQHQX}	Echo Clock (CQ) High to Output Hold	–0.66		–0.72		–0.76		–0.90		ns
t_{CKHZ1}[30]	C Rise to DQ Output High Z in Flow-Through Mode	1.00	7.20	1.00	9.00	1.00	11.00	1.00	13.00	ns
t_{CKLZ1}[30]	C Rise to DQ Output Low Z in Flow-Through Mode	1.00		1.00		1.00		1.00		ns
t_{CKHZ2}[30]	C Rise to DQ Output High Z in Pipelined Mode	1.00[31]	2.64[31]	1.00[31]	3.30[31]	1.00[31]	4.00[31]	1.00[31]	4.50[31]	ns
t_{CKLZ2}[30]	C Rise to DQ Output Low Z in Pipelined Mode	1.00		1.00		1.00		1.00		ns
t_{AC}	Address Output Hold after C Rise	1.00		1.00		1.00		1.00		ns

Notes:
30. Parameters specified with the load capacitance in *Figure 5* and *Figure 6*.
31. For the x18 devices, add 200 ps to this parameter in the table above.
32. Test conditions assume a signal transition time of 2 V/ns.
33. Flow-Through Mode operates at this frequency regardless of DLL being enabled or disabled

Table 15.SDR Mode with DLL Enabled ($\overline{\text{LOWSPD}}$-HIGH)[32] (continued)

Parameter	Description	-250[15]		-200		-167		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKHZA1}[30]	C Rise to Address Output High Z for Flow-Through Mode	1.00	7.20	1.00	9.00	1.00	11.00	1.00	13.00	ns
t_{CKHZA2}[30]	C Rise to Address Output High Z for Pipelined Mode	1.00	4.00	1.00	5.00	1.00	6.00	1.00	7.50	ns
t_{CKLZA}[30]	C Rise to Address Output Low Z	1.00		1.00		1.00		1.00		ns
t_{SCINT}	C Rise to CNTINT Low	1.00	2.64	1.00	3.30	1.00	4.00	1.00	4.50	ns
t_{RCINT}	C Rise to CNTINT High	1.00	2.64	1.00	3.30	1.00	4.00	1.00	4.50	ns
t_{SINT}	C Rise to INT Low	0.50	6.00	0.50	7.00	0.50	8.00	0.50	8.50	ns
t_{RINT}	C Rise to INT High	0.50	6.00	0.50	7.00	0.50	8.00	0.50	8.50	ns
t_{BSY}	C Rise to $\overline{\text{BUSY}}$ Valid	1.00	2.64	1.00	3.30	1.00	4.00	1.00	4.50	ns

Table 16. SDR Mode with DLL Disabled ($\overline{\text{LOWSPD}}$-LOW)[32]

Parameter	Description	-100		Unit
		Min.	Max.	
f_{MAX} (PIPELINED)	Maximum Operating Frequency for Pipelined mode		100	MHz
f_{MAX} (FLOW-THROUGH)[33]	Maximum Operating Frequency for Flow-through mode		55.6	MHz
t_{CYC} (PIPELINED)	C Clock Cycle Time for Pipelined mode	7.00	10.00	ns
t_{CYC} (FLOW-THROUGH)	C Clock Cycle Time for Flow-through mode	18.00		ns
t_{CKD}	C Clock Duty Time	45	55	%
t_{SD}	Data Input Set-up Time to C Rise	1.80[31]		ns
t_{HD}	Data Input Hold Time after C Rise	0.50[31]		ns
t_{SAC}	Address & Control Input Setup Time to C Rise	1.80		ns
t_{HAC}	Address & Control Input Hold Time after C Rise	0.70		ns
t_{OE}	Output Enable to Data Valid		5.50[31]	ns
t_{OLZ}[30]	OE to Low Z	1.00		ns
t_{OHZ}[30]	OE to High Z	1.00[31]	5.50[31]	ns
t_{CD1}	C Rise to DQ Valid for Flow-through Mode (LowSPD = 0)		13.00	ns
t_{CD2}	C Rise to DQ Valid for Pipelined mode (LowSPD = 0)		6.00[31]	ns
t_{CA1}	C Rise to Address Readback Valid for flow-through mode		13.00	ns
t_{CA2}	C Rise to Address Readback Valid for pipelined mode		7.50	ns
t_{DC}	DQ Output Hold after C Rise	1.00		ns
t_{CCQ}	C Rise to CQ Rise	1.00	6.00	ns
t_{CQHQV}	Echo Clock (CQ) High to Output Valid		0.90[31]	ns
t_{CQHQX}	Echo Clock (CQ) High to Output Hold	–0.90		ns
t_{CKHZ1}[30]	C Rise to DQ Output High Z in Flow-through Mode	1.00	13.00	ns
t_{CKLZ1}[30]	C Rise to DQ Output Low Z in Flow-Through Mode	1.00		ns
t_{CKHZ2}[30]	C Rise to DQ Output High Z in Pipelined Mode	1.00[31]	6.00[31]	ns
t_{CKLZ2}[30]	C Rise to DQ Output Low Z in Pipelined Mode	1.00		ns
t_{AC}	Address Output Hold after C Rise	1.00		ns
t_{CKHZA1}[30]	C Rise to Address Output High Z for Flow-Through mode	1.00	13.00	ns
t_{CKHZA2}[30]	C Rise to Address Output High Z for Pipelined mode	1.00	7.50	ns
t_{CKLZA}[30]	C Rise to Address Output Low Z	1.00		ns
t_{SCINT}	C Rise to CNTINT Low	1.00	4.50	ns
t_{RCINT}	C Rise to CNTINT High	1.00	4.50	ns

Table 16. SDR Mode with DLL Disabled ($\overline{\text{LOWSPD}}$-LOW)[32]

Parameter	Description	-100		Unit
		Min.	Max.	
t_{SINT}	C Rise to INT Low	0.50	8.50	ns
t_{RINT}	C Rise to INT High	0.50	8.50	ns
t_{BSY}	C Rise to BUSY Valid	1.00	4.50	ns

Master Reset Timing

Parameter	Description	-250[15]		-200		-167		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PUP}	Power-Up Time	1		1		1		1		ms
t_{RS}	Master Reset Pulse Width	5		5		5		5		cycles
t_{RSR}	Master Reset Recovery Time	5		5		5		5		cycles
t_{RSF}	Master Reset to Outputs Inactive/Hi Z		10		10		10		10	ns
t_{RDY}[34]	Master Reset Release to Port Ready		1024		1024		1024		1024	cycles
t_{CORDY}[35]	C Rise to Port Ready		8		9.5		11		13	ns

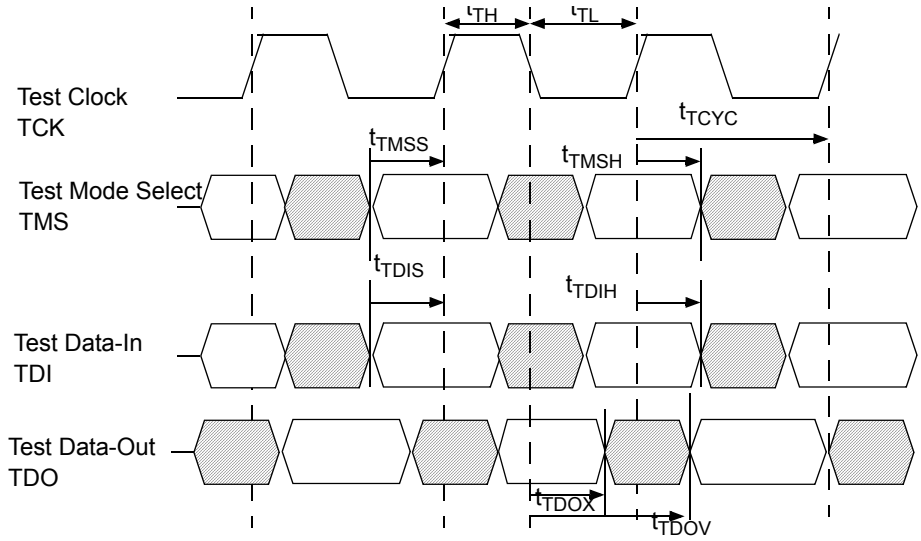
Table 17.JTAG Timing

Parameter	Description	-250[15]		-200		-167		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{JTAG}	JTAG TAP Controller Frequency		20		20		20		20	MHz
t_{TCYC}	TCK Cycle Time	50		50		50		50		ns
t_{TH}	TCK High Time	20		20		20		20		ns
t_{TL}	TCK Low Time	20		20		20		20		ns
t_{TMSS}	TMS Set-up to TCK Rise	10		10		10		10		ns
t_{TMSH}	TMS Hold to TCK Rise	10		10		10		10		ns
t_{TDIS}	TDI Set-up to TCK Rise	10		10		10		10		ns
t_{TDIH}	TDI Hold to TCK Rise	10		10		10		10		ns
t_{TDOV}	TCK Low to TDO Valid		10		10		10		10	ns
t_{TDOX}	TCK Low to TDO Invalid	0		0		0		0		ns
t_{JXZ}	TCK Low to TDO High Z		15		15		15		15	ns
t_{JZX}	TCK Low to TDO Active		15		15		15		15	ns

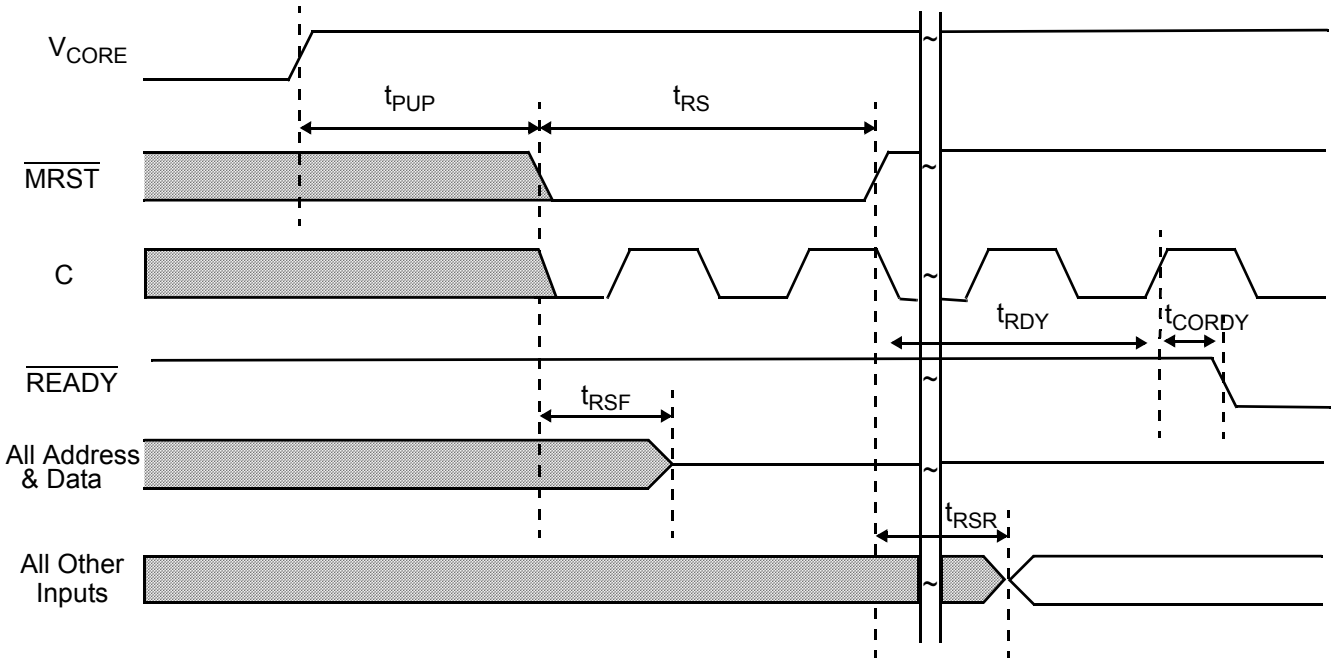
Notes:
34. $\overline{\text{READY}}$ is a wired OR capable output with a weak pull-down. For a decreased falling delay, connect a 250-Ohm resistor to VSS.
35. Add this propagation delay after t_{RDY} for all Master Reset Operations.

Switching Waveforms

JTAG Timing

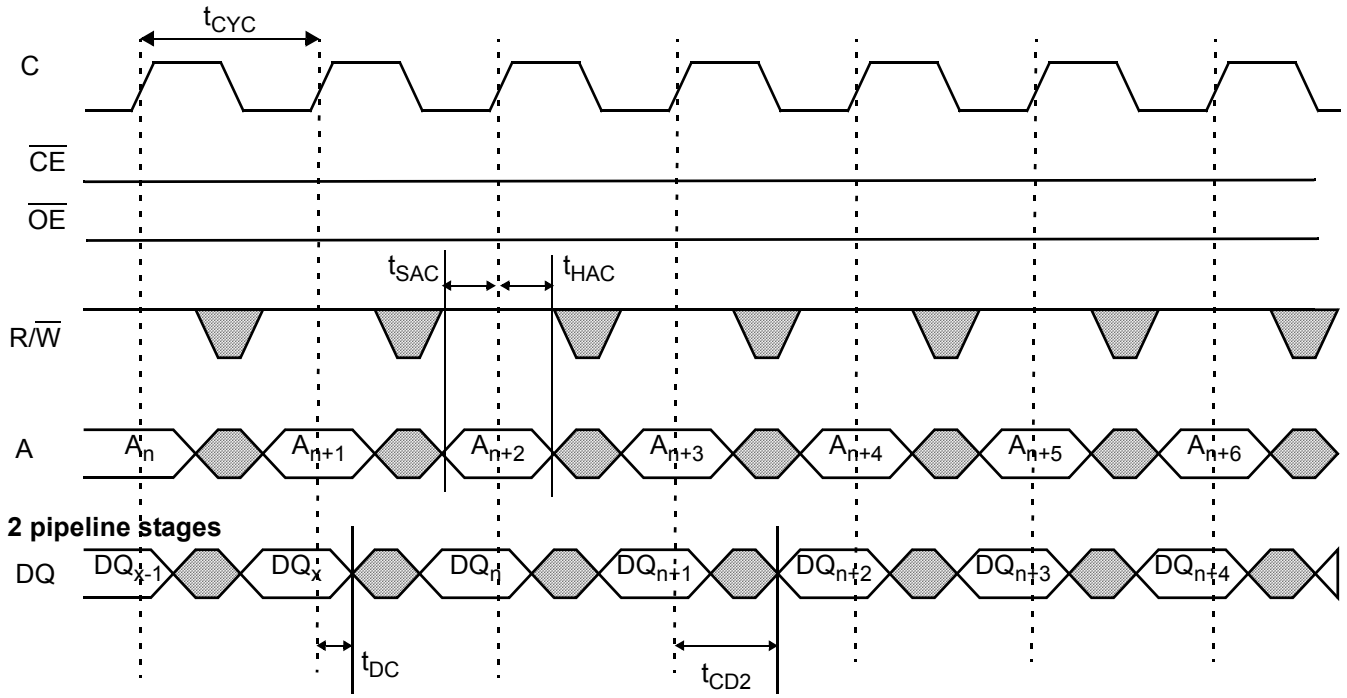


Master Reset[34]

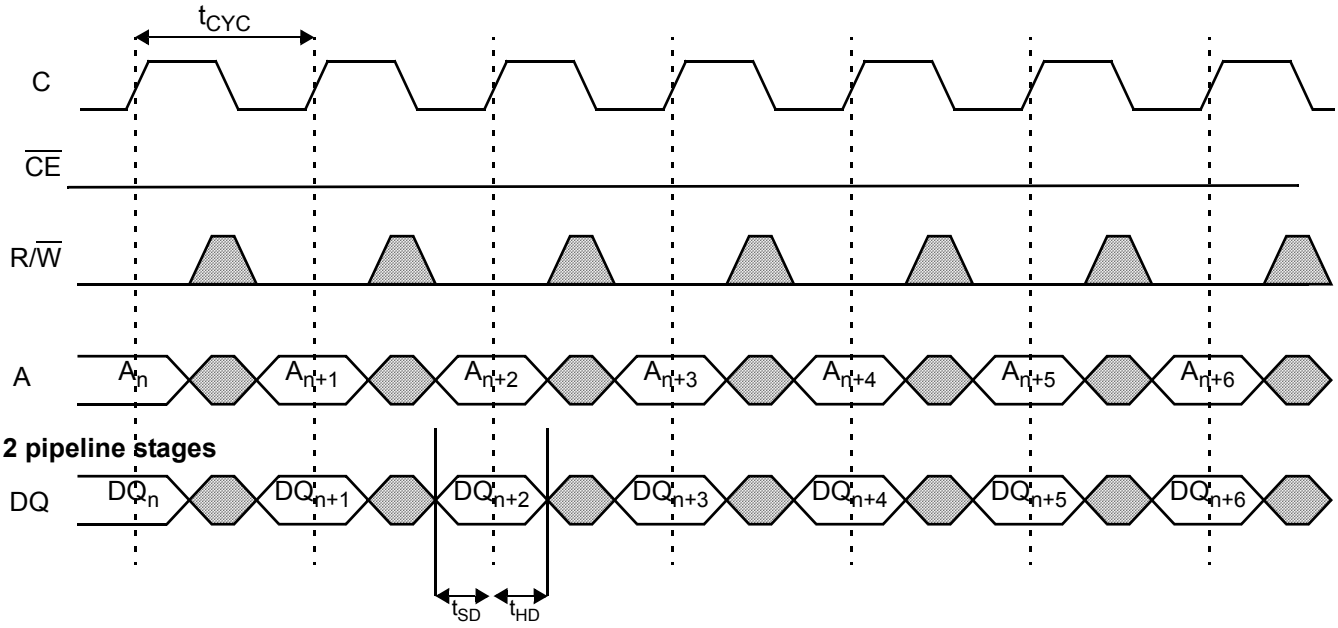


Switching Waveforms (continued)

READ Cycle for Pipelined Mode

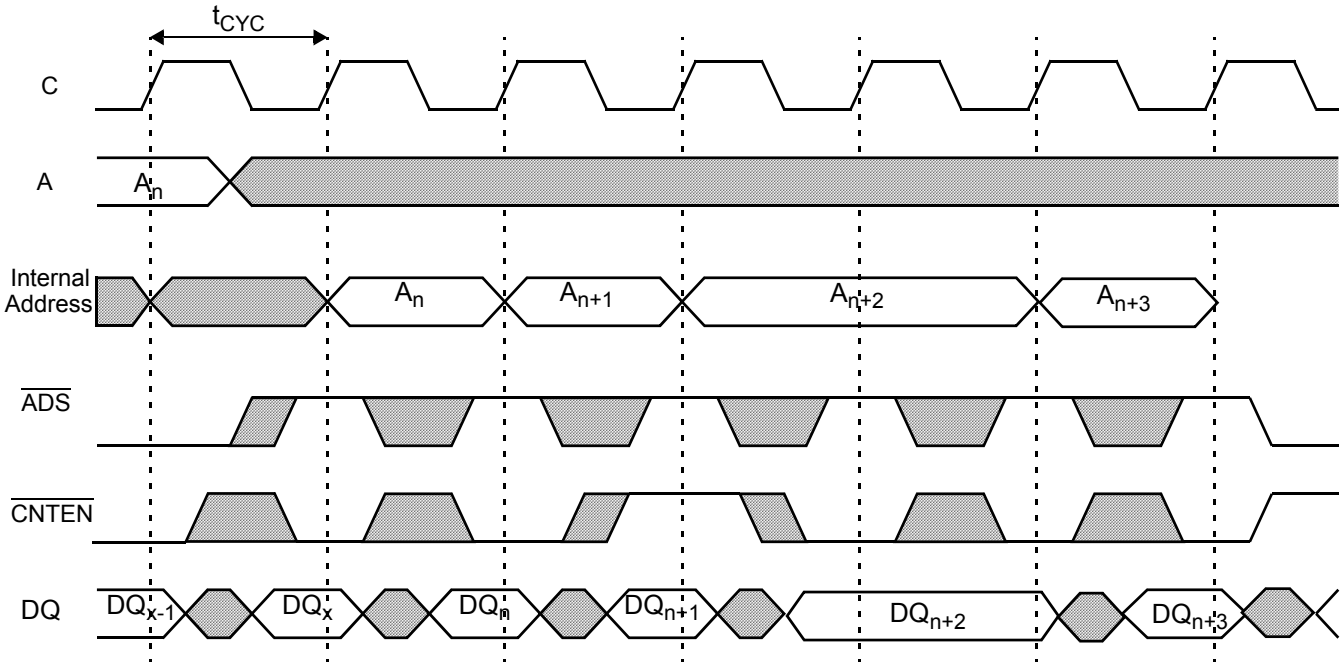


WRITE Cycle for Pipelined and Flow-Through Modes

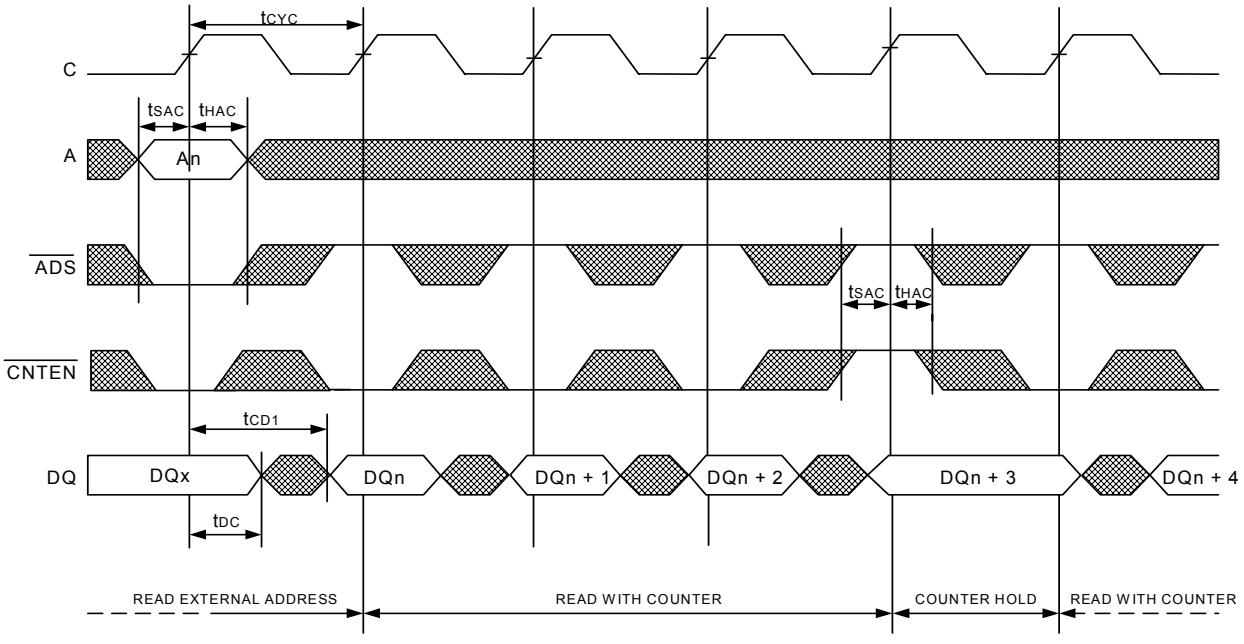


Switching Waveforms (continued)

READ with Address Counter Advance for Pipelined Mode

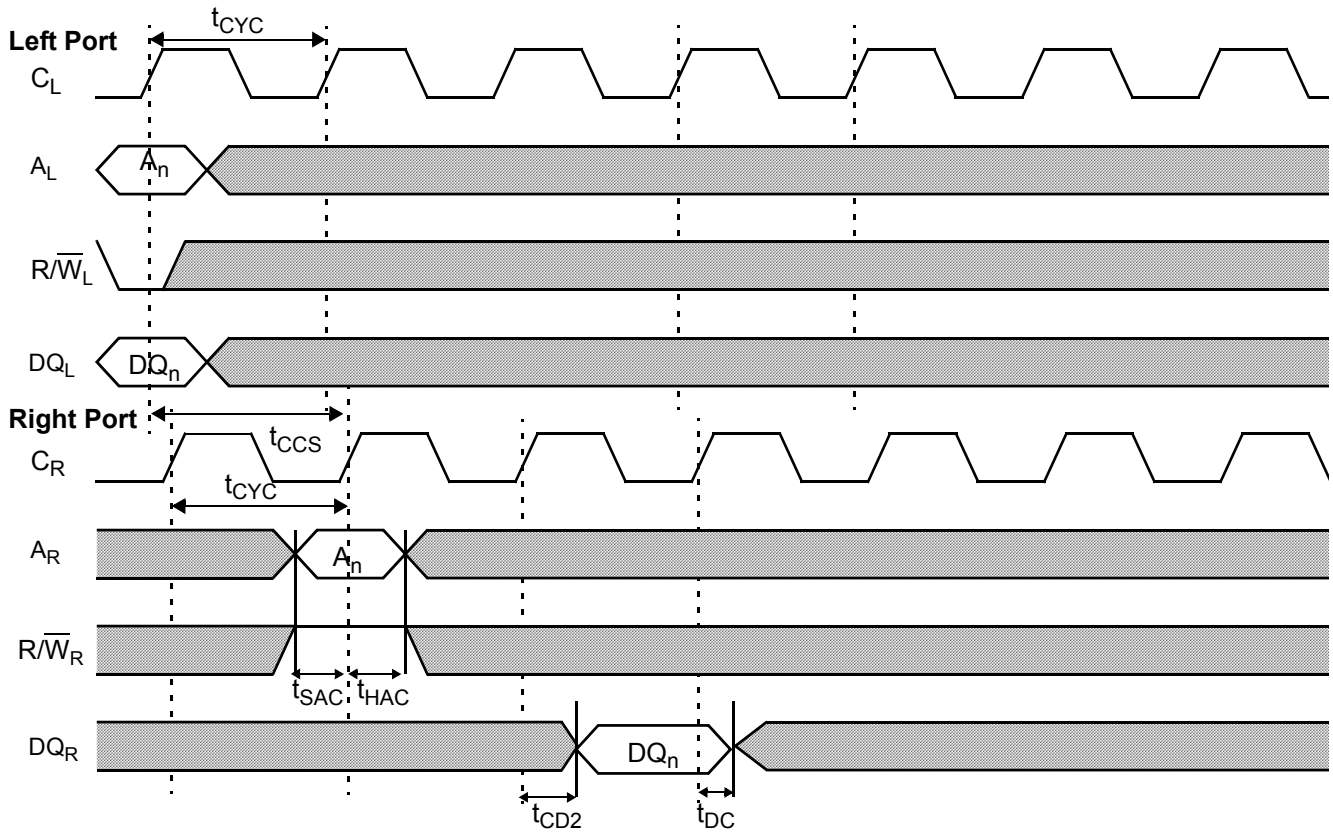


READ with Address Counter Advance for Flow-Through Mode

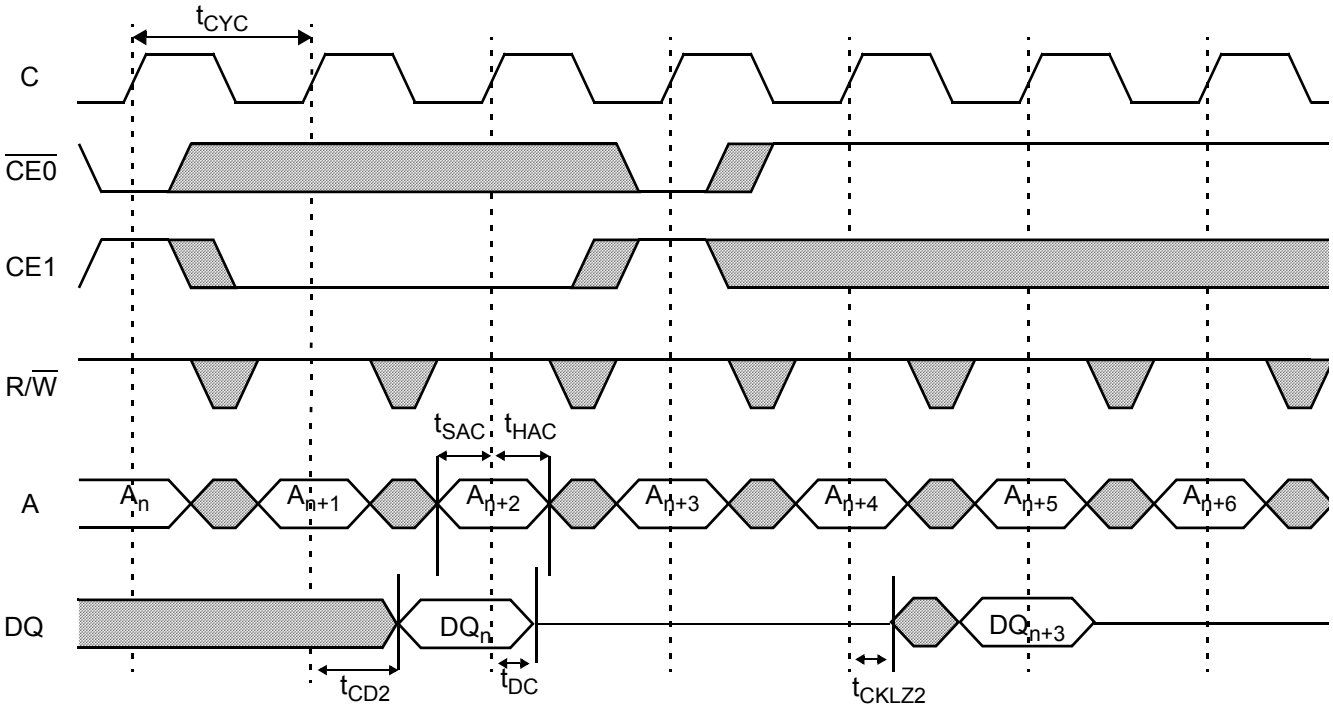


Switching Waveforms (continued)

Port-to-Port WRITE–READ for Pipelined Mode

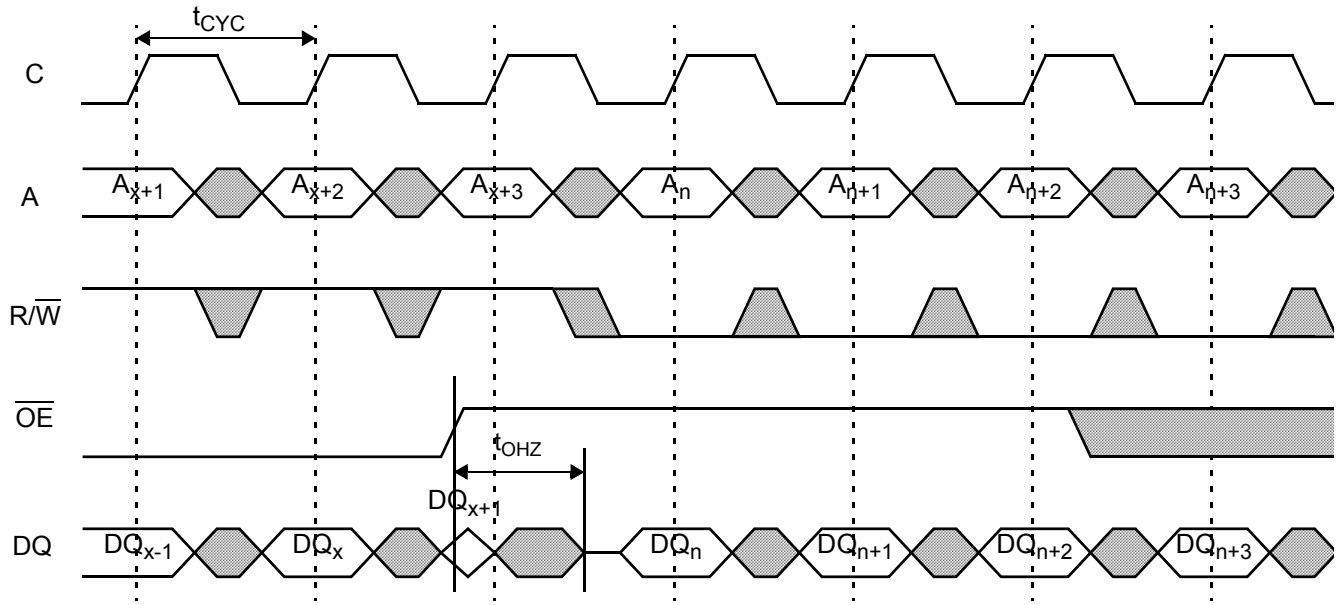


Chip Enable READ for Pipelined Mode

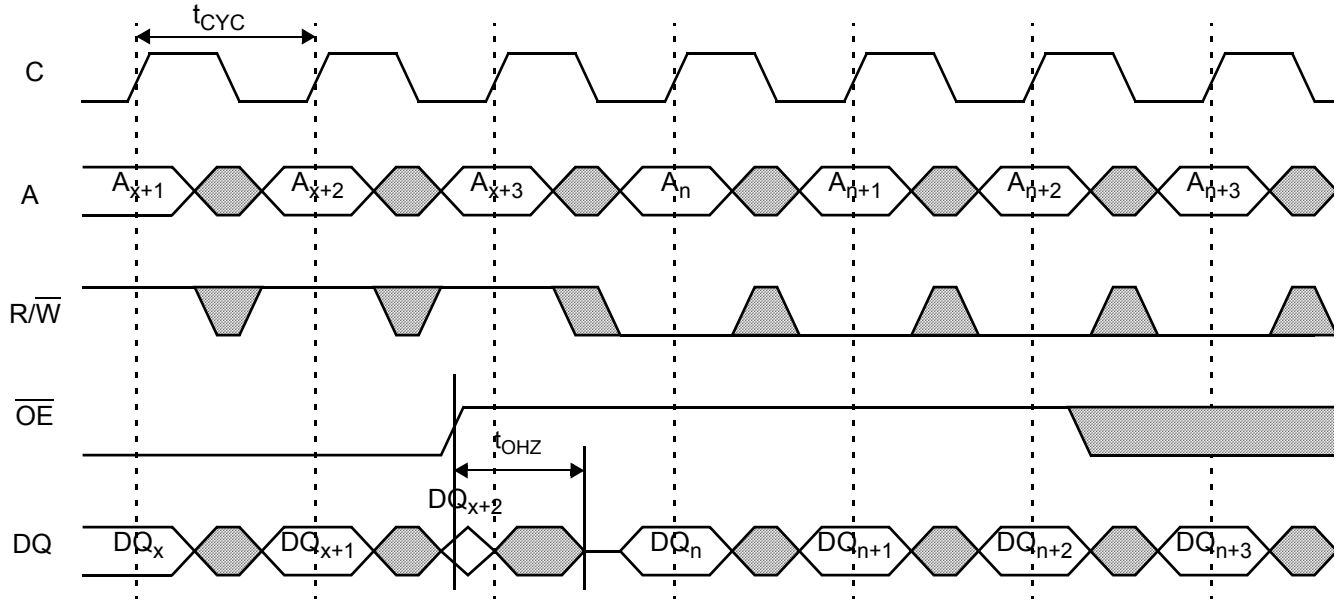


Switching Waveforms (continued)

OE Controlled WRITE for Pipelined Mode

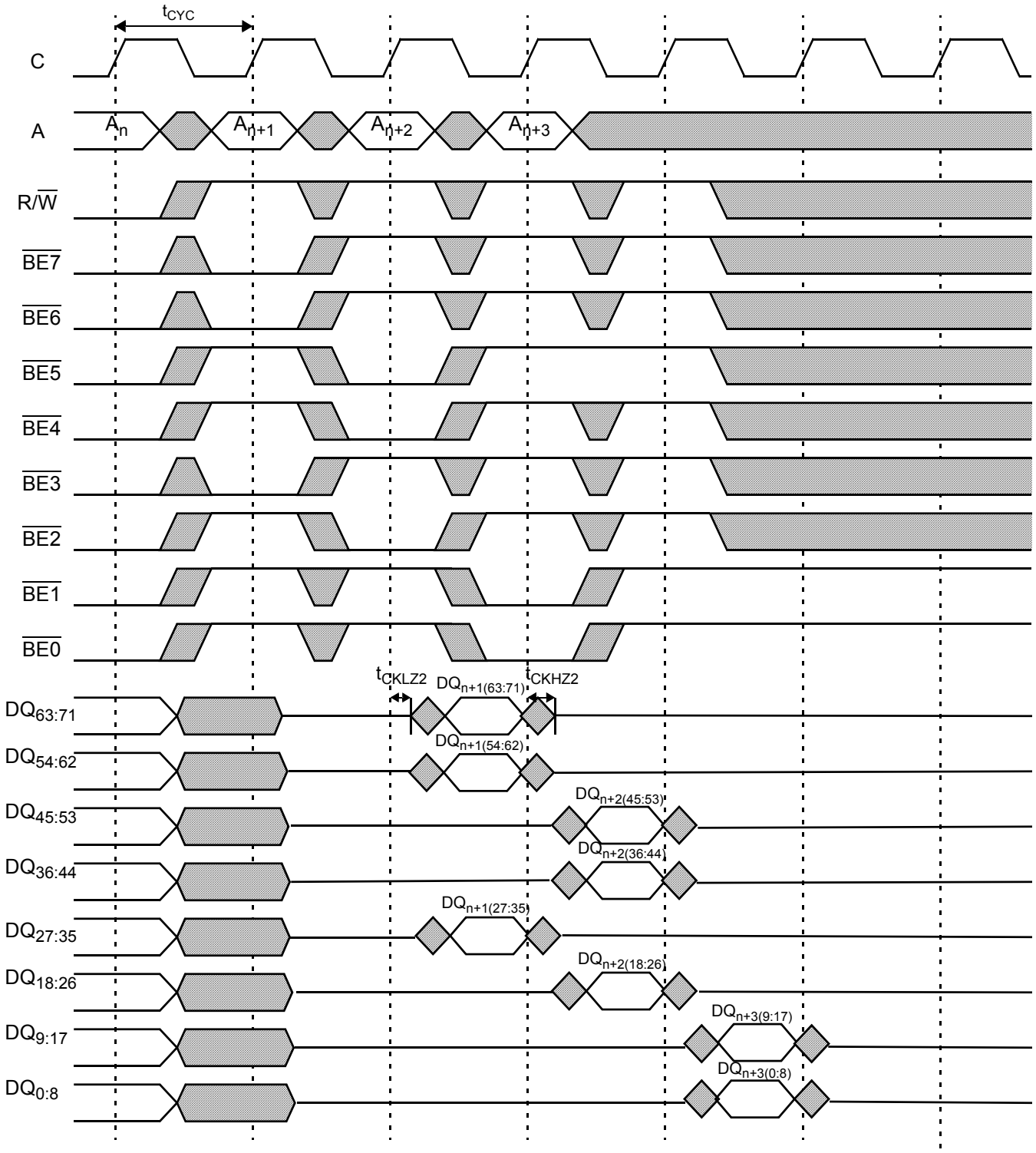


OE Controlled WRITE for Flow-Through Mode



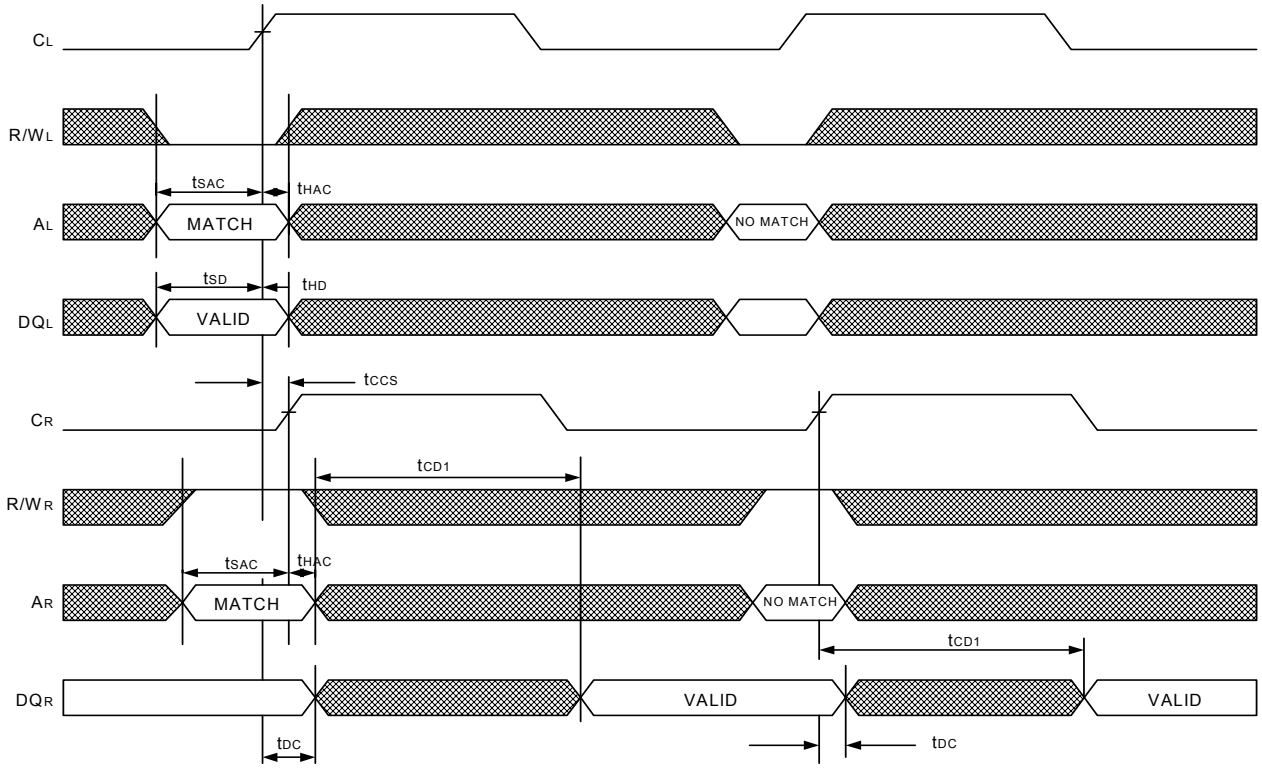
Switching Waveforms (continued)

Byte-Enable READ for Pipelined Mode

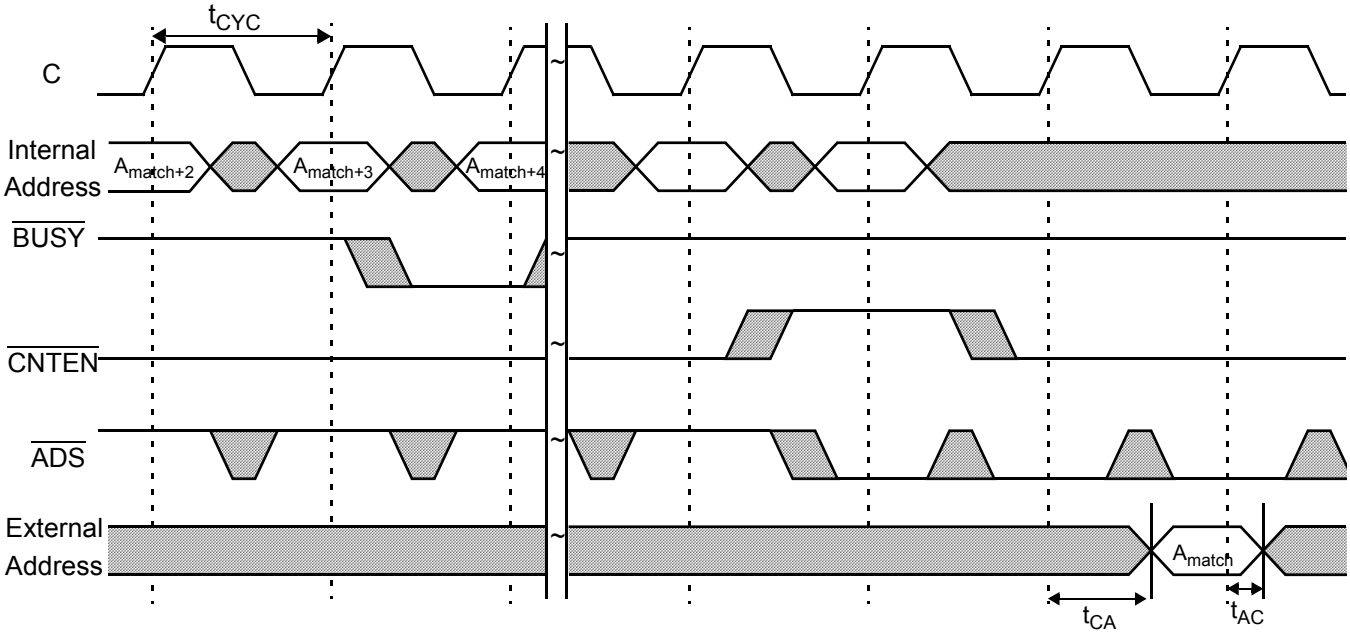


Switching Waveforms (continued)

Port-to-Port WRITE-to-READ for Flow-Through Mode



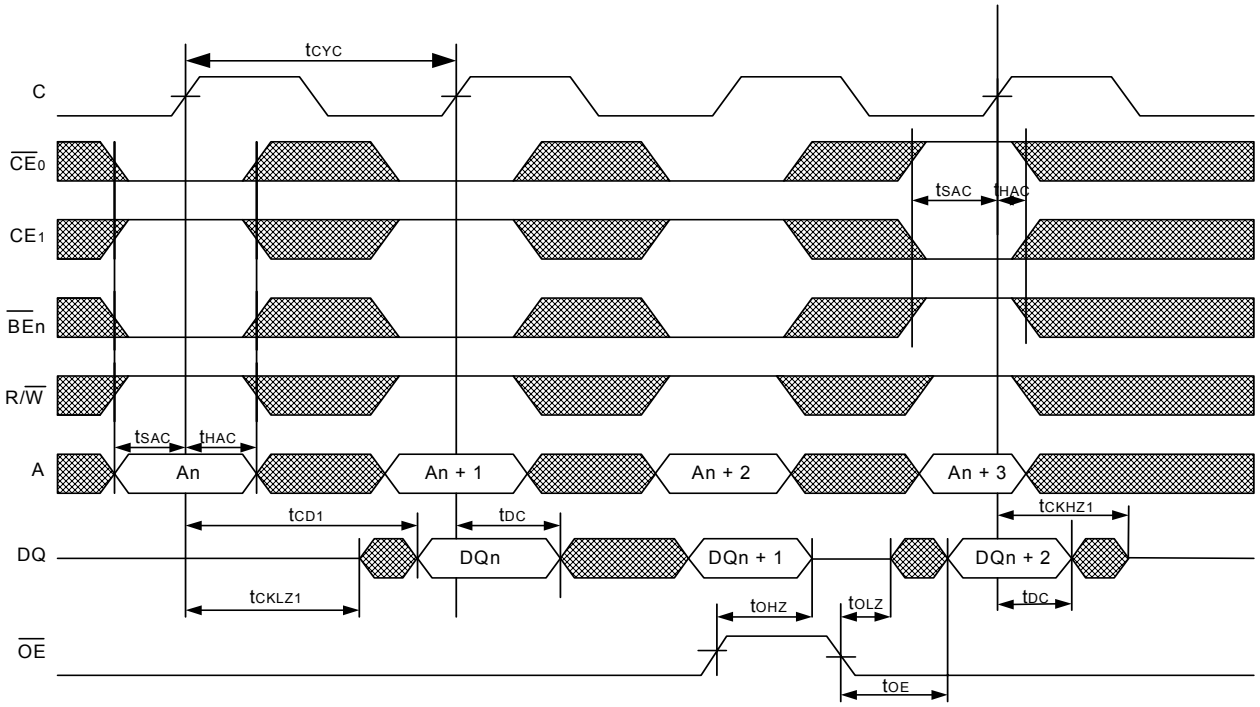
Busy Address Readback for Pipelined and Flow-Through Modes[36]



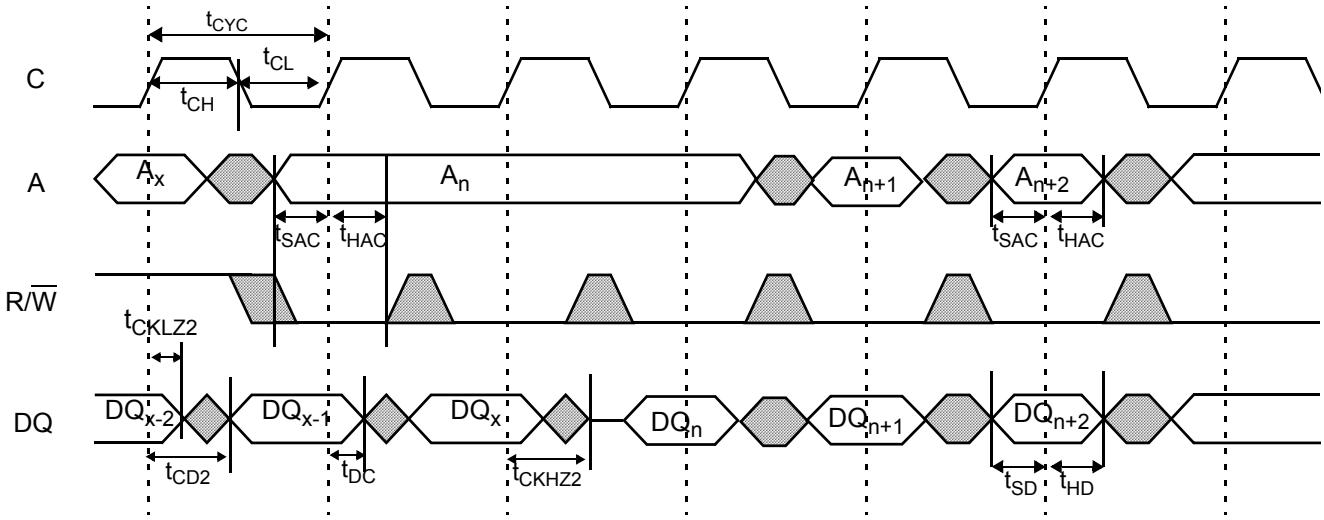
Note:
36. A_{match} is the matching address which will be reported on the address bus of the losing port. The counter operation selected for reporting the address is "Busy Address Readback."

Switching Waveforms (continued)

Read Cycle for Flow-Through Mode



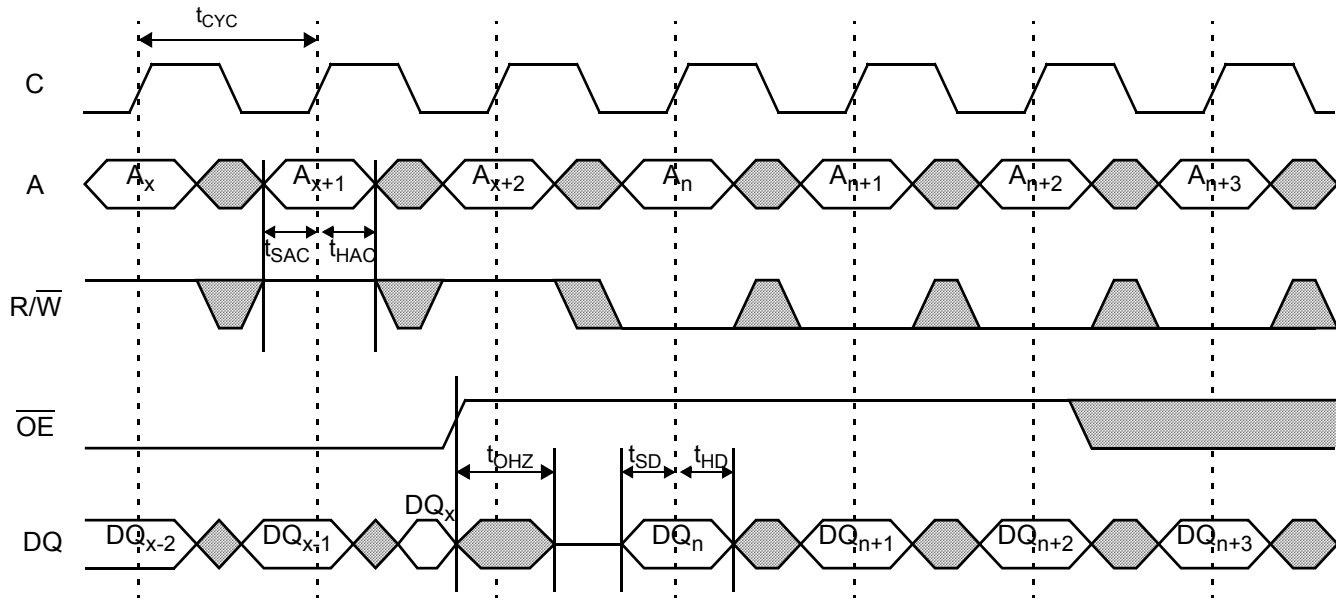
READ-to-WRITE for Pipelined Mode (OE = V_{IL})[37,38,39]



Notes:
37. When $\overline{OE}$ = V_{IL}, the last read operation is allowed to complete before the DQ bus is tri-stated and the user is allowed to drive write data.
38. Two dummy writes should be issued to accomplish bus turnaround. The 3rd instruction is the first valid write.
39. Chip enable or all byte enables should be held inactive during the two dummy writes to avoid data corruption.

Switching Waveforms (continued)

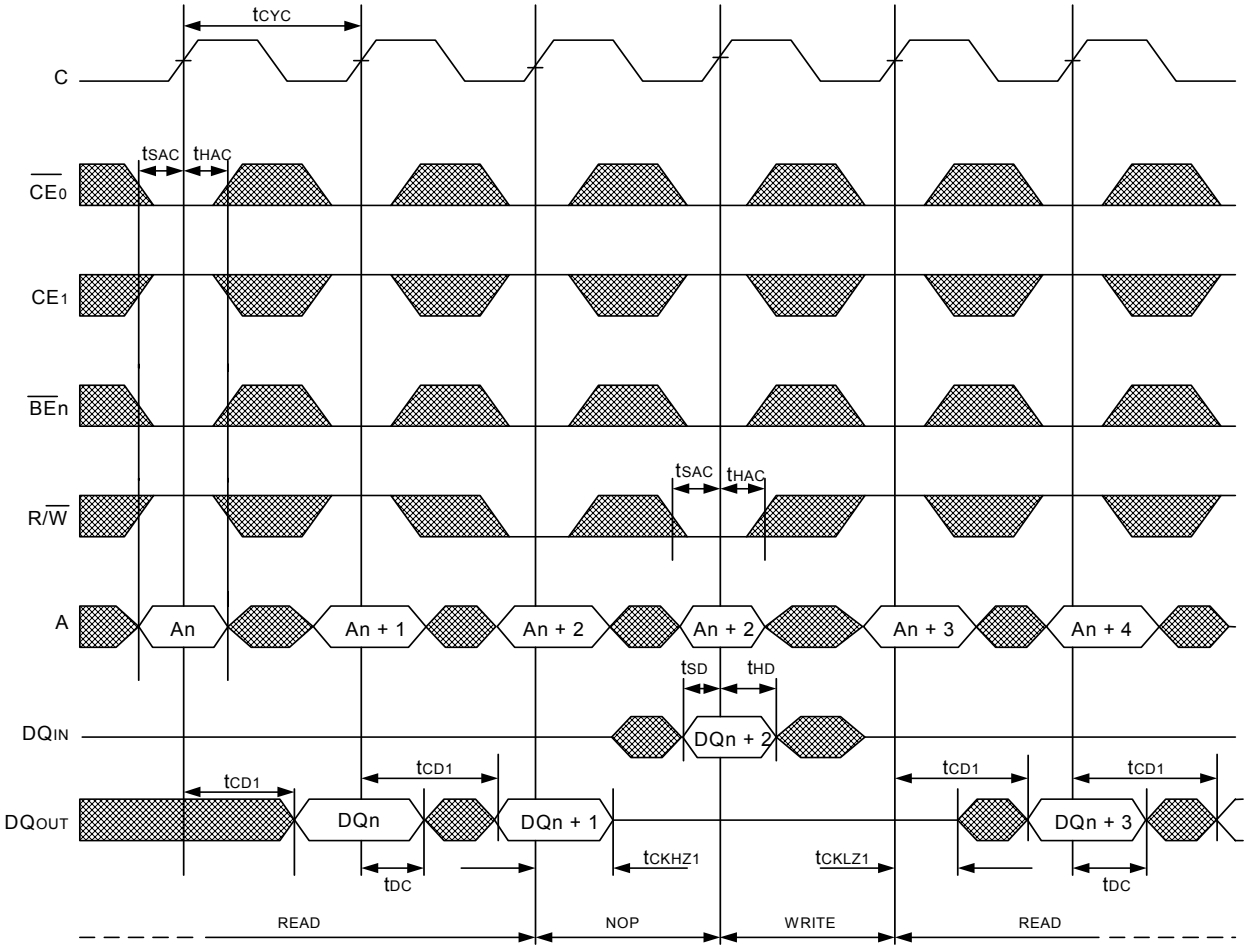
READ-to-WRITE for Pipelined Mode ($\overline{OE}$ Controlled)[40,41]



Notes:
40. $\overline{OE}$ should be deasserted and t_{OHZ} allowed to elapse before the first write operation is issued.
41. Any write scheduled to complete after $\overline{OE}$ is deasserted will be preempted.

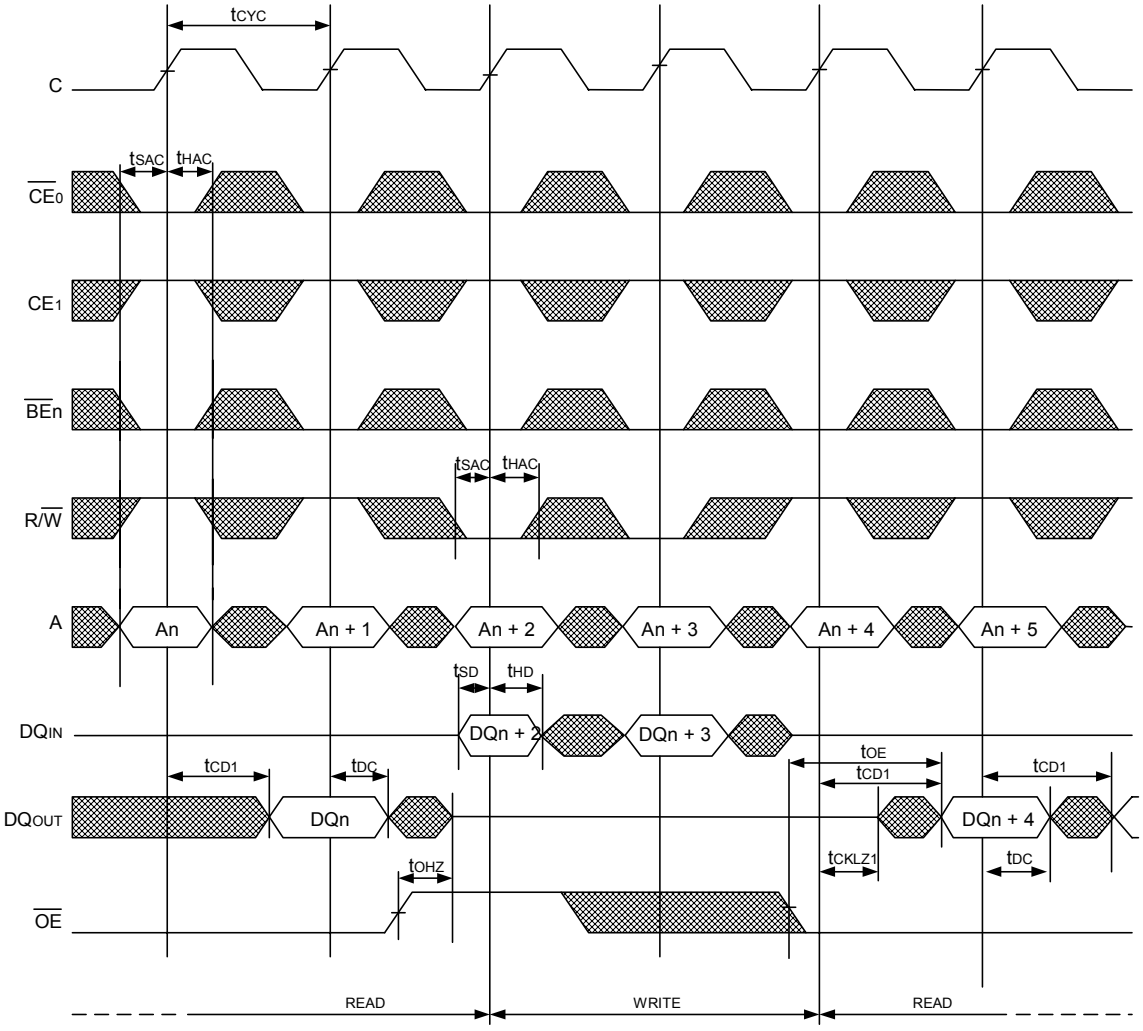
Switching Waveforms (continued)

Read-to-Write-to-Read for Flow-Through Mode ($\overline{OE}$ = LOW)



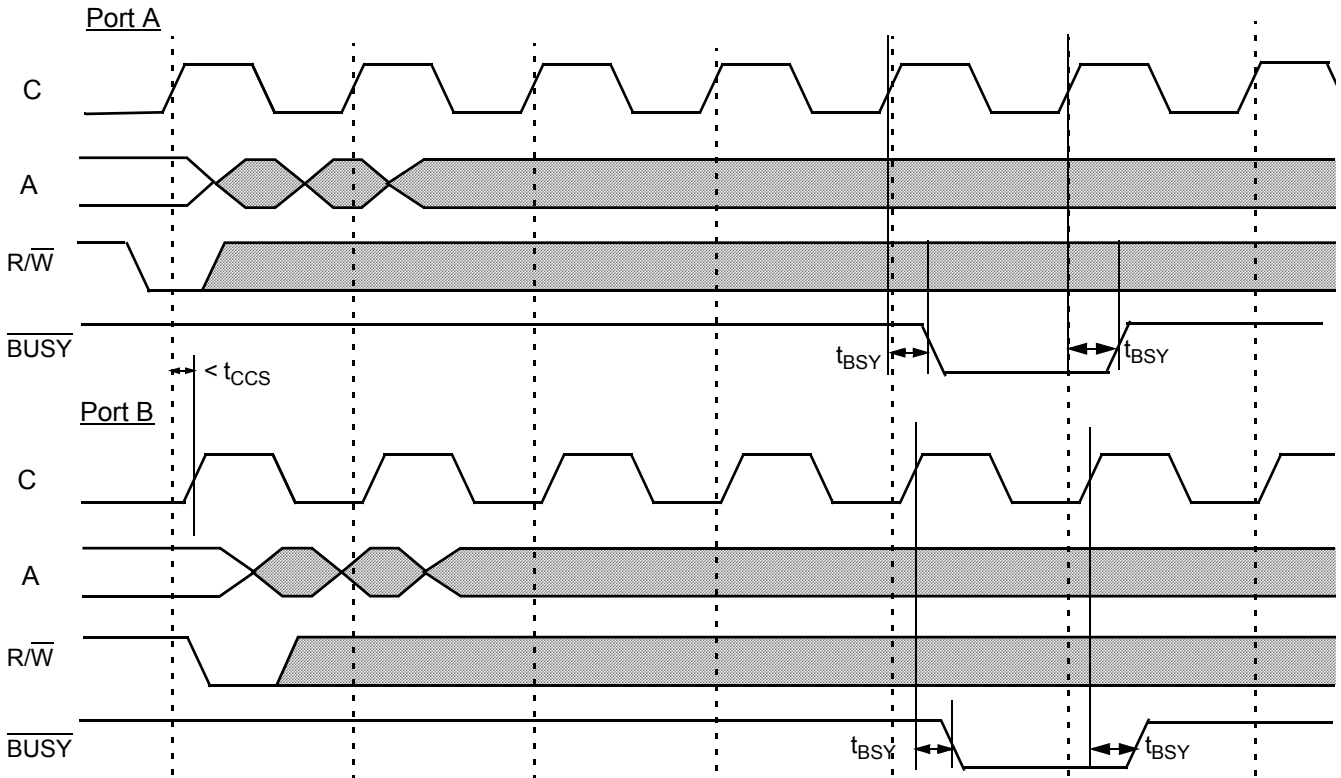
Switching Waveforms (continued)

Read-to-Write-to-Read for Flow-Through Mode ($\overline{OE}$ Controlled)

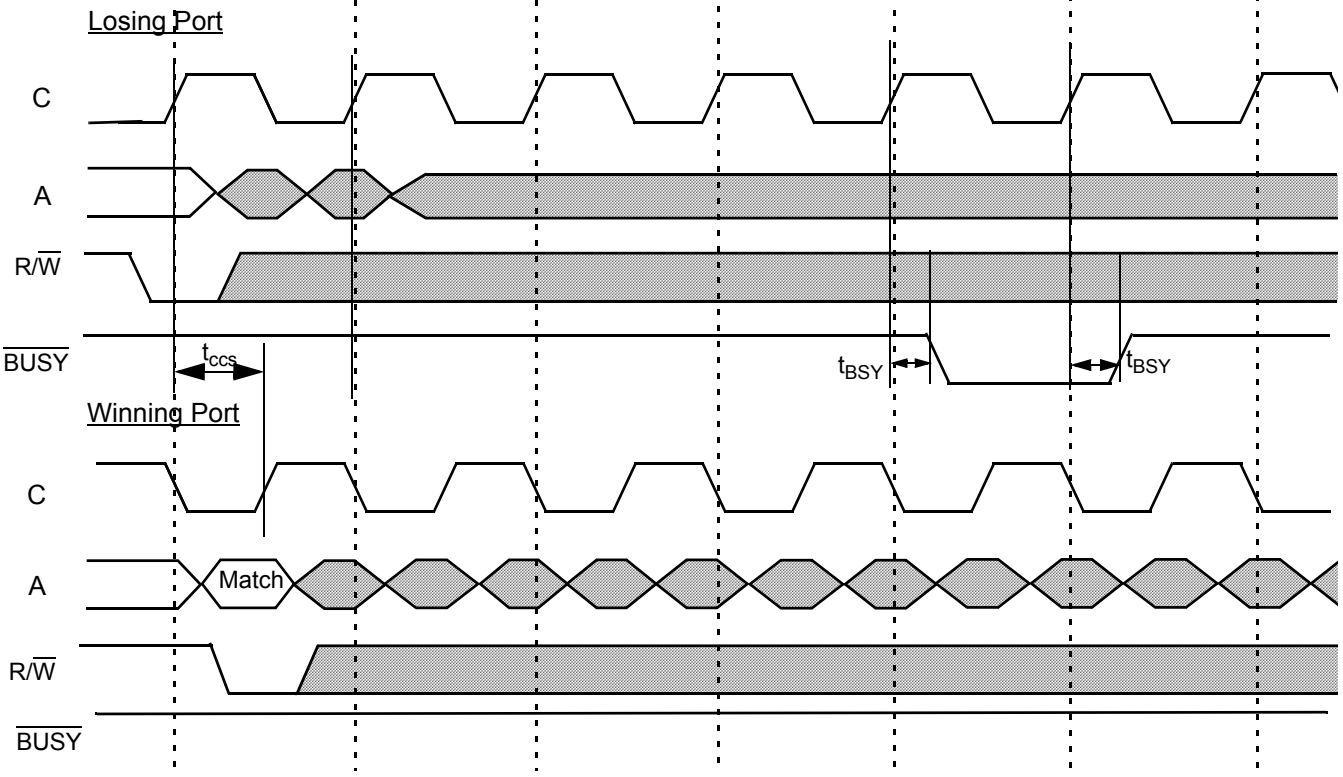


Switching Waveforms (continued)

BUSY Timing, WRITE-WRITE Collision for Pipelined and Flow-Through Modes, Clock Timing Violates t_{CCS}. (Flag Both Ports)

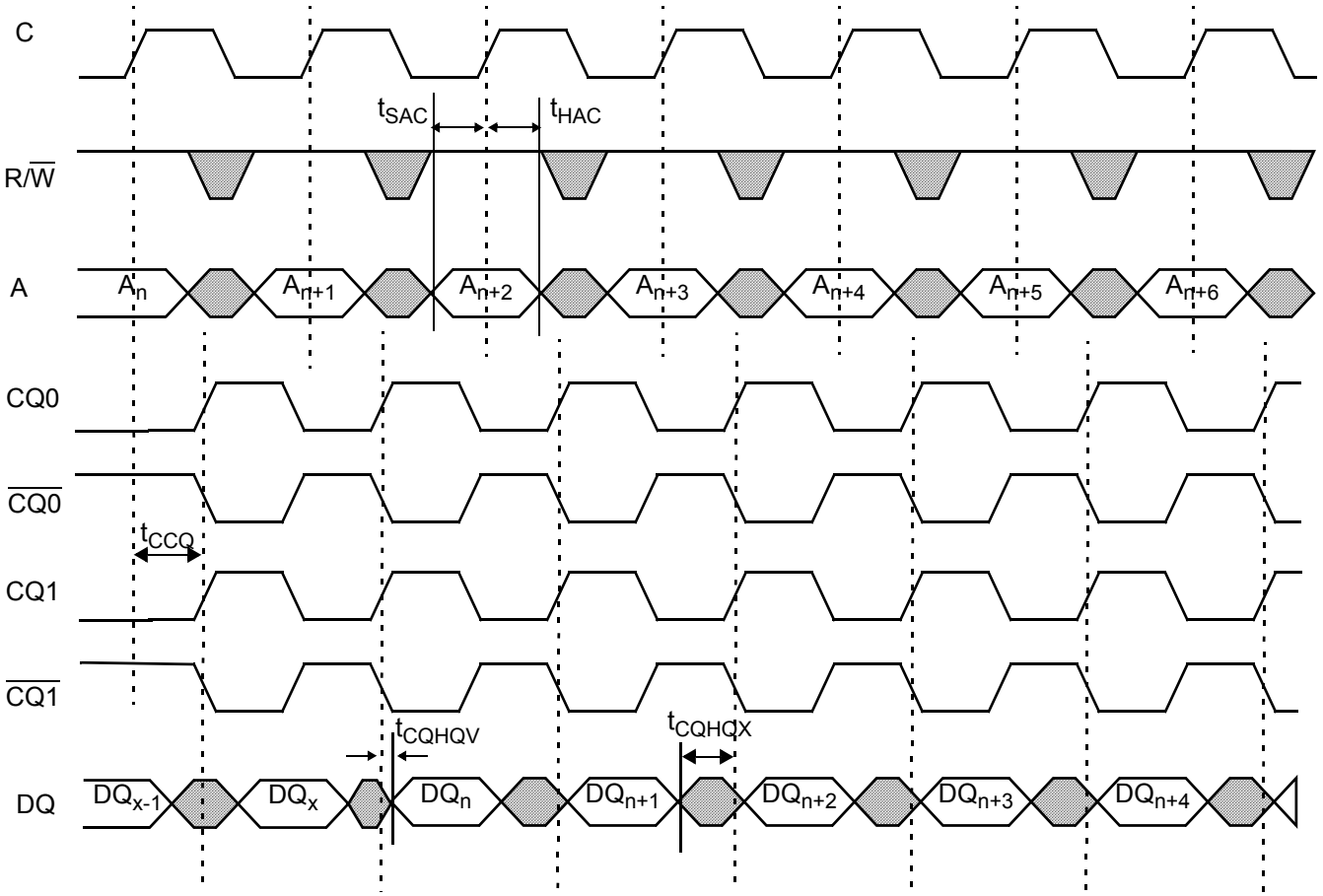


BUSY Timing, WRITE-WRITE Collision for Pipelined and Flow-Through Modes, Clock Timing Meets t_{CCS}. (Flag Losing Port)



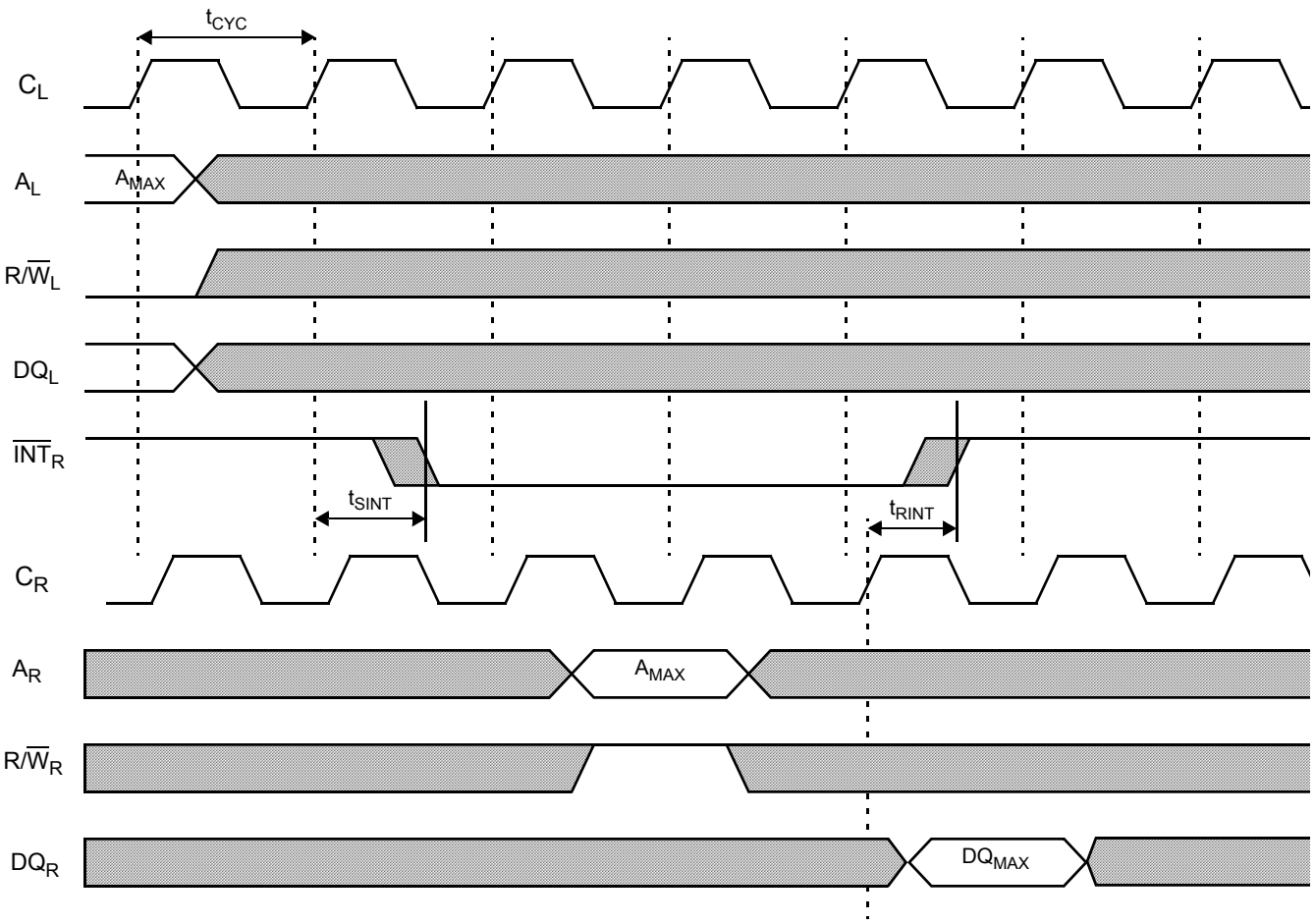
Switching Waveforms (continued)

Read with Echo Clock for Pipelined and Flow-Through Modes (CQEN = HIGH)



Switching Waveforms (continued)

Mailbox Interrupt Output



Ordering Information

512K × 72 (36 Mbit) 1.8V Synchronous CYD36S72V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYD36S72V18-200BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
167	CYD36S72V18-167BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD36S72V18-167BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial
133	CYD36S72V18-133BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD36S72V18-133BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial

256K × 72 (18 Mbit) 1.8V Synchronous CYD18S72V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD18S72V18-250BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
200	CYD18S72V18-200BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD18S72V18-200BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial
167	CYD18S72V18-167BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD18S72V18-167BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial

128K × 72 (9 Mbit) 1.8V Synchronous CYD09S72V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD09S72V18-250BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
200	CYD09S72V18-200BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD09S72V18-200BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial
167	CYD09S72V18-167BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD09S72V18-167BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial

64K × 72 (4 Mbit) 1.8V Synchronous CYD04S72V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD04S72V18-250BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
200	CYD04S72V18-200BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD04S72V18-200BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial
167	CYD04S72V18-167BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD04S72V18-167BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial

1024K × 36 (36 Mbit) 1.8V Synchronous CYD36S36V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYD36S36V18-200BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
167	CYD36S36V18-167BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD36S36V18-167BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial
133	CYD36S36V18-133BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD36S36V18-133BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial

Ordering Information (continued)

512K × 36 (18 Mbit) 1.8V Synchronous CYD18S36V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD18S36V18-250BBC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Commercial
200	CYD18S36V18-200BBC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD18S36V18-200BBI	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Industrial
167	CYD18S36V18-167BBC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD18S36V18-167BBI	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Industrial

256K × 36 (9 Mbit) 1.8V Synchronous CYD09S36V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD09S36V18-250BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
200	CYD09S36V18-200BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD09S36V18-200BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial
167	CYD09S36V18-167BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD09S36V18-167BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial

128K × 36 (4 Mbit) 1.8V Synchronous CYD04S36V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD04S36V18-250BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
200	CYD04S36V18-200BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD04S36V18-200BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial
167	CYD04S36V18-167BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD04S36V18-167BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial

2048K × 18 (36 Mbit) 1.8V Synchronous CYD36S18V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CYD36S18V18-200BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
167	CYD36S18V18-167BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD36S18V18-167BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial
133	CYD36S18V18-133BBC	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Commercial
	CYD36S18V18-133BBI	BY484	484-ball Grid Array 23 mm x 23 mm with 1.0 mm pitch (PBGA)	Industrial

1024K × 18 (18 Mbit) 1.8V Synchronous CYD18S18V18 Dual-Port SRAM

Speed MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD18S18V18-250BBC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Commercial
200	CYD18S18V18-200BBC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD18S18V18-200BBI	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Industrial
167	CYD18S18V18-167BBC	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD18S18V18-167BBI	BW256C	256-ball Grid Array 19 mm x 19 mm with 1.0 mm pitch (FBGA)	Industrial

Ordering Information (continued)

512K × 18 (9 Mbit) 1.8V Synchronous CYD09S18V18 Dual-Port SRAM

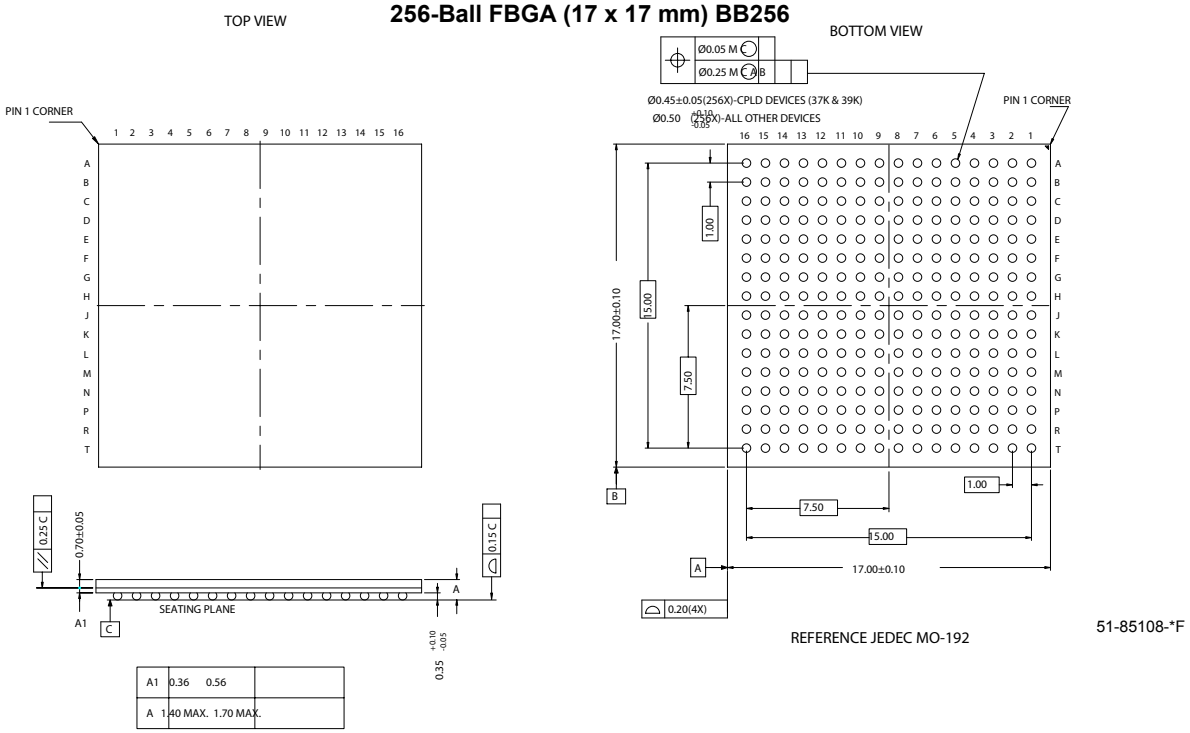
Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD09S18V18-250BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
200	CYD09S18V18-200BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD09S18V18-200BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial
167	CYD09S18V18-167BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD09S18V18-167BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial

256K × 18 (4 Mbit) 1.8V Synchronous CYD04S18V18 Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CYD04S18V18-250BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
200	CYD04S18V18-200BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD04S18V18-200BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial
167	CYD04S18V18-167BBC	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Commercial
	CYD04S18V18-167BBI	BB256	256-ball Grid Array 17 mm x 17 mm with 1.0 mm pitch (FBGA)	Industrial

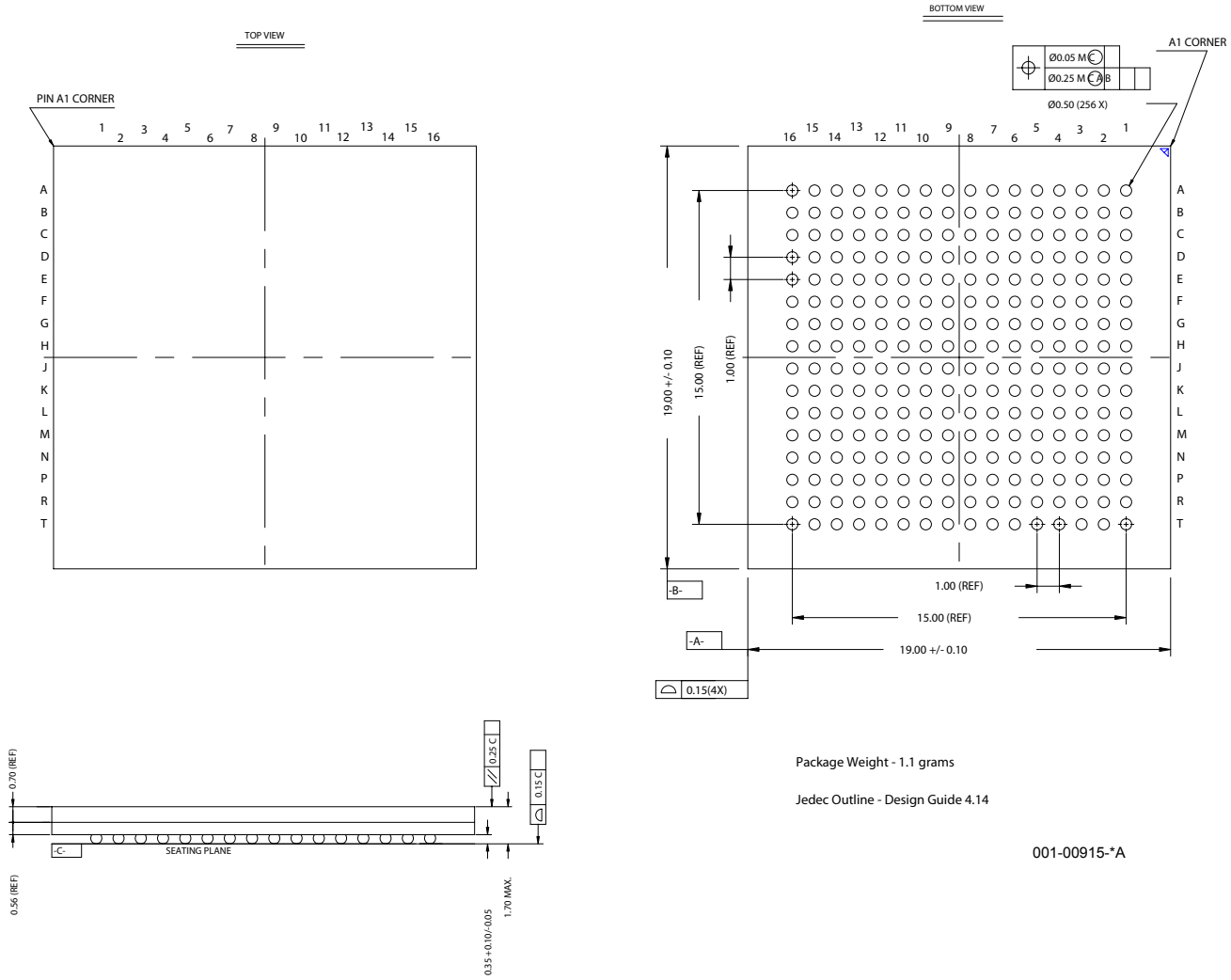
Package Diagrams

256-Ball FBGA (17 x 17 mm) BB256



Package Diagrams (continued)

256 FBGA (19 x 19 x 1.7 mm) BW256C



Package Weight - 1.1 grams

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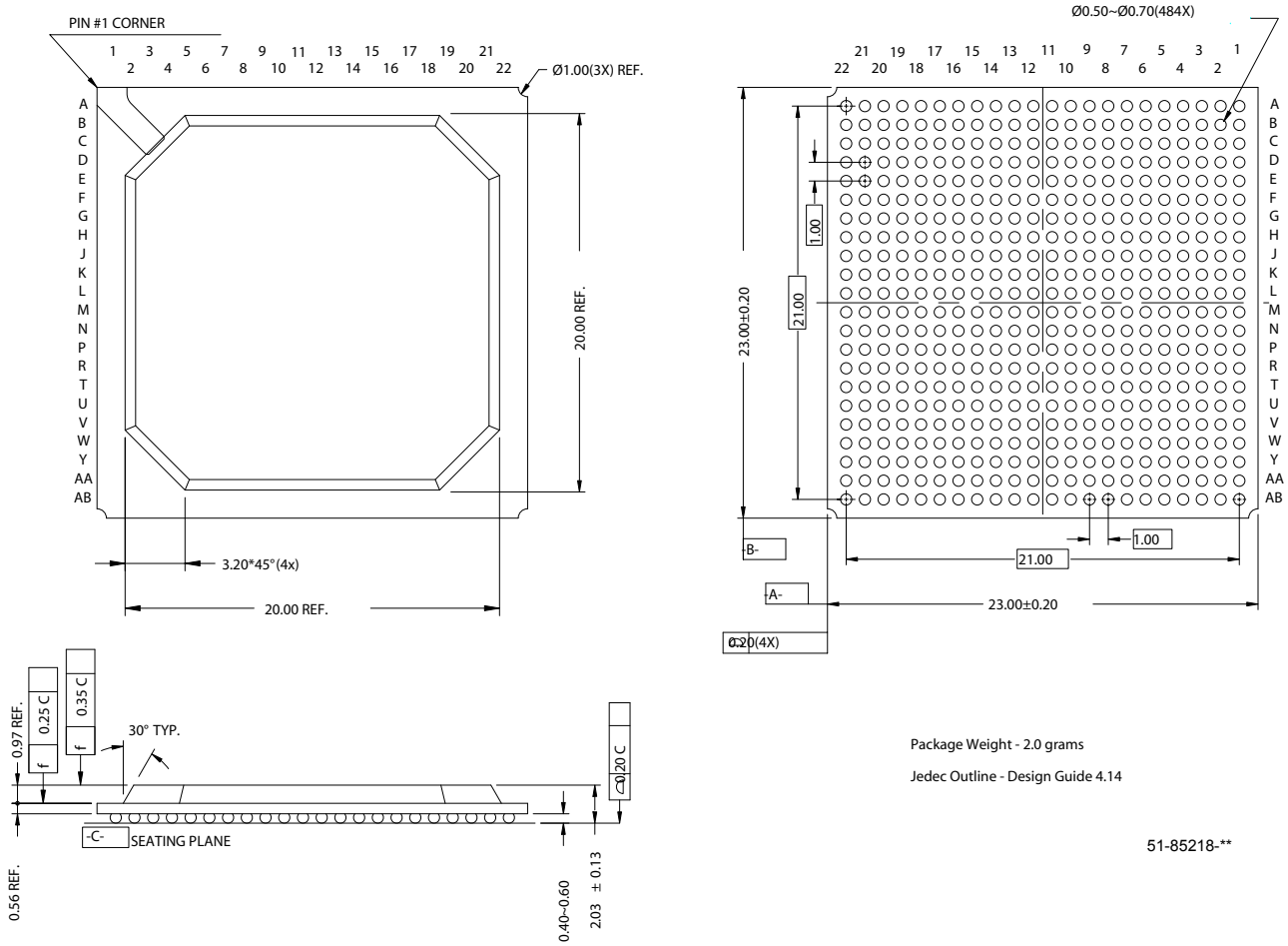
Package Diagrams (continued)

484-ball PBGA (23 mm x 23 mm x 2.03 mm) BY484



Document History Page

Document Title: FullFlex™ Synchronous SDR Dual-Port SRAM Document Number: 38-06082				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	302411	See ECN	YDT	New data sheet
*A	334036	See ECN	YDT	Corrected typo on page 1 Reproduced PDF file to fix formatting errors
*B	395800	See ECN	SPN	Added statement about no echo clocks for flow-through mode Updated electrical characteristics Added note 16 and 17 (1.5V timing) Added note 33 (timing for x18 devices) Updated input edge rate (note 34) Updated table 5 on deterministic access control logic Added description of busy readback in deterministic access control section Changed dummy write descriptions Updated ZQ pins connection details Updated note 24, B0 to BE0 Added power supply requirements to $\overline{MRST}$ and VC_SEL Added note 4 (VIM disable) Updated supply voltage to ground potential to 4.1V Updated parameters on table 15 Updated and added parameters to table 16 Updated x72 pinout to SDR only pinout Updated 484 PBGA pin diagram Updated the pin definition of $\overline{MRST}$ Updated the pin definition of VC_SEL Updated $\overline{READY}$ description to include Wired OR note Updated master reset to include wired OR note for $\overline{READY}$ Updated minimum V_{OH} value for the 1.8V LVCMOS configuration Updated electrical characteristics to include I_{OH} and I_{OL} values Updated electrical characteristics to include $\overline{READY}$ Added I_{IX3} Updated maximum input capacitance Added Note 33 Added Note 34 Removed Notes 15 and 17 Updated Pin Definitions for CQ0, $\overline{CQ0}$, CQ1, and $\overline{CQ1}$ Removed -100 Speed bin from Table.1 Selection Guide Changed voltage name from V_{DDQ} to V_{DDIO} Changed voltage name from V_{DD} to V_{CORE} Moved the Mailbox Interrupt Timing Diagram to be the final timing diagram Updated the Package Type for the CYD36S18V18 parts Updated the Package Type for the CYD36S18V18 parts Updated the Package Type for the CYD18S18V18 parts Updated the Package Type for the CYD18S36V18 parts Included the Package Diagram for the 256-Ball FBGA (19 x 19 mm) BW256 Included an OE Controlled Write for Flow-Through Mode Switching Waveform Included a Read with Echo Clock Switching Waveform Updated Figure 5 and Figure 6 Updated Electrical Characteristics for $\overline{READY}$ V_{OH} and $\overline{READY}$ V Updated Electrical Characteristics for V_{OH} and V_{OL} for the -167 and -133 speeds Included a Unit column for Table 5 Removed Switching Characteristic t_{CA} from chart Included t_{OHZ} in Switching Waveform $\overline{OE}$ Controlled Write for Pipelined Mode Included t_{CKLZ2} in Waveform Read-to-Write-to-Read for Flow-Through Mode
*C	402238	SEE ECN	KGH	Updated AC Test Load and Waveforms Included FullFlex36 SDR 484-ball BGA Pinout (Top View) Included FullFlex18 SDR 484-ball BGA Pinout (Top View) Included Timing Parameter t_{CORDY}