Harris
SEMICONDUCTOR

CD54HC4051,
CD74HC4051, CD74HCT4051,
CD74HC4052, CD74HCT4052,
CD74HC4053, CD74HCT4053

High Speed CMOS Logic
Analog Multiplexers/Demultiplexers

November 1997

Features

- **Wide Analog Input Voltage Range** . . . . $\pm$5V Max
- **Low "On" Resistance**
  - 70Ω Typical (V_{CC} - V_{EE} = 4.5V)
  - 40Ω Typical (V_{CC} - V_{EE} = 9V)
- **Low Crosstalk between Switches**
- **Fast Switching and Propagation Speeds**
- **"Break-Before-Make" Switching**
- **Wide Operating Temperature Range** . . -55°C to 125°C
- **CD54HC/CD74HC Types**
  - Operation Control Voltage . . . . 2V to 6V
  - Switch Voltage . . . . 0V to 10V
  - High Noise Immunity . . . N_{IL} = 30%, N_{IH} = 30% of V_{CC}, V_{CC} = 5V
- **CD545HCT/CD74HCT Types**
  - Operation Control Voltage . . . . 4.5V to 5.5V
  - Switch Voltage . . . . 0V to 10V
  - Direct LSTTL Input
    Logic Compatibility . . . V_{IL} = 0.8V Max, V_{IH} = 2V Min
  - CMOS Input Compatibility . . . . . $I_I \leq 1\mu$A at V_{OL}, V_{OH}

Description

The Harris CD54HC4051, CD54HCT4051, CD74HC4051, CD74HCT4051 are digitally controlled analog switches which utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e. V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, all three devices have an enable control which, when high, disables all switches to their "off" state.
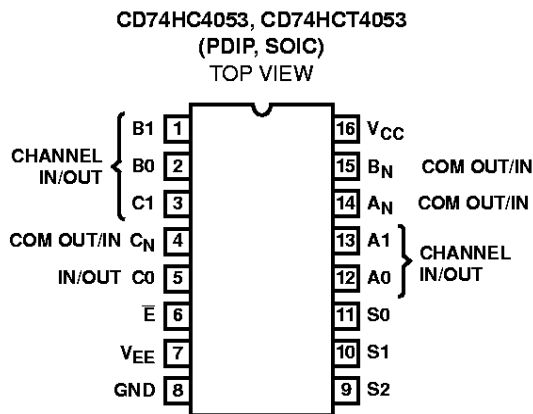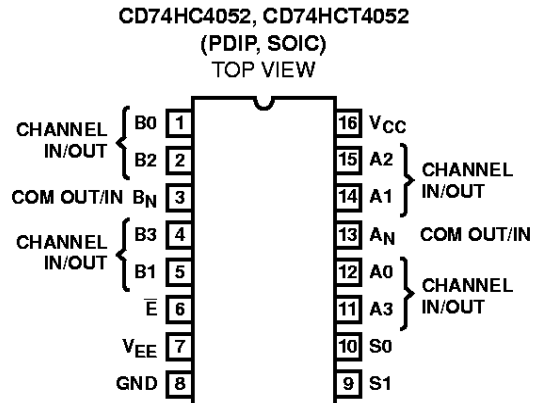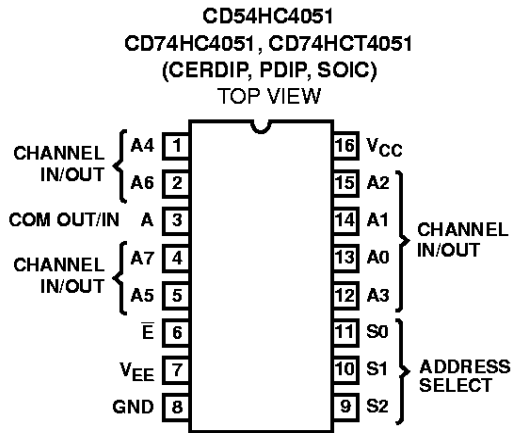
Ordering Information

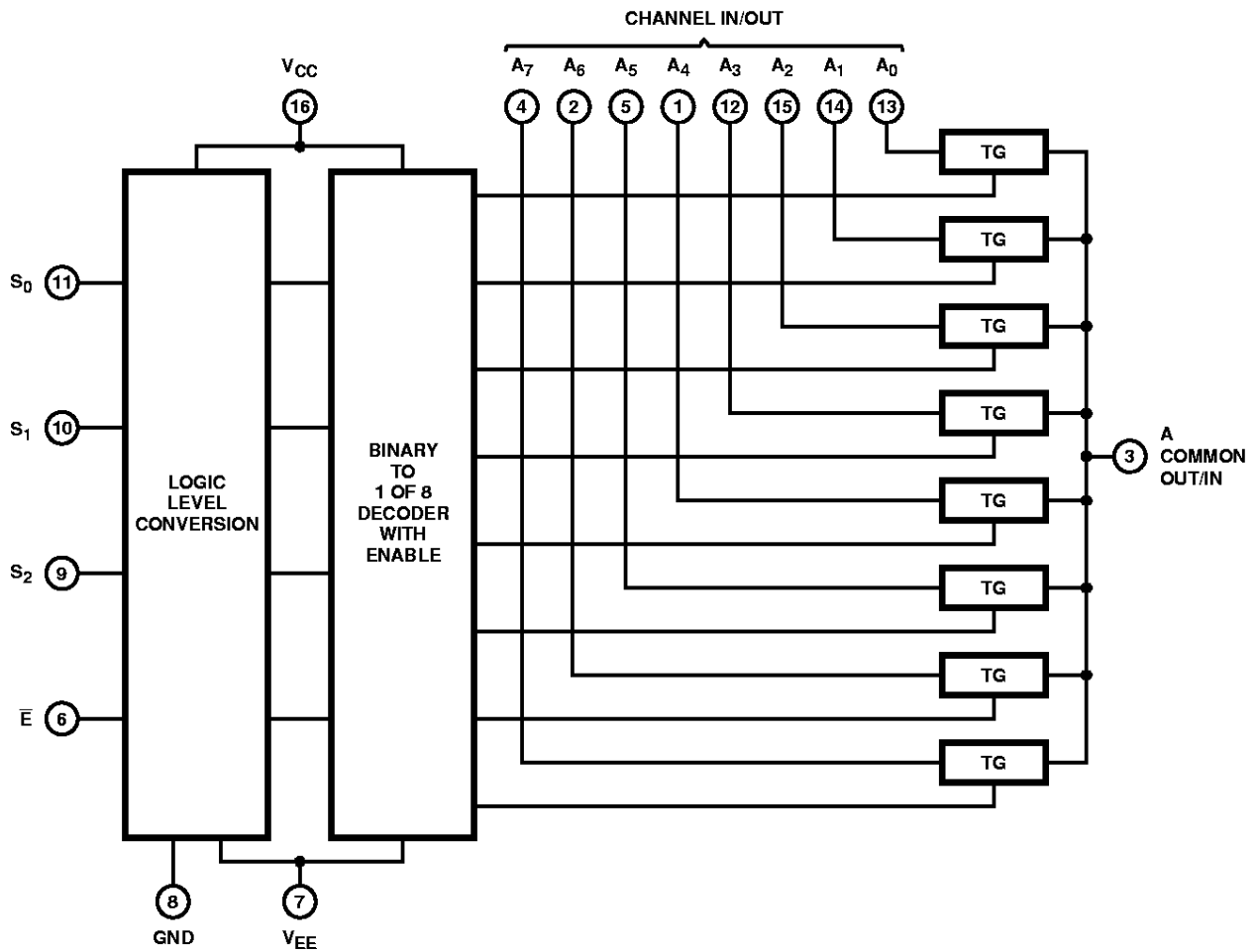| PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD54HC4051F	-55 to 125	16 Ld CERDIP	F16.3
CD74HC4051E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4052E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4053E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT4051E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT4052E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT4053E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4051M	-55 to 125	16 Ld SOIC	M16.15
CD74HC4052M	-55 to 125	16 Ld SOIC	M16.15
CD74HC4053M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4051M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4052M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4053M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4052SM	-55 to 125	16 Ld SSOP	M16.15A

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer or die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

File Number **1676.1**

Pinouts

CD54HC4051
CD74HC4051, CD74HCT4051
(CERDIP, PDIP, SOIC)
TOP VIEW

```
CHANNEL   { A4  [1]        [16]  Vcc
IN/OUT    { A6  [2]        [15]  A2 }
COM OUT/IN  A   [3]        [14]  A1 }  CHANNEL
CHANNEL   { A7  [4]        [13]  A0 }  IN/OUT
IN/OUT    { A5  [5]        [12]  A3 }
            E̅   [6]        [11]  S0 }
            VEE [7]        [10]  S1 }  ADDRESS
            GND [8]        [9]   S2 }  SELECT
```

CD74HC4052, CD74HCT4052
(PDIP, SOIC)
TOP VIEW

```
CHANNEL   { B0  [1]        [16]  Vcc
IN/OUT    { B2  [2]        [15]  A2 }  CHANNEL
COM OUT/IN  BN  [3]        [14]  A1 }  IN/OUT
CHANNEL   { B3  [4]        [13]  AN    COM OUT/IN
IN/OUT    { B1  [5]        [12]  A0 }  CHANNEL
            E̅   [6]        [11]  A3 }  IN/OUT
            VEE [7]        [10]  S0
            GND [8]        [9]   S1
```

CD74HC4053, CD74HCT4053
(PDIP, SOIC)
TOP VIEW

```
CHANNEL   { B1  [1]        [16]  Vcc
IN/OUT    { B0  [2]        [15]  BN    COM OUT/IN
          { C1  [3]        [14]  AN    COM OUT/IN
COM OUT/IN  CN  [4]        [13]  A1 }  CHANNEL
IN/OUT      C0  [5]        [12]  A0 }  IN/OUT
            E̅   [6]        [11]  S0
            VEE [7]        [10]  S1
            GND [8]        [9]   S2
```

Functional Diagram of HC/HCT4051

CHANNEL IN/OUT

A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0

V_{CC}
(16)

(4) (2) (5) (1) (12) (15) (14) (13)

TG

TG

S_0 (11)

TG

LOGIC
LEVEL
CONVERSION

BINARY
TO
1 OF 8
DECODER
WITH
ENABLE

TG

S_1 (10)

TG

(3) A
COMMON
OUT/IN

S_2 (9)

TG

TG

$\overline{E}$ (6)

TG

(8)
GND

(7)
V_{EE}

TRUTH TABLE
CD54/74HC/HCT4051

INPUT STATES				"ON" CHANNELS
ENABLE	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

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Functional Diagram of HC/HCT4052
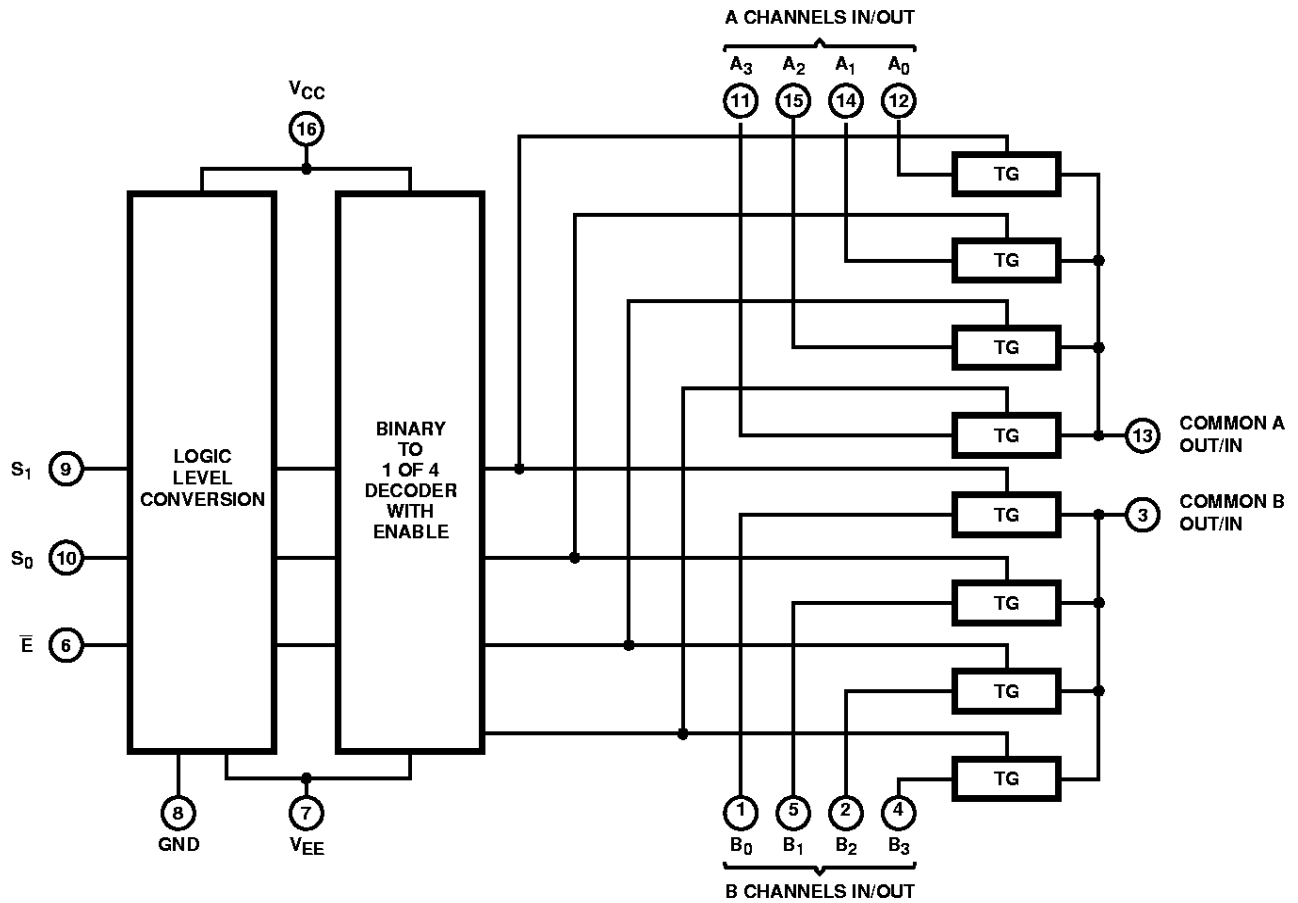
TRUTH TABLE
CD74HC4052, CD74HCT4052

INPUT STATES			"ON" CHANNELS
ENABLE	S_1	S_0	
L	L	L	A0, B0
L	L	H	A1, B1
L	H	L	A2. B2
L	H	H	A3, B3
H	X	X	None

X = Don't care

Functional Diagram of HC/HCT4053
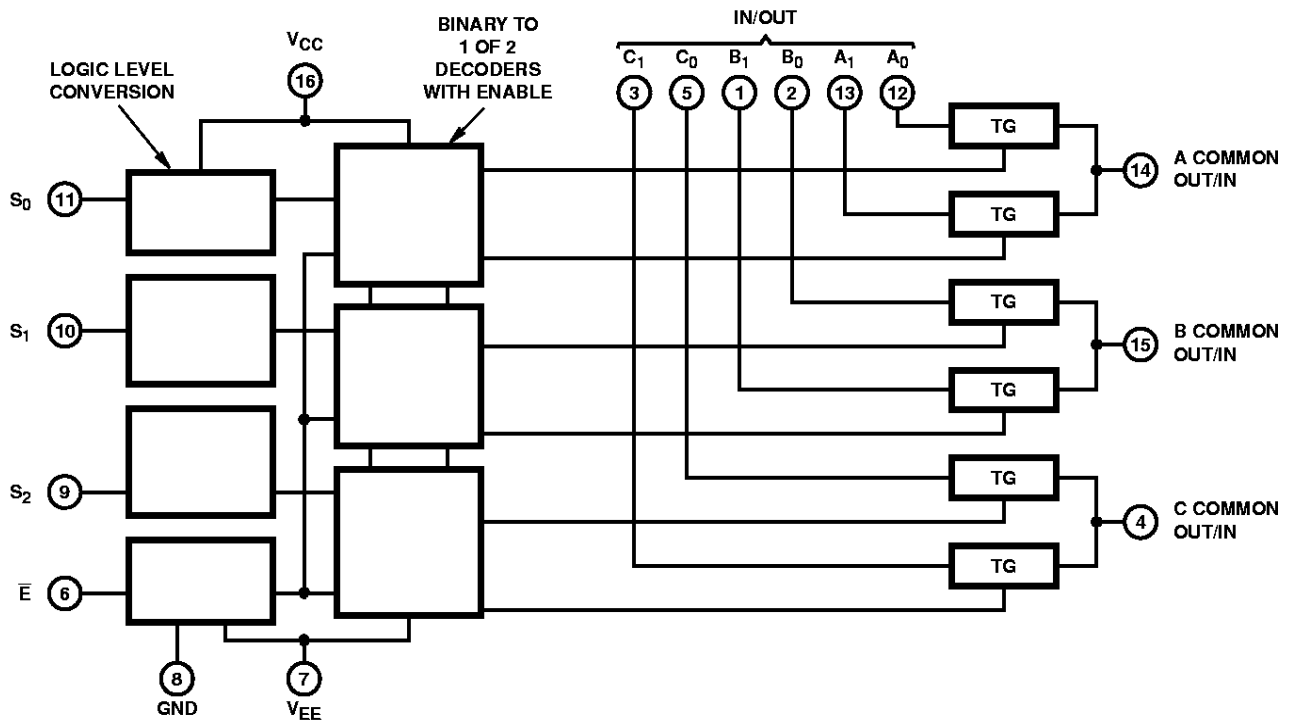
TRUTH TABLE
CD74HC4053, CD74HCT4053

INPUT STATES				"ON" CHANNELS
ENABLE	S_0	S_1	S_2	
L	L	L	L	C0, B0, A0
L	H	L	L	C0, B0, A1
L	L	H	L	C0, B1, A0
L	H	H	L	C0, B1, A1
L	L	L	H	C1, B0, A0
L	H	L	H	C1, B0, A1
L	L	H	H	C1, B1, A0
L	H	H	H	C1, B1, A1
H	X	X	X	None

X = Don't care

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Absolute Maximum Ratings (Note 3)

DC Supply Voltage, V_{CC} - V_{EE} . . . . -0.5V to 10.5V
DC Supply Voltage, V_{CC}. . . . . -0.5V to +7V
DC Supply Voltage, V_{EE} . . . . +0.5V to -7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . .±20mA
DC Switch Diode Current, I_{OK}
  For V_I < V_{EE} -0.5V or V_I > V_{CC} + 0.5V . . . .±20mA
DC Switch Current, (Note 2)
  For V_I > V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . .±25mA
DC V_{CC} or Ground Current, I_{CC} . . . .±50mA
DC V_{EE} Current, I_{EE} . . . . -20mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package	90	N/A
SOIC Package.	160	N/A
CERDIP Package	130	55

Maximum Junction Temperature . . . . .150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . .300°C

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

PARAMETER	MIN	MAX	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range), V_{CC} (Note 5)			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
Supply Voltage Range (For T_A = Full Package Temperature Range), V_{CC} - V_{EE} CD54/74HC Types, CD54/74HCT Types (See Figure 1)	2	10	V
Supply Voltage Range (For T_A = Full Package Temperature Range), V_{EE} (Note 5) CD54/74HC Types, CD54/74HCT Types (See Figure 2)	0	-6	V
DC Input Control Voltage, V_I	GND	V_{CC}	V
Analog Switch I/O Voltage, V_{IS}	V_{EE}	V_{CC}	V
Operating Temperature, T_A	-55	125	^{o}C
Input Rise and Fall Times, t_r, t_f			
2V	0	1000	ns
4.5V	0	500	ns
6V	0	400	ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. All voltages referenced to GND unless otherwise specified.

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

5. In certain applications, the external load resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{ON} values shown in Electrical Specifications table). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4051; terminals 3 and 13 on the HC/HCT4052; terminals 4, 14 and 15 on the HC/HCT4053.

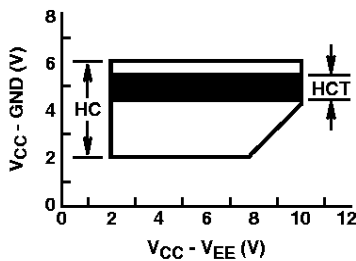## Recommended Operating Area as a Function of Supply Voltages
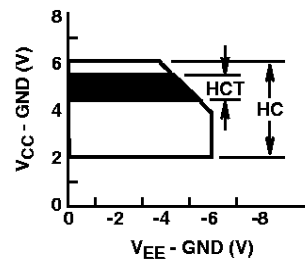
FIGURE 1.

FIGURE 2.

DC Electrical Specifications

PARAMETER	TEST CONDITIONS				AMBIENT TEMPERATURE, T_A							UNITS
	V_{IS} (V)	V_I (V)	V_{EE} (V)	V_{CC} (V)	25°C			-40°C - 85°C		-55°C - 125°C		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage, V_{IH}				2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	0	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage, V_{IL}				2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
On Resistance, r_{ON} I_O = 1mA, (Figure 11)	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	-	70	160	-	200	-	240	Ω
			0	6	-	60	140	-	175	-	210	Ω
			-4.5	4.5	-	40	120	-	150	-	180	Ω
	V_{CC} to V_{EE}		0	4.5	-	90	180	-	225	-	270	Ω
			0	6	-	80	160	-	200	-	240	Ω
			-4.5	4.5	-	45	130	-	162	-	195	Ω
Maximum On Resistance Between any Two Channels, Δr_{ON}			0	4.5	-	10	-	-	-	-	-	Ω
			0	6	-	8.5	-	-	-	-	-	Ω
			-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch On/Off Leakage Current, I_{IZ}	For Switch Off: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC} For Switch On: All Applicable Combinations of V_{IS} and V_{OS} Voltage Levels	V_{IL} or V_{IH}										
1 and 2 Channels			0	6	-	-	±0.1	-	±1	-	±1	µA
4053			-5	5	-	-	±0.1	-	±1	-	±1	µA
4 Channels			0	6	-	-	±0.1	-	±1	-	±1	µA
4052			-5	5	-	-	±0.2	-	±2	-	±2	µA
8 Channels			0	6	-	-	±0.2	-	±2	-	±2	µA
4051			-5	5	-	-	±0.4	-	±4	-	±4	µA
Control Input Leakage Current, I_{IL}		V_{CC} or GND	0	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current, I_{CC} I_O = 0	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
	When V_{IS} = V_{CC}, V_{OS} = V_{EE}		-5	5	-	-	16	-	160	-	320	µA

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS V_{IS} (V)	V_I (V)	V_{EE} (V)	V_{CC} (V)	25°C MIN	TYP	MAX	-40°C - 85°C MIN	MAX	-55°C - 125°C MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage, V_{IH}				4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage, V_{IL}				4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
On Resistance, r_{ON} I_O = 1mA, (Figure 15)	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	-	70	160	-	200	-	240	Ω
			-	-	-	-	-	-	-	-	-	Ω
			-4.5	4.5	-	40	120	-	150	-	180	Ω
	V_{CC} to V_{EE}		0	4.5	-	90	180	-	225	-	270	Ω
			-	-	-	-	-	-	-	-	-	Ω
			-4.5	4.5	-	45	130	-	162	-	195	Ω
Maximum On Resistance Between any Two Channels, Δr_{ON}			0	4.5	-	10	-	-	-	-	-	Ω
			-	-	-	-	-	-	-	-	-	Ω
			-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch On/Off Leakage Current, I_{IZ}	For Switch Off: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC} For Switch On: All Applicable Combinations of V_{IS} and V_{OS} Voltage Levels	V_{IL} or V_{IH}										
1 and 2 Channels			0	6	-	-	±0.1	-	±1	-	±1	µA
4053			-5	5	-	-	±0.1	-	±1	-	±1	µA
4 Channels			0	6	-	-	±0.1	-	±1	-	±1	µA
4052			-5	5	-	-	±0.2	-	±2	-	±2	µA
8 Channels			0	6	-	-	±0.2	-	±2	-	±2	µA
4051			-5	5	-	-	±0.4	-	±4	-	±4	µA
Control Input Leakage Current, I_{IL}	-	(Note 7)	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current, I_{CC} I_O = 0	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
	When V_{IS} = V_{CC}, V_{OS} = V_{EE}		-4.5	5.5	-	-	16	-	160	-	320	µA
Additional Quiescent Device Current, ΔI_{CC} (Note 6) Per Input Pin: 1 Unit Load		V_{CC} - 2.1		4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

6. For dual supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

7. Any voltage between V_{CC} and GND.

HCT Input Loading Table

TYPE	INPUT	UNIT LOADS (NOTE)
4051, 4053	All	0.5
4052	All	0.4

NOTE: Unit load is ΔI_{CC} limit specified in DC Specifications table, e.g., 360mA max. at 25°C.

Switching Specifications V_{CC} = 5V, T_A = 25°C, Input t_r, t_r = 6ns

PARAMETER	C_L (pF)	TYPICAL						UNITS
		4051		4052		4053		
		HC	HCT	HC	HCT	HC	HCT	
Propagation Delay								
Switch IN to OUT, t_{PHL}, t_{PLH}	15	4	4	4	4	4	4	ns
Switch Turn-Off (S or $\overline{E}$), t_{PHZ}, t_{PLZ}	15	19	19	21	21	18	18	ns
Switch Turn-On (S or $\overline{E}$), t_{PZH}, t_{PZL}	15	19	23	27	29	18	20	ns
Power Dissipation Capacitance, C_{PD} (Note 8)	-	50	52	74	76	38	42	pF

NOTE:

8. C_{PD} is used to determine the dynamic power consumption, per package.
  $P_D = C_{PD} V_{CC}^2 f_I + \Sigma (C_L + C_S) V_{CC}^2 f_O$
  f_O = output frequency
  f_I = input frequency
  C_L = output load capacitance
  C_S = switch capacitance
  V_{CC} = supply voltage

Switching Specifications C_L = 50pF, Input t_r, t_r = 6ns

PARAMETER		V_{EE} (V)	V_{CC} (V)	AMBIENT TEMPERATURE, T_A											UNITS
				25°C				-40°C - 85°C				-55°C - 125°C			
				HC		HCT		HC		HCT		HC		HCT		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, Switch In to Out, t_{PLH}, t_{PHL}		0	2	-	60	-	-	-	75	-	-	-	90	-	-	ns
		0	4.5	-	12	-	12	-	15	-	15	-	18	-	18	ns
		0	6	-	10	-	-	-	13	-	-	-	15	-	-	ns
		-4.5	4.5	-	8	-	8	-	10	-	10	-	12	-	12	ns
Maximum Switch Turn "Off" Delay from S or $\overline{E}$ to Switch Output t_{PHZ}, t_{PLZ}	4051	0	2	-	225	-	-	-	280	-	-	-	340	-	-	ns
		0	4.5	-	45	-	45	-	56	-	56	-	68	-	68	ns
		0	6	-	38	-	-	-	48	-	-	-	57	-	-	ns
		-4.5	4.5	-	32	-	32	-	40	-	40	-	48	-	48	ns
	4052	0	2	-	250	-	-	-	315	-	-	-	375	-	-	ns
		0	4.5	-	50	-	50	-	63	-	63	-	75	-	75	ns
		0	6	-	43	-	-	-	54	-	-	-	65	-	-	ns
		-4.5	4.5	-	38	-	38	-	48	-	48	-	57	-	57	ns
	4053	0	2	-	210	-	-	-	265	-	-	-	315	-	-	ns
		0	4.5	-	42	-	44	-	53	-	55	-	63	-	66	ns
		0	6	-	36	-	-	-	45	-	-	-	54	-	-	ns
		-4.5	4.5	-	29	-	31	-	36	-	39	-	44	-	47	ns

Switching Specifications $C_L = 50pF$, Input t_r, $t_f = 6ns$ (Continued)

PARAMETER		V_{EE} (V)	V_{CC} (V)	25°C HC MIN	25°C HC MAX	25°C HCT MIN	25°C HCT MAX	-40°C - 85°C HC MIN	-40°C - 85°C HC MAX	-40°C - 85°C HCT MIN	-40°C - 85°C HCT MAX	-55°C - 125°C HC MIN	-55°C - 125°C HC MAX	-55°C - 125°C HCT MIN	-55°C - 125°C HCT MAX	UNITS
Maximum Switch Turn "On" Delay from S or E to Switch Output t_{PZL}, t_{PZH}	4051	0	2	-	225	-	-	-	280	-	-	-	340	-	-	ns
		0	4.5	-	45	-	55	-	56	-	69	-	68	-	83	ns
		0	6	-	38	-	-	-	48	-	-	-	57	-	-	ns
		-4.5	4.5	-	32	-	39	-	40	-	49	-	48	-	59	ns
	4052	0	2	-	325	-	-	-	405	-	-	-	490	-	-	ns
		0	4.5	-	65	-	70	-	81	-	68	-	98	-	105	ns
		0	6	-	55	-	-	-	69	-	-	-	83	-	-	ns
		-4.5	4.5	-	46	-	48	-	58	-	60	-	69	-	72	ns
	4053	0	2	-	220	-	-	-	275	-	-	-	330	-	-	ns
		0	4.5	-	44	-	48	-	55	-	60	-	66	-	72	ns
		0	6	-	37	-	-	-	47	-	-	-	56	-	-	ns
		-4.5	4.5	-	31	-	34	-	39	-	43	-	47	-	51	ns
Input (Control) Capacitance, C_I		-	-	-	10	-	10	-	10	-	10	-	10	-	10	pF

Analog Channel Specifications Typical Values at $T_A = 25°C$

PARAMETER	TEST CONDITIONS	HC/HCT TYPES	V_{EE} (V)	V_{CC} (V)	HC/ HCT	UNITS
Switch Input Capacitance, C_I		All	-	-	5	pF
Common Output Capacitance, C_{COM}		4051	-	-	25	pF
		4052	-	-	12	pF
		4053	-	-	8	pF
Minimum Switch Frequency Response at -3dB, f_{MAX} (Figures 12, 14, 16)	See Figure 3, Notes 9, 10	4051	-2.25	2.25	145	MHz
		4052			165	MHz
		4053			200	MHz
		4051	-4.5	4.5	180	MHz
		4052			185	MHz
		4053			200	MHz

Analog Channel Specifications Typical Values at $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	HC/HCT TYPES	V_{EE} (V)	V_{CC} (V)	HC/ HCT	UNITS
Crosstalk Between any Two Switches (Note 12)	See Figure 4, Notes 10, 11	4051			N/A	dB
		4052	-2.25	2.25	(TBE)	dB
		4053			(TBE)	dB
		4051			N/A	dB
		4052	-4.5	4.5	(TBE)	dB
		4053			(TBE)	dB
Sinewave Distortion	See Figure 5	All	-2.25	2.25	0.035	%
		All	-4.5	4.5	0.018	%
$\overline{E}$ or S to Switch Feedthrough Noise	See Figure 6 Notes 10, 11	4051				mV
		4052	-2.25	2.25	(TBE)	mV
		4053				mV
		4051				mV
		4052	-4.5	4.5	(TBE)	mV
		4053				mV
Switch "OFF" Signal Feedthrough (Figures 13, 15, 17)	See Figure 7 Notes 10, 11	4051			-73	dB
		4052	-2.25	2.25	-65	dB
		4053			-64	dB
		4051			-75	dB
		4052	-4.5	4.5	-67	dB
		4053			-66	dB

NOTES:

9. Adjust input voltage to obtain 0dBm at V_{OS} for f_{IN} = 1MHz.

10. V_{IS} is centered at (V_{CC} - V_{EE})/2.

11. Adjust input for 0dBm.

12. Not applicable for HC/HCT4051.

Test Circuits and Waveforms
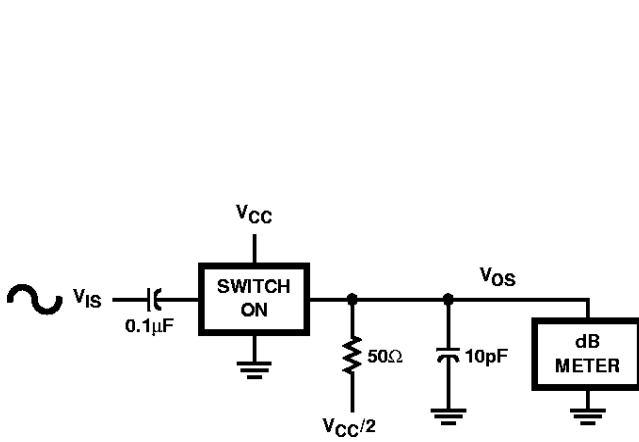
FIGURE 3. FREQUENCY RESPONSE TEST CIRCUIT

f_{IS} = 1MHz SINEWAVE
R = 50Ω
C = 10pF
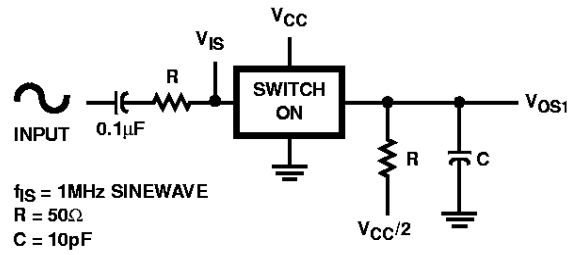
FIGURE 4. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

f_{IS} = 1kHz TO 10kHz
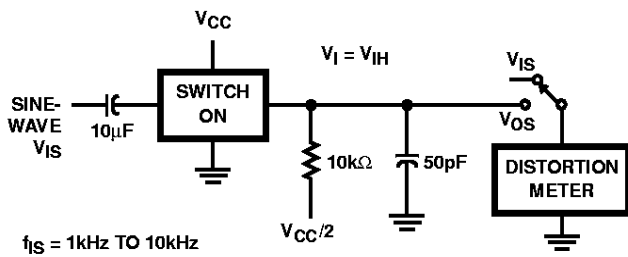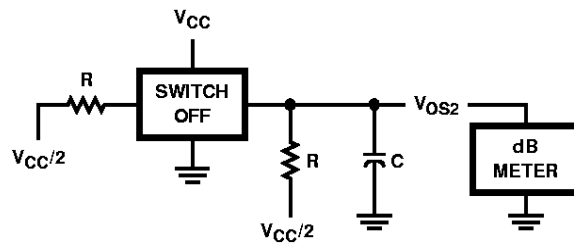
FIGURE 5. SINEWAVE DISTORTION TEST CIRCUIT
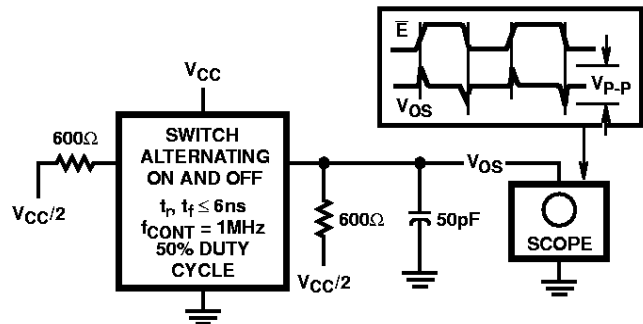
FIGURE 6. CONTROL TO SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

$f_{IS} \geq$ 1MHz SINEWAVE
R = 50Ω
C = 10pF
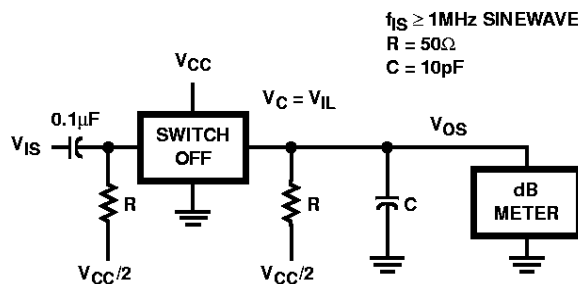
FIGURE 7. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms (Continued)
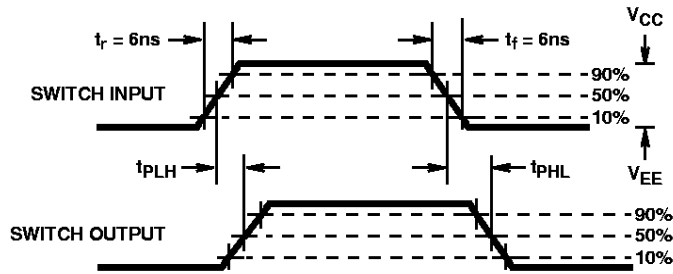
FIGURE 8A.
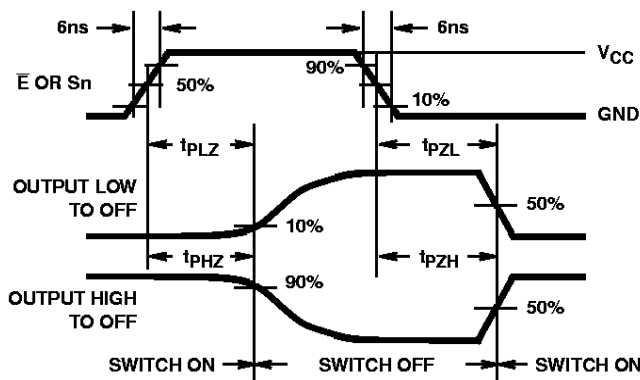
FIGURE 8B. HC TYPES
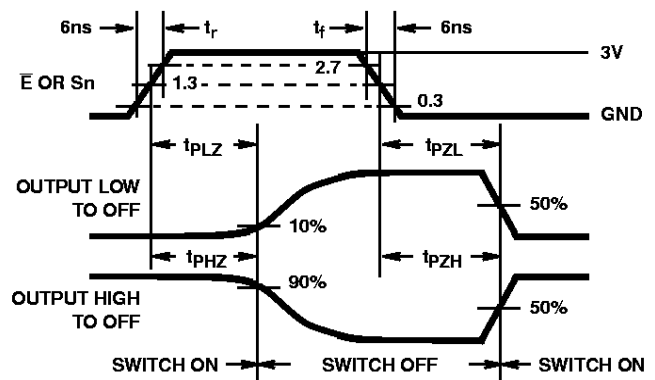
FIGURE 8C. HCT TYPES

FIGURE 8. SWITCH PROPAGATION DELAY, TURN-ON, TURN-OFF TIMES
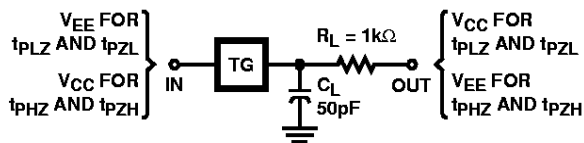
FIGURE 9. SWITCH ON/OFF PROPAGATION DELAY TEST CIRCUIT
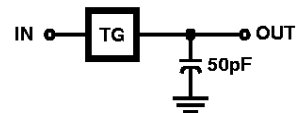
FIGURE 10. SWITCH IN TO SWITCH OUT PROPAGATION DELAY TEST CIRCUIT

Typical Performance Curves
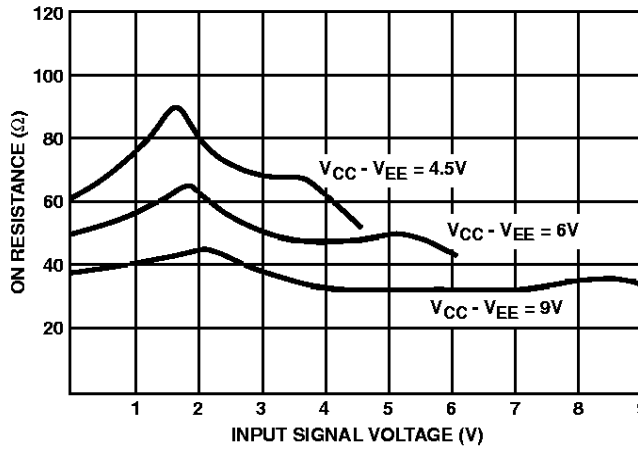
FIGURE 11. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE
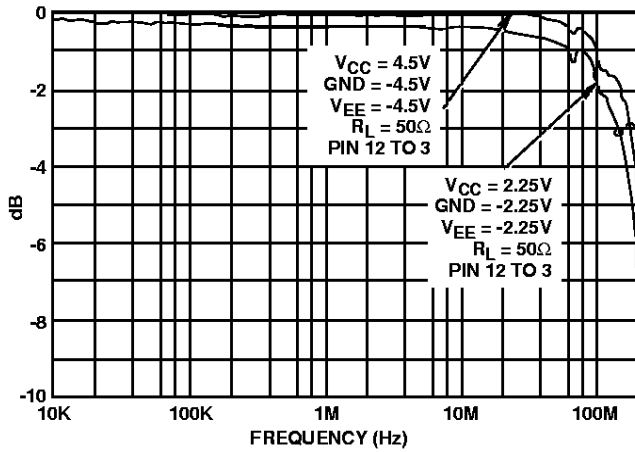
FIGURE 12. CHANNEL ON BANDWIDTH (HC/HCT4051)
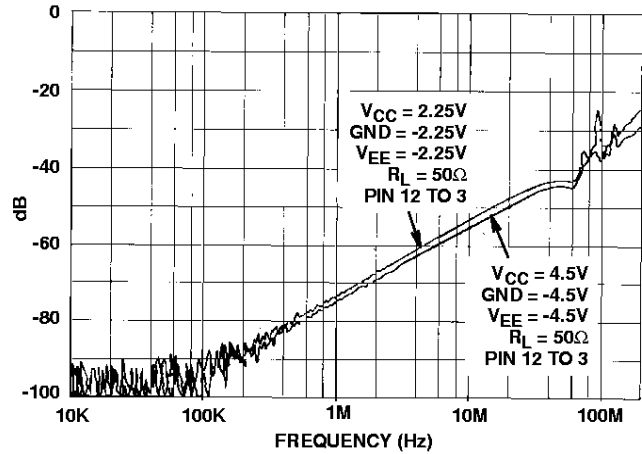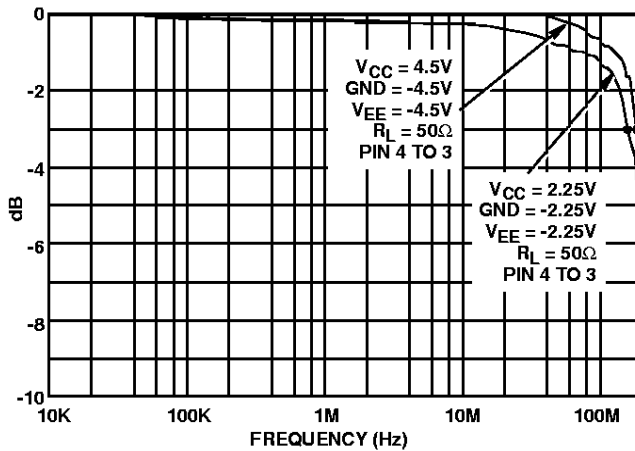

FIGURE 13. CHANNEL OFF FEEDTHROUGH (HC/HCT4051)

FIGURE 14. CHANNEL ON BANDWIDTH (HC/HCT4052)
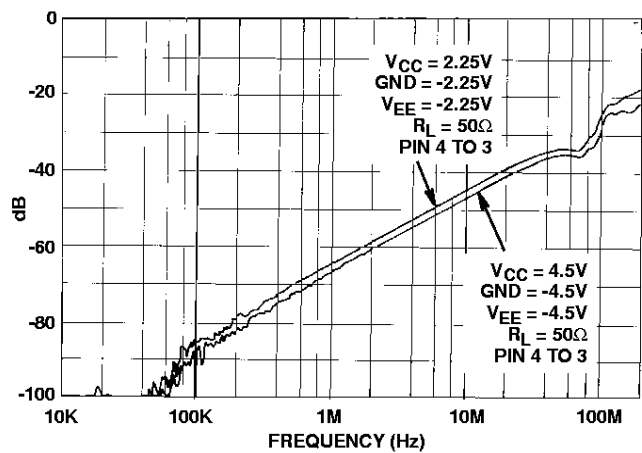
FIGURE 15. CHANNEL OFF FEEDTHROUGH (HC/HCT4052)
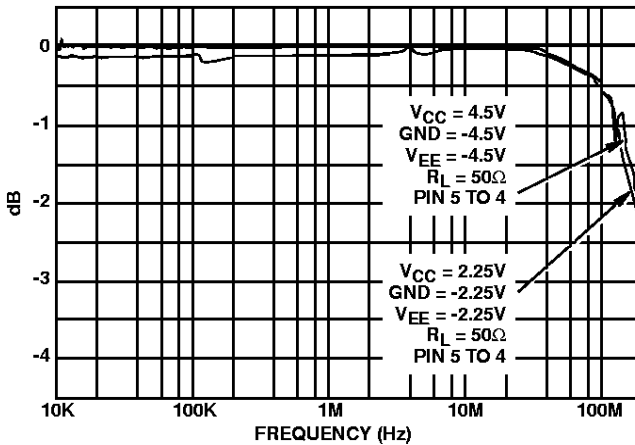
Typical Performance Curves (Continued)

V$_{CC}$ = 4.5V
GND = -4.5V
V$_{EE}$ = -4.5V
R$_L$ = 50Ω
PIN 5 TO 4

V$_{CC}$ = 2.25V
GND = -2.25V
V$_{EE}$ = -2.25V
R$_L$ = 50Ω
PIN 5 TO 4

FREQUENCY (Hz)

FIGURE 16. CHANNEL ON BANDWIDTH (HC/HCT4053)

V$_{CC}$ = 2.25V
GND = -2.25V
V$_{EE}$ = -2.25V
R$_L$ = 50Ω
PIN 5 TO 4

V$_{CC}$ = 4.5V
GND = -4.5V
V$_{EE}$ = -4.5V
R$_L$ = 50Ω
PIN 5 TO 4

FREQUENCY (Hz)
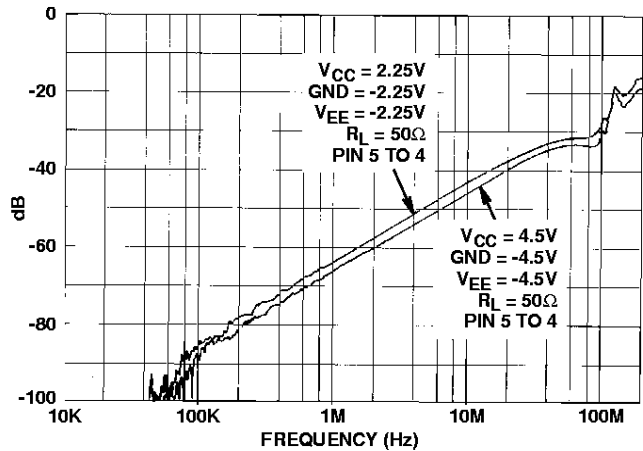
FIGURE 17. CHANNEL OFF FEEDTHROUGH (HC/HCT4053)

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