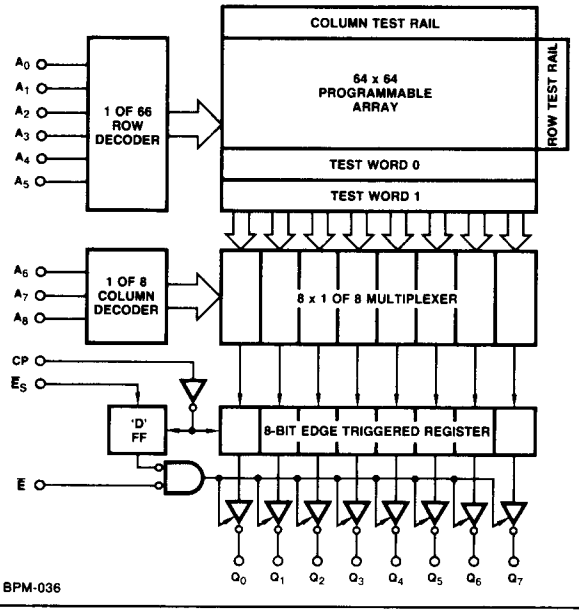
Am27S26 • Am27S27

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Space saving 22 pin package
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



BPM-036

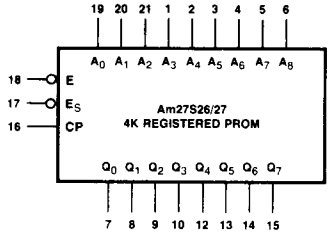
FUNCTIONAL DESCRIPTION

The Am27S26 and Am27S27 are electrically programmable Schottky TTL read only memories incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512 word by 8 bit organization and are available in both the open collector Am27S26 and three-state Am27S27 output versions. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed system and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S26 and Am27S27 also offer maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

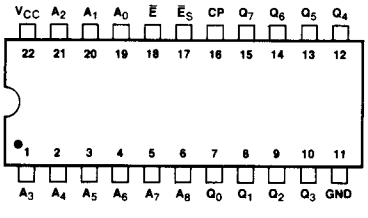
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

BPM-037

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-038

GENERIC SERIES CHARACTERISTICS

The Am27S26 and Am27S27 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 11) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM27S26XC, AM27S27XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	AM27S26XM, AM27S27XM	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S27 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}		0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S27 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $\overline{VE}$ = 2.4V; Am27S27 Only; V_O = 4.5V			100	μA
		V_O = 2.4V			40	
		V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)		12		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

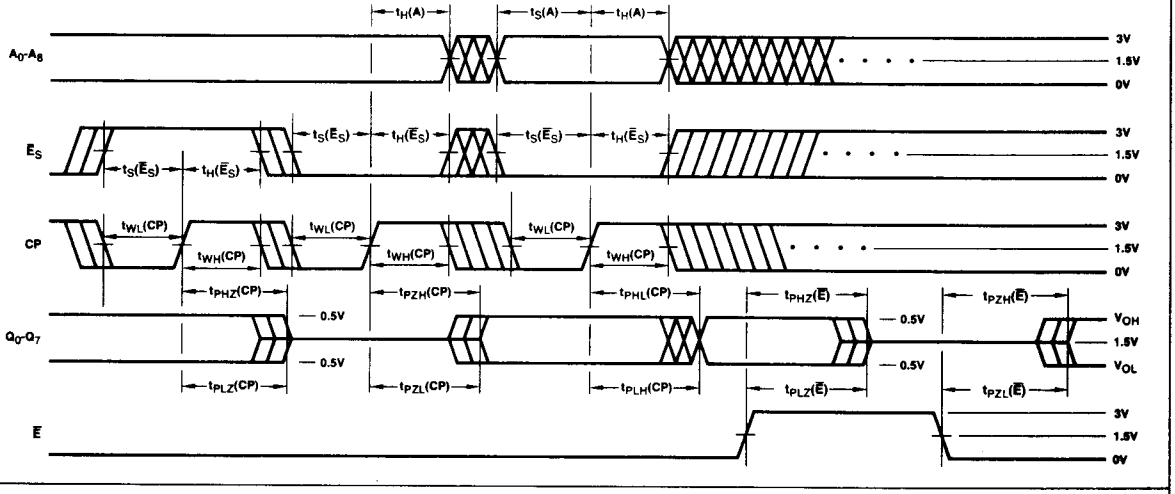
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

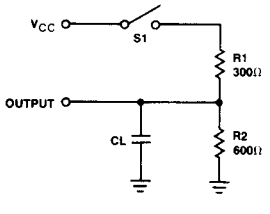
Parameter	Description	Test Conditions	Typ 5V 25°C	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF, S_1 closed. (See AC Test Load below)	40	55		65		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0		0		ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		27		30	ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10	30		40		ns
$t_S(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Setup Time		10	25		30		ns
$t_H(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Hold Time		−10	0		0		ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 1)	C_L = 30pF, S_1 closed for t_{PZL} and open for t_{PZH}	15		35		45	ns
$t_{PZL}(\overline{E})$ $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (Note 1)		15		40		45	ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or High Impedance) (Note 1)	C_L = 5pF (Note 2), S_1 closed for t_{PLZ} and open for t_{PHZ}	15		35		45	ns
$t_{PLZ}(\overline{E})$ $t_{PHZ}(\overline{E})$	Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance) (Note 1)		10		30		40	ns

Notes:
1. t_{PHZ} and t_{PZH} apply to the three-state Am27S27 only.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS



AC TEST LOAD



BPM-040

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING

The Am27S26 and Am27S27 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

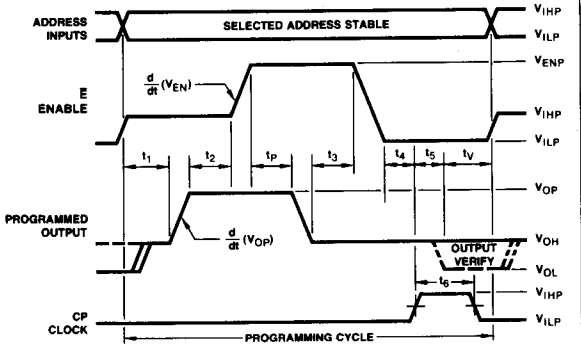
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

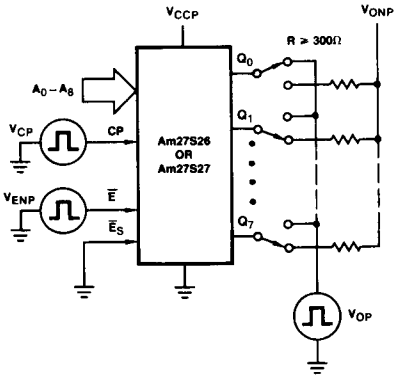
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-041

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-042

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S26 • Am27S27 ADAPTERS AND CONFIGURATOR	715-1412-2	PA22-4 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

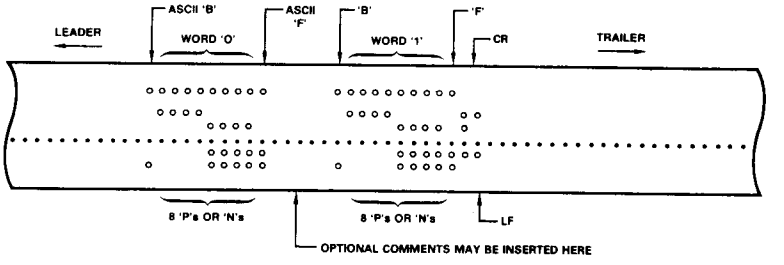
ØØØ	BPNPPNNNPF	WORD ZERO (R) (L)
	BPPPPPPNNF	COMMENT FIELD (R) (L)
ØØ2	BNNNPPPPNF	ANY (R) (L)
	BNNNNNNNNF	TEXT (R) (L)
ØØ4	BPNNNNNNPF	CAN (R) (L)
	BNPPNPPNNF	GO (R) (L)
ØØ6	BPNNPPPNNF	HERE (R) (L)
⋮	⋮	⋮
511	BNNNNPPPNF	END (R) (L)

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\bar{E}$ AND $\bar{E}_S$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-043

APPLYING THE Am27S26 AND Am27S27 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am27S26/27 registered PROM, the design engineer can upgrade the performance of existing systems or implement new systems taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familiar to many design engineers. This technique is called microprogramming.

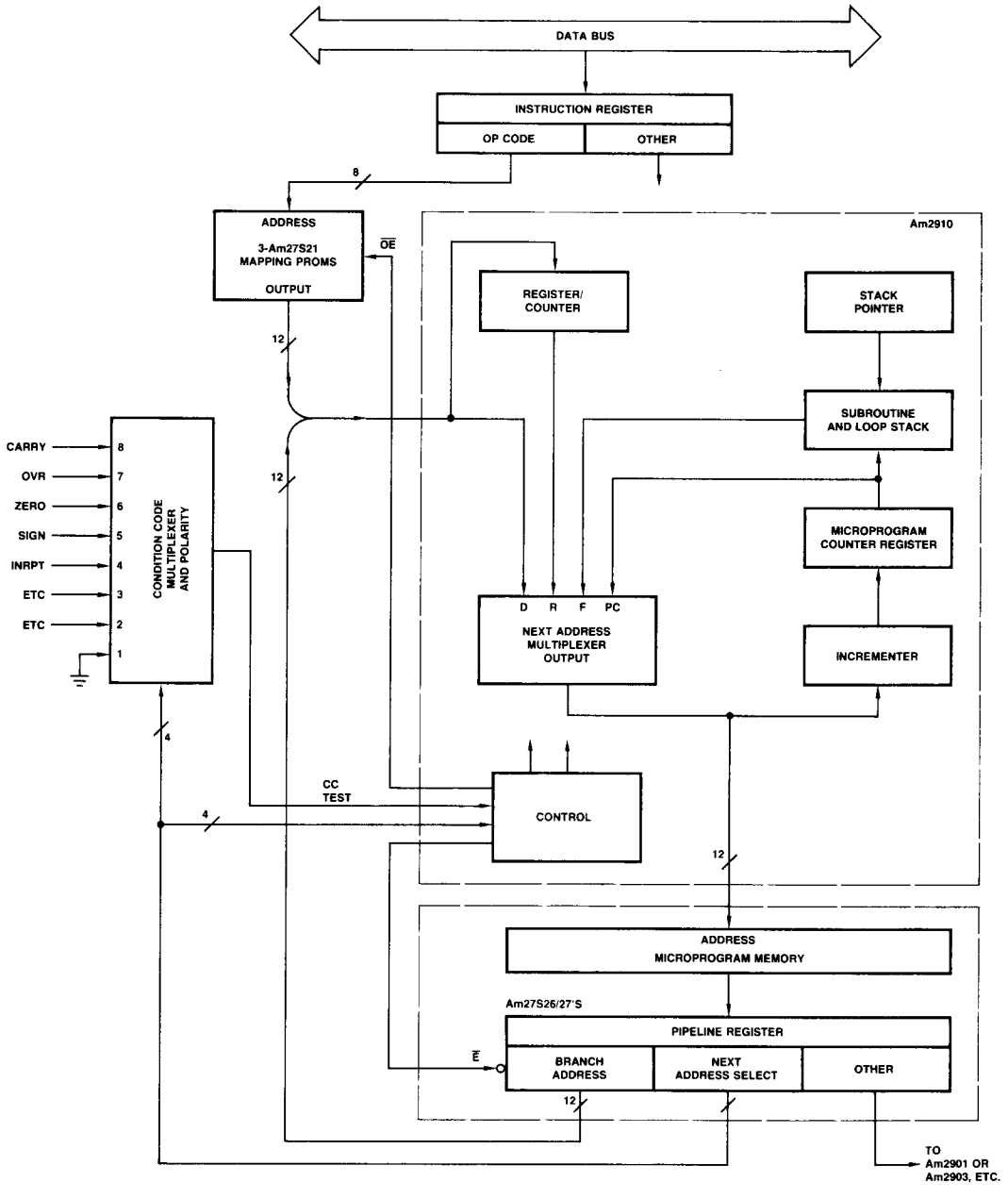


Fig. 1. A Typical Computer Control Unit using the Am27S26/27. BPM-044

APPLYING THE Am27S26 and Am27S27 IN BIPOLAR MICROCOMPUTERS (Cont.)

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROMs for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am27S26/27 registered PROM's. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and the file (F). The starting address decoder (mapping PROM) output and the Am27S26/27's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcycle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am27S26/27 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am27S26/27 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The expansion scheme for increasing the depth of Am27S26/27's is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am27S26/27 registered PROM's is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

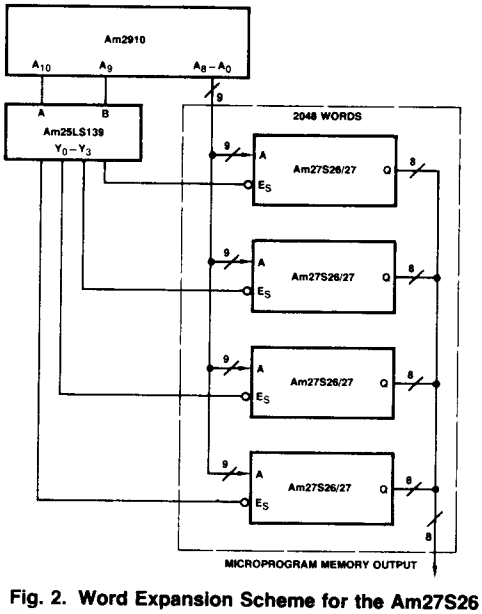


Fig. 2. Word Expansion Scheme for the Am27S26 and Am27S27.

BPM-045

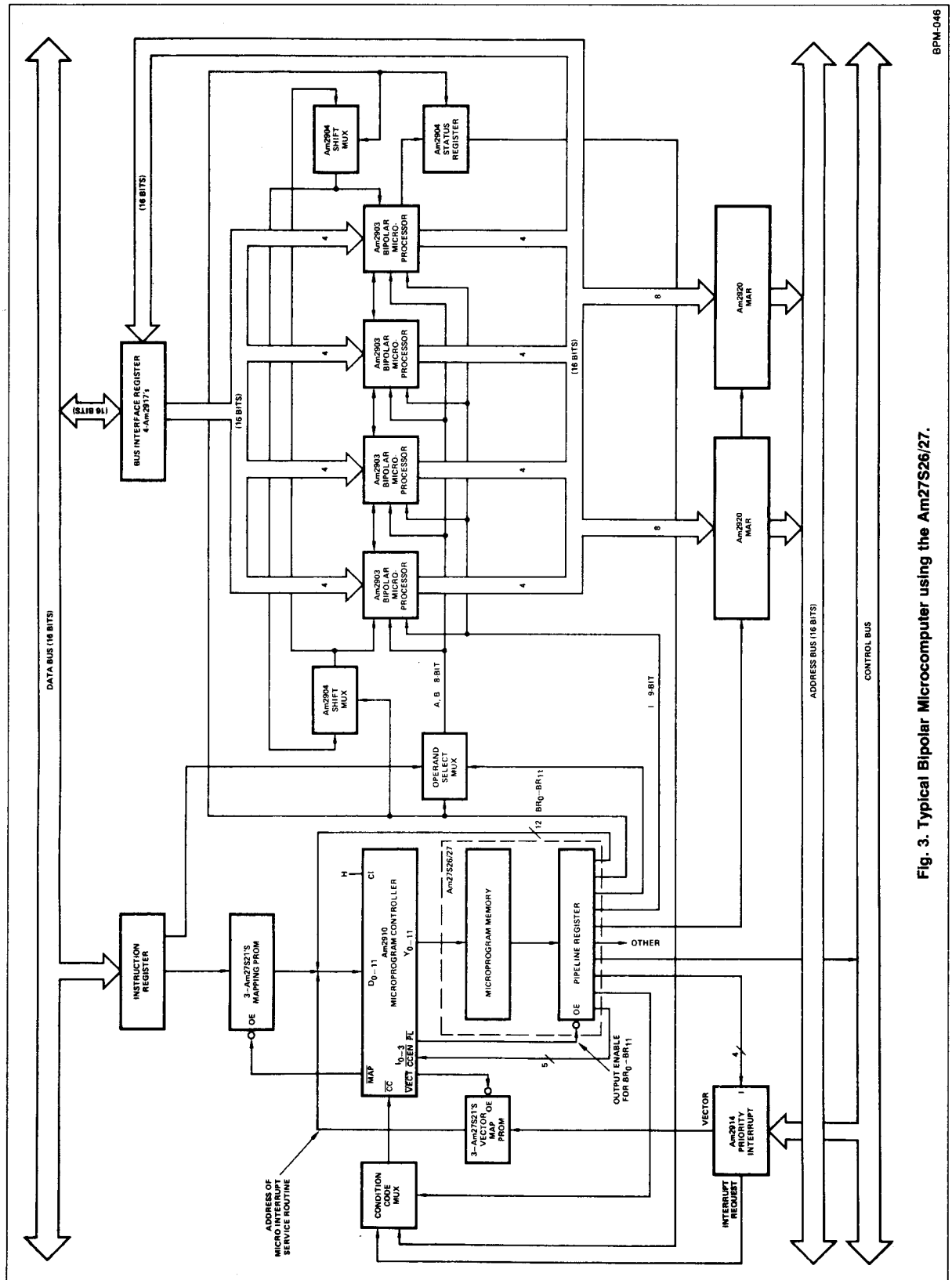
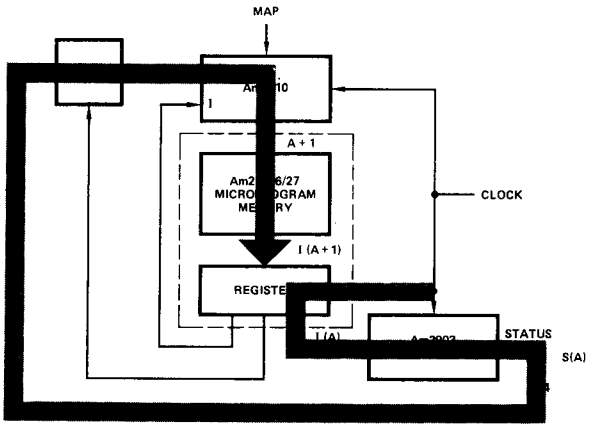


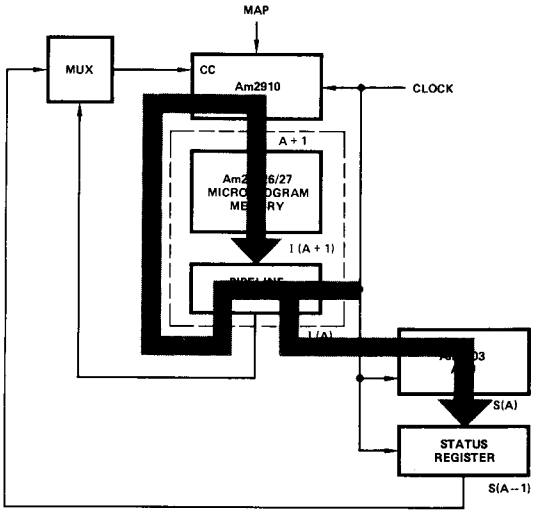
Fig. 3. Typical Bipolar Microcomputer using the Am27S26/27.

USING THE Am27S26/27 IN A PIPELINED ARCHITECTURE



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

BPM-047



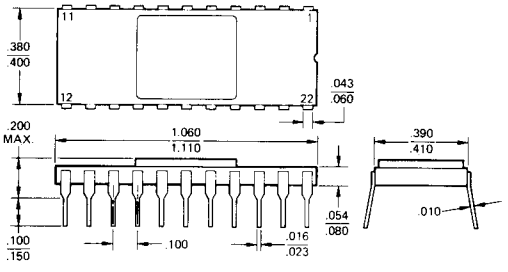
One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am27S26/27 reduces the parts count of the microprogram memory/pipeline by a factor of two.

BPM-048

PHYSICAL DIMENSIONS

Dual In-Line

22-Pin Hermetic



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S26DC
Hermetic DIP	−55°C to +125°C	AM27S26DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S27DC
Hermetic DIP	−55°C to +125°C	AM27S27DM