

### FEATURE

#### HIGH DC PRECISION

50  $\mu\text{V}$  max Offset Voltage  
 0.6  $\mu\text{V}/^\circ\text{C}$  max Offset Drift  
 110 pA max Input Bias Current

#### LOW NOISE

0.5  $\mu\text{V}$  p-p Voltage Noise, 0.1 Hz to 10 Hz

#### LOW POWER

750  $\mu\text{A}$  Supply Current  
 Available in 8-Lead Plastic Mini-DIP, Hermetic Cerdip and Surface Mount (SOIC) Packages  
 Available in Tape and Reel in Accordance with EIA-481A Standard  
 Quad Version: AD704

### APPLICATIONS

Low Frequency Active Filters  
 Precision Instrumentation  
 Precision Integrators

### PRODUCT DESCRIPTION

The AD706 is a dual, low power, bipolar op amp that has the low input bias current of a BiFET amplifier, but which offers a significantly lower  $I_B$  drift over temperature. It utilizes superbeta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its  $I_B$  typically only increases by 5 $\times$  at 125 $^\circ\text{C}$  (unlike a BiFET amp, for which  $I_B$  doubles every 10 $^\circ\text{C}$  for a 1000 $\times$  increase at 125 $^\circ\text{C}$ ). The AD706 also achieves the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

Since it has only 1/20 the input bias current of an OP07, the AD706 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP07, which makes this amplifier usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP07, the AD706 is better suited for today's higher density boards.

The AD706 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation and as a high quality integrator. The AD706 is internally compensated for unity gain and is available in five performance grades. The AD706J and AD706K are rated over the commercial temperature range of 0 $^\circ\text{C}$  to +70 $^\circ\text{C}$ .

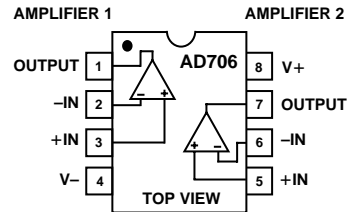
The AD706 is offered in two varieties of an 8-lead package: plastic mini-DIP and surface mount (SOIC). "J" grade chips are also available.

### REV. D

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### CONNECTION DIAGRAM

Plastic Mini-DIP (N) and Plastic SOIC (R) Packages



### PRODUCT HIGHLIGHTS

1. The AD706 is a dual low drift op amp that offers BiFET level input bias currents, yet has the low  $I_B$  drift of a bipolar amplifier. It may be used in circuits using dual op amps such as the LT1024.
2. The AD706 provides both low drift and high dc precision.
3. The AD706 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise.

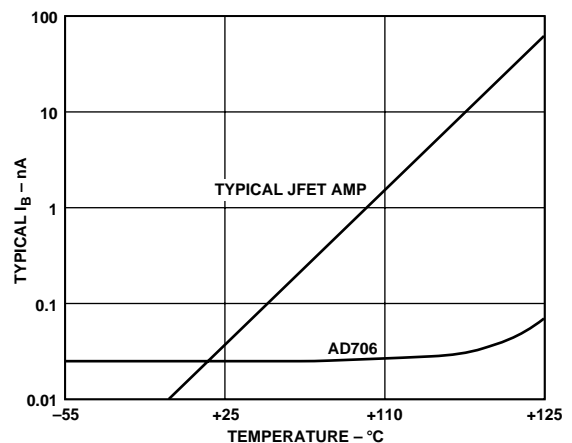


Figure 1. Input Bias Current vs. Temperature

# AD706—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$ , $V_{CM} = 0\text{ V}$ and $\pm 15\text{ V}$ dc, unless otherwise noted)

Parameter	Conditions	AD706J			AD706K			Units
		Min	Typ	Max	Min	Typ	Max	
<b>INPUT OFFSET VOLTAGE</b>								
Initial Offset			30	100		10	50	$\mu\text{V}$
Offset	$T_{MIN}$ to $T_{MAX}$		40	150		25	100	$\mu\text{V}$
vs. Temp, Average TC			0.2	1.5		0.2	0.6	$\mu\text{V}/^\circ\text{C}$
vs. Supply (PSRR)	$V_S = \pm 2\text{ V}$ to $\pm 18\text{ V}$	110	132		112	132		dB
$T_{MIN}$ to $T_{MAX}$	$V_S = \pm 2.5\text{ V}$ to $\pm 18\text{ V}$	106	126		108	126		dB
Long Term Stability			0.3			0.3		$\mu\text{V}/\text{Month}$
<b>INPUT BIAS CURRENT<sup>1</sup></b>								
	$V_{CM} = 0\text{ V}$		50	200		30	110	pA
	$V_{CM} = \pm 13.5\text{ V}$			250			160	pA
vs. Temp, Average TC			0.3			0.2		$\text{pA}/^\circ\text{C}$
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = 0\text{ V}$			300			200	pA
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = \pm 13.5\text{ V}$			400			300	pA
<b>INPUT OFFSET CURRENT</b>								
	$V_{CM} = 0\text{ V}$		30	150		30	100	pA
	$V_{CM} = \pm 13.5\text{ V}$			250			200	pA
vs. Temp, Average TC			0.6			0.4		$\text{pA}/^\circ\text{C}$
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = 0\text{ V}$		80	250		80	200	pA
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = \pm 13.5\text{ V}$		80	350		80	300	pA
<b>MATCHING CHARACTERISTICS</b>								
Offset Voltage				150			75	$\mu\text{V}$
	$T_{MIN}$ to $T_{MAX}$			250			150	$\mu\text{V}$
Input Bias Current <sup>2</sup>				300			150	pA
	$T_{MIN}$ to $T_{MAX}$			500			250	pA
Common-Mode Rejection		106			110			dB
	$T_{MIN}$ to $T_{MAX}$	106			108			dB
Power Supply Rejection		106			110			dB
	$T_{MIN}$ to $T_{MAX}$	104			106			dB
Crosstalk (Figure 19a)	$T_{MIN}$ to $T_{MAX}$ @ $f = 10\text{ Hz}$ $R_L = 2\text{ k}\Omega$		150			150		dB
<b>FREQUENCY RESPONSE</b>								
Unity Gain Crossover Frequency			0.8			0.8		MHz
Slew Rate	$G = -1$		0.15			0.15		$\text{V}/\mu\text{s}$
	$T_{MIN}$ to $T_{MAX}$		0.15			0.15		$\text{V}/\mu\text{s}$
<b>INPUT IMPEDANCE</b>								
Differential			40  2			40  2		$\text{M}\Omega  \text{pF}$
Common Mode			300  2			300  2		$\text{G}\Omega  \text{pF}$
<b>INPUT VOLTAGE RANGE</b>								
Common-Mode Voltage		$\pm 13.5$	$\pm 14$		$\pm 13.5$	$\pm 14$		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{ V}$	110	132		114	132		dB
	$T_{MIN}$ to $T_{MAX}$	108	128		108	128		dB
<b>INPUT CURRENT NOISE</b>								
	0.1 Hz to 10 Hz		3			3		$\text{pA p-p}$
	$f = 10\text{ Hz}$		50			50		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE NOISE</b>								
	0.1 Hz to 10 Hz		0.5		0.5	1.0		$\mu\text{V p-p}$
	$f = 10\text{ Hz}$		17		17			$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		15	22	15	22		$\text{nV}/\sqrt{\text{Hz}}$
<b>OPEN-LOOP GAIN</b>								
	$V_O = \pm 12\text{ V}$		200	2000		400	2000	$\text{V}/\text{mV}$
	$R_{LOAD} = 10\text{ k}\Omega$							$\text{V}/\text{mV}$
	$T_{MIN}$ to $T_{MAX}$		150	1500		300	1500	$\text{V}/\text{mV}$
	$V_O = \pm 10\text{ V}$							$\text{V}/\text{mV}$
	$R_{LOAD} = 2\text{ k}\Omega$		200	1000		300	1000	$\text{V}/\text{mV}$
	$T_{MIN}$ to $T_{MAX}$		150	1000		200	1000	$\text{V}/\text{mV}$
<b>OUTPUT CHARACTERISTICS</b>								
Voltage Swing	$R_{LOAD} = 10\text{ k}\Omega$	$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
	$T_{MIN}$ to $T_{MAX}$	$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
Current Capacitive Load Drive Capability	Short Circuit		$\pm 15$			$\pm 15$		mA
	Gain = +1		10,000			10,000		pF

Parameter	Conditions	AD706J			AD706K			Units	
		Min	Typ	Max	Min	Typ	Max		
<b>POWER SUPPLY</b>									
Rated Performance			±15			±15		V	
Operating Range		±2.0		±18	±2.0		±18	V	
Quiescent Current, Total	$T_{MIN}$ to $T_{MAX}$		0.75	1.2		0.75	1.2	mA	
			0.8	1.4		0.8	1.4	mA	
<b>TRANSISTOR COUNT</b>									
	# of Transistors		90			90			

**NOTES**

<sup>1</sup>Bias current specifications are guaranteed maximum at either input.

<sup>2</sup>Input bias current match is the difference between corresponding inputs ( $I_B$  of -IN of Amplifier #1 minus  $I_B$  of -IN of Amplifier #2).

CMRR match is the difference between  $\frac{\Delta V_{OS} \#1}{\Delta V_{CM}}$  for amplifier #1 and  $\frac{\Delta V_{OS} \#2}{\Delta V_{CM}}$  for amplifier #2 expressed in dB.

PSRR match is the difference between  $\frac{\Delta V_{OS} \#1}{\Delta V_{SUPPLY}}$  for amplifier #1 and  $\frac{\Delta V_{OS} \#2}{\Delta V_{SUPPLY}}$  for amplifier #2 expressed in dB.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	±18 V
Internal Power Dissipation (Total: Both Amplifiers) <sup>2</sup>	650 mW
Input Voltage	± $V_S$
Differential Input Voltage <sup>3</sup>	+0.7 Volts
Output Short Circuit Duration	Indefinite
Storage Temperature Range (N, R)	-65°C to +125°C
Operating Temperature Range	
AD706J/K	0°C to +70°C
Lead Temperature (Soldering 10 secs)	+300°C

**NOTES**

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Specification is for device in free air:

8-Lead Plastic Package:  $\theta_{JA} = 100^\circ\text{C/Watt}$

8-Lead Small Outline Package:  $\theta_{JA} = 155^\circ\text{C/Watt}$

<sup>3</sup>The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

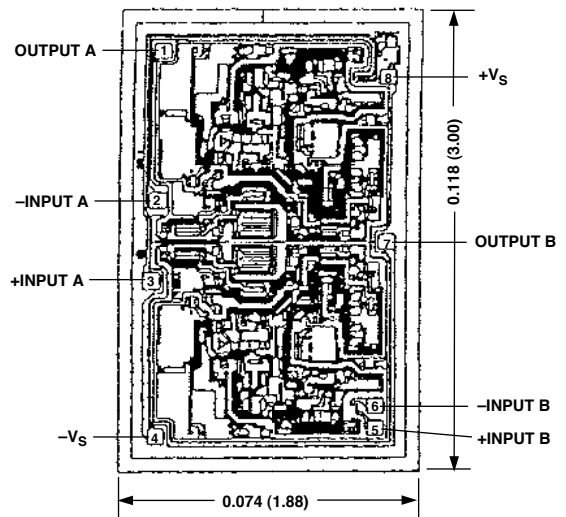
**ORDERING GUIDE**

Model	Temperature Range	Description	Package Option*
AD706JN	0°C to +70°C	Plastic DIP	N-8
AD706KN	0°C to +70°C	Plastic DIP	N-8
AD706JR	0°C to +70°C	SOIC	RN-8
AD706JR-REEL	0°C to +70°C	Tape and Reel	
AD706AR	-40°C to +85°C	SOIC	RN-8
AD706AR-REEL	-40°C to +85°C	Tape and Reel	

\*N = Plastic DIP; RN = SOIC Package.

**METALIZATION PHOTOGRAPH**

Dimensions shown in inches and (mm).  
Contact factory for latest dimensions.



**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD706 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# AD706—Typical Performance Characteristics (@ +25°C, $V_S = \pm 15$ V, unless otherwise noted)

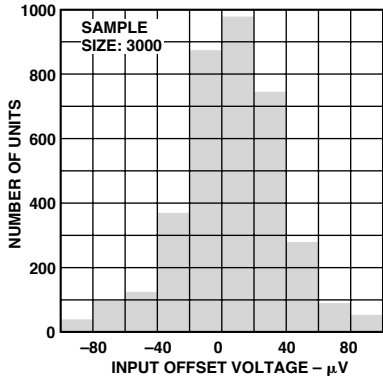


Figure 2. Typical Distribution of Input Offset Voltage

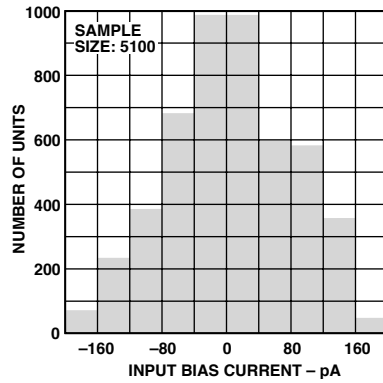


Figure 3. Typical Distribution of Input Bias Current

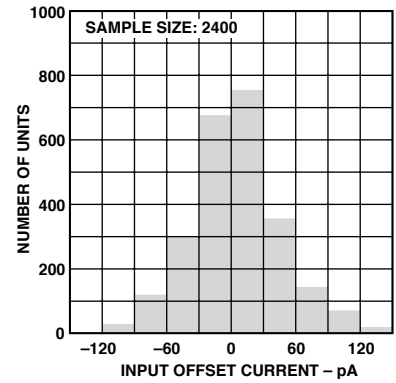


Figure 4. Typical Distribution of Input Offset Current

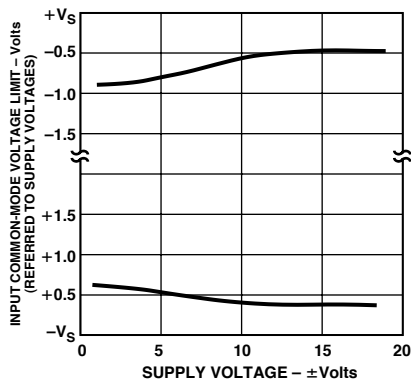


Figure 5. Input Common-Mode Voltage Range vs. Supply Voltage

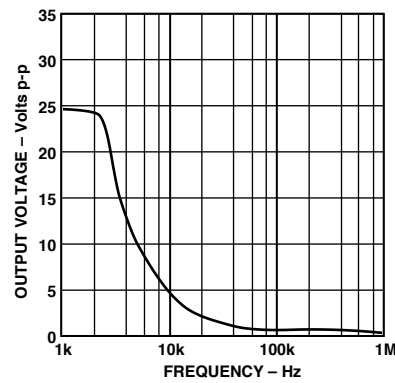


Figure 6. Large Signal Frequency Response

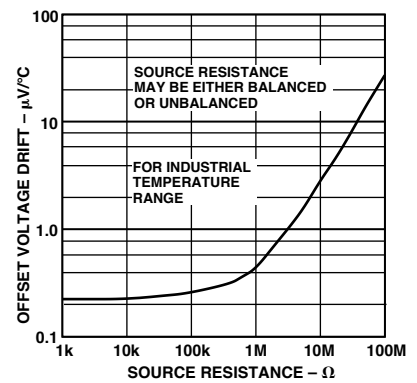


Figure 7. Offset Voltage Drift vs. Source Resistance

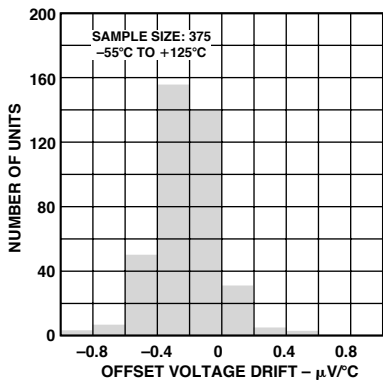


Figure 8. Typical Distribution of Offset Voltage Drift

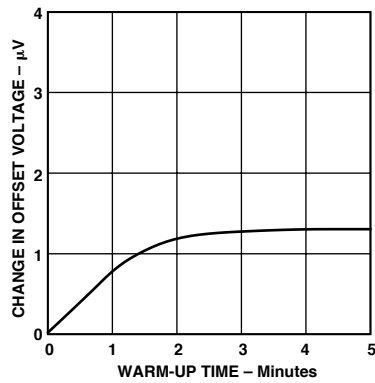


Figure 9. Change in Input Offset Voltage vs. Warm-Up Time

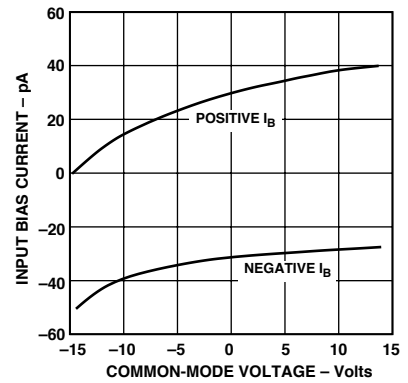


Figure 10. Input Bias Current vs. Common-Mode Voltage

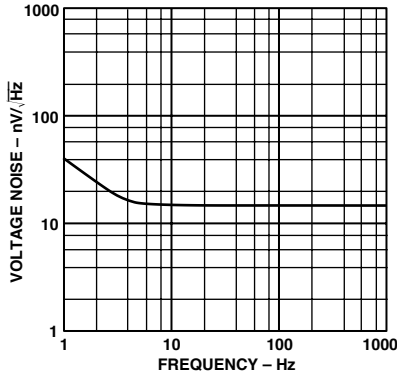


Figure 11. Input Noise Voltage Spectral Density

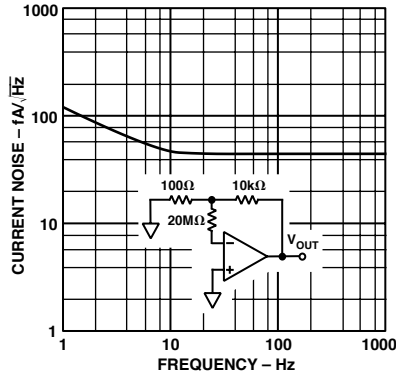


Figure 12. Input Noise Current Spectral Density

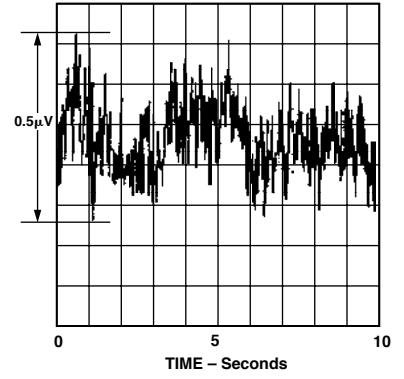


Figure 13. 0.1 Hz to 10 Hz Noise Voltage

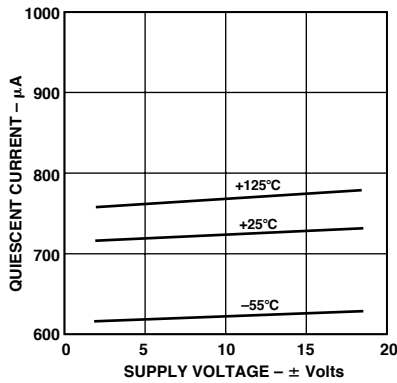


Figure 14. Quiescent Supply Current vs. Supply Voltage

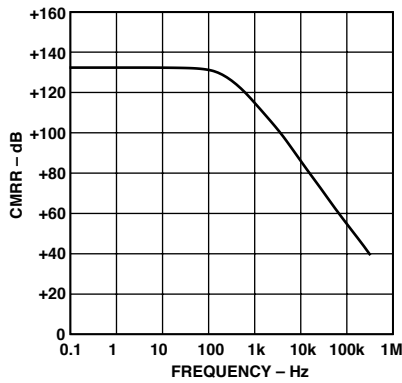


Figure 15. Common-Mode Rejection Ratio vs. Frequency

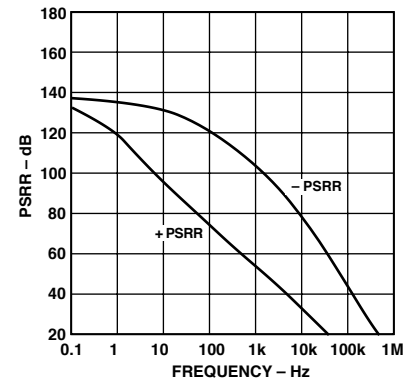


Figure 16. Power Supply Rejection Ratio vs. Frequency

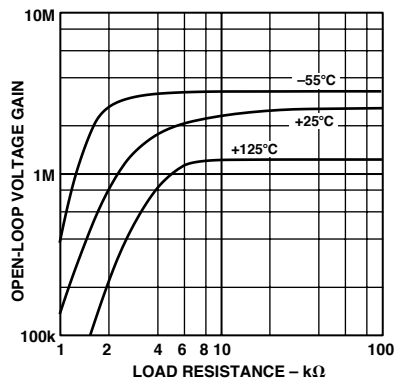


Figure 17. Open-Loop Gain vs. Load Resistance vs. Load Resistance

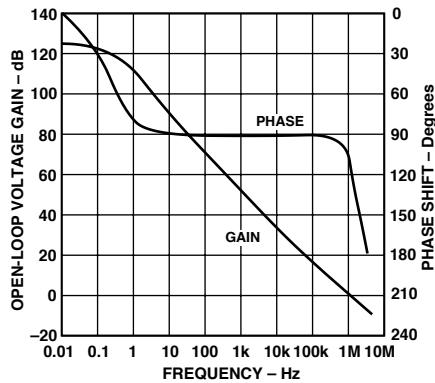


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

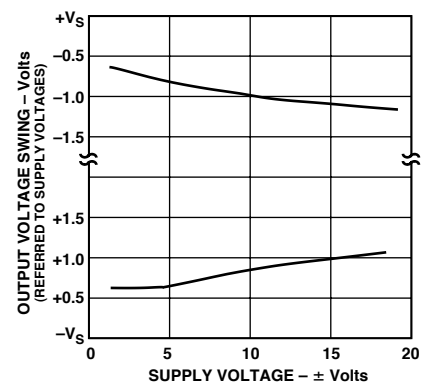


Figure 19. Output Voltage Swing vs. Supply Voltage

# AD706

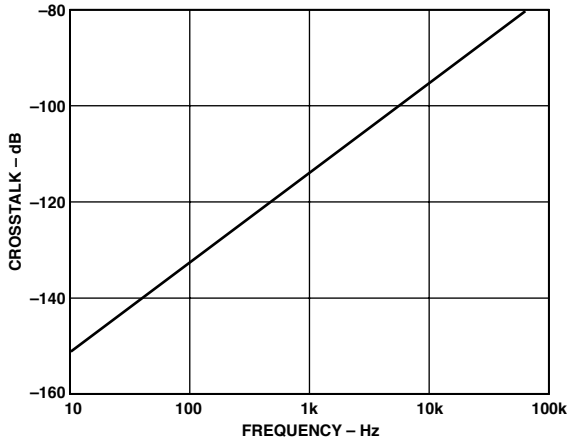


Figure 20a. Crosstalk vs. Frequency

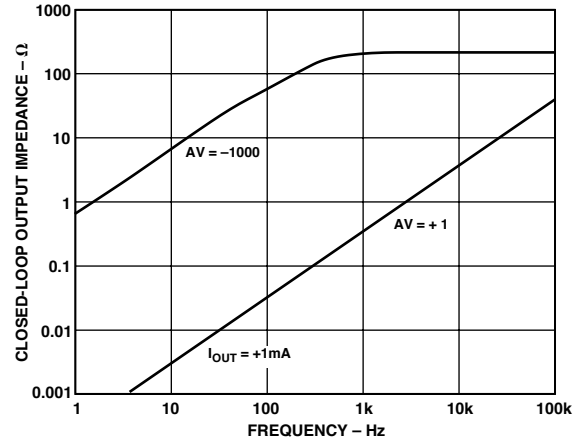


Figure 21. Magnitude of Closed-Loop Output Impedance vs. Frequency

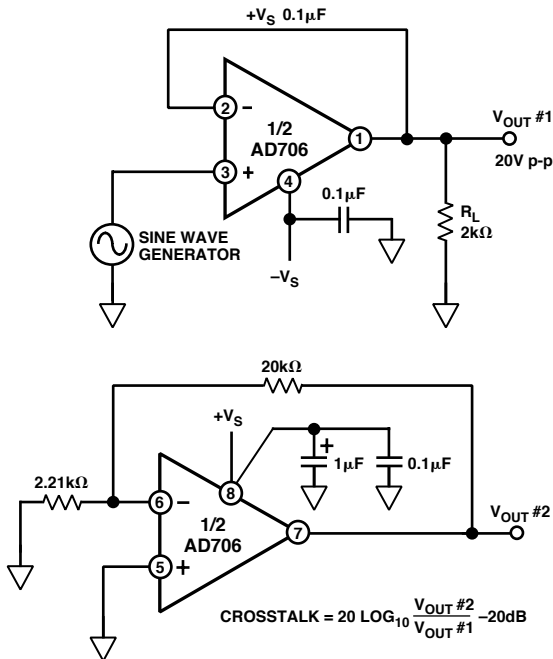


Figure 20b. Crosstalk Test Circuit

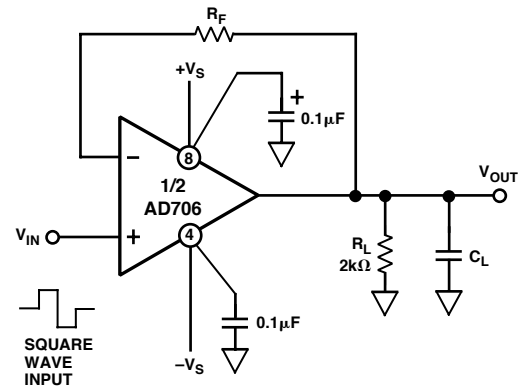


Figure 22a. Unity Gain Follower (For Large Signal Applications, Resistor  $R_F$  Limits the Current Through the Input Protection Diodes)

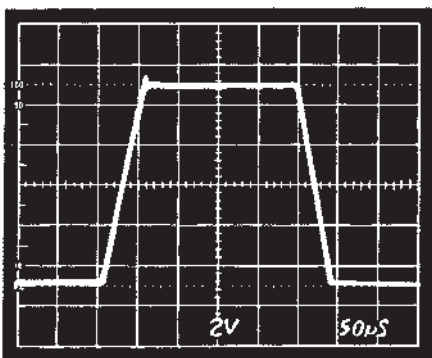


Figure 22b. Unity Gain Follower Large Signal Pulse Response,  $R_F = 10 \text{ k}\Omega$ ,  $C_L = 1,000 \text{ pF}$

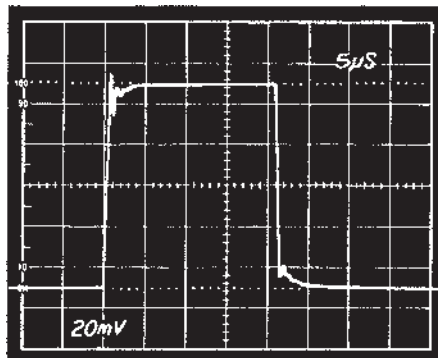


Figure 22c. Unity Gain Follower Small Signal Pulse Response,  $R_F = 0 \Omega$ ,  $C_L = 100 \text{ pF}$

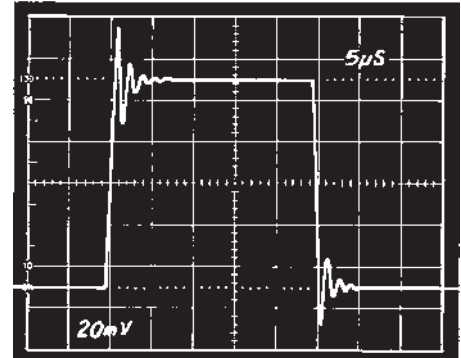


Figure 22d. Unity Gain Follower Small Signal Pulse Response,  $R_F = 0 \Omega$ ,  $C_L = 1000 \text{ pF}$

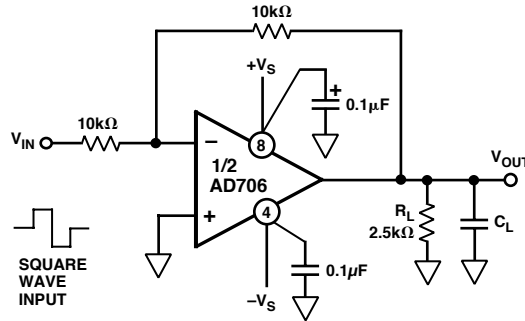


Figure 23a. Unity Gain Inverter Connection

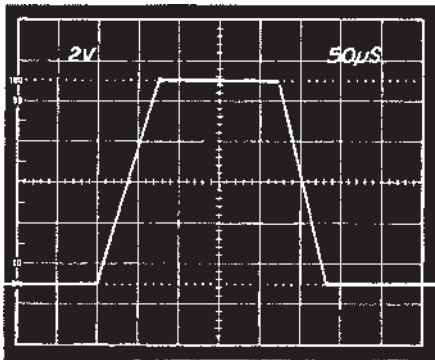


Figure 23b. Unity Gain Inverter Large Signal Pulse Response,  $C_L = 1,000 \text{ pF}$

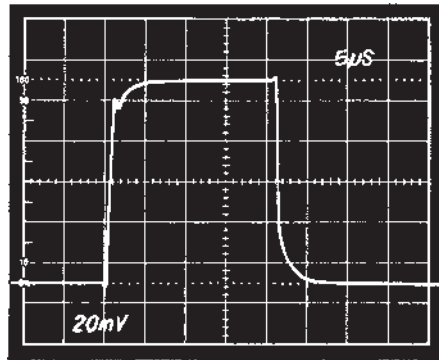


Figure 23c. Unity Gain Inverter Small Signal Pulse Response,  $C_L = 100 \text{ pF}$

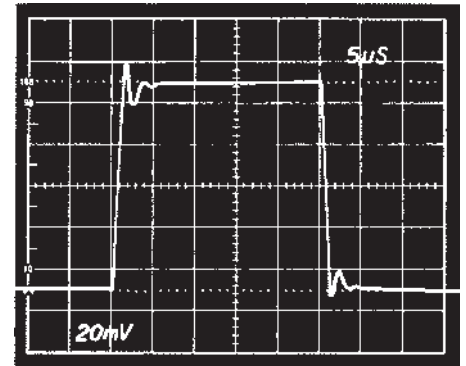


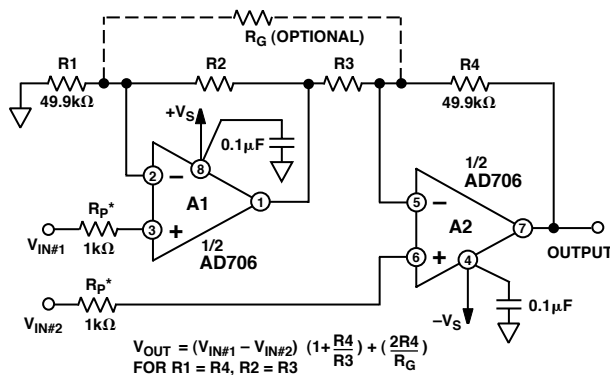
Figure 23d. Unity Gain Inverter Small Signal Pulse Response,  $C_L = 1000 \text{ pF}$

Figure 24 shows an in-amp circuit that has the obvious advantage of requiring only one AD706, rather than three op amps, with subsequent savings in cost and power consumption. The transfer function of this circuit (without  $R_G$ ) is:

$$V_{OUT} = (V_{IN\#1} - V_{IN\#2}) \left( 1 + \frac{R_4}{R_3} \right)$$

for  $R_1 = R_4$  and  $R_2 = R_3$

Input resistance is high, thus permitting the signal source to have an unbalanced output impedance.



\*OPTIONAL INPUT PROTECTION RESISTOR FOR GAINS GREATER THAN 100 OR INPUT VOLTAGES EXCEEDING THE SUPPLY VOLTAGE.

Figure 24. A Two Op-Amp Instrumentation Amplifier

Furthermore, the circuit gain may be fine trimmed using an optional trim resistor,  $R_G$ . Like the three op-amp circuit, CMR

increases with gain, once initial trimming is accomplished—but CMR is still dependent upon the ratio matching of Resistors  $R_1$  through  $R_4$ . Resistor values for this circuit, using the optional gain resistor,  $R_G$ , can be calculated using:

$$R_1 = R_4 = 49.9 \text{ k}\Omega$$

$$R_2 = R_3 = \frac{49.9 \text{ k}\Omega}{0.9G - 1}$$

$$R_G = \frac{99.8 \text{ k}\Omega}{0.06G}$$

where  $G = \text{Desired Circuit Gain}$

Table I provides practical 1% resistance values. (Note that without resistor  $R_G$ ,  $R_2$  and  $R_3 = 49.9 \text{ k}\Omega / (G - 1)$ .)

Table I. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 24

Circuit Gain	Gain of A1	Gain of A2	R2, R3	R1, R4
1.10	11.00	1.10	499 kΩ	49.9 kΩ
1.33	4.01	1.33	150 kΩ	49.9 kΩ
1.50	3.00	1.50	100 kΩ	49.9 kΩ
2.00	2.00	2.00	49.9 kΩ	49.9 kΩ
10.1	1.11	10.10	5.49 kΩ	49.9 kΩ
101.0	1.01	101.0	499 Ω	49.9 kΩ
1001	1.001	1001	49.9 Ω	49.9 kΩ

For a much more comprehensive discussion of in-amp applications, refer to the *Instrumentation Amplifier Applications Guide*—available free from Analog Devices, Inc.

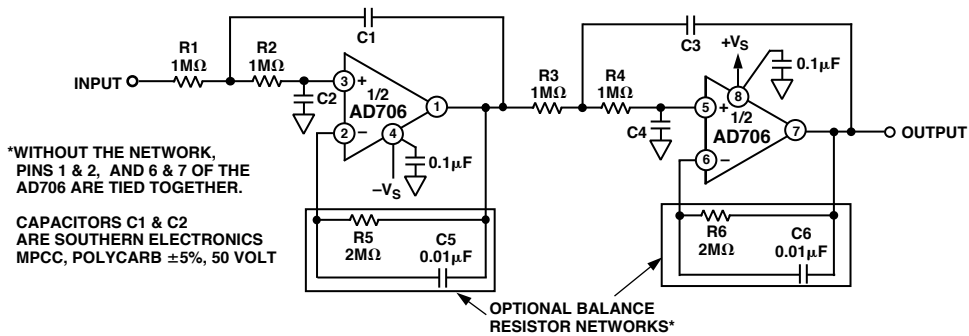


Figure 25. A 1 Hz, 4-Pole Active Filter

### A 1 Hz, 4-Pole, Active Filter

Figure 25 shows the AD706 in an active filter application. An important characteristic of the AD706 is that both the input bias current, input offset current and their drift remain low over most of the op amp's rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor. Adding the balancing resistor enhances performance at high temperatures, as shown by Figure 26.

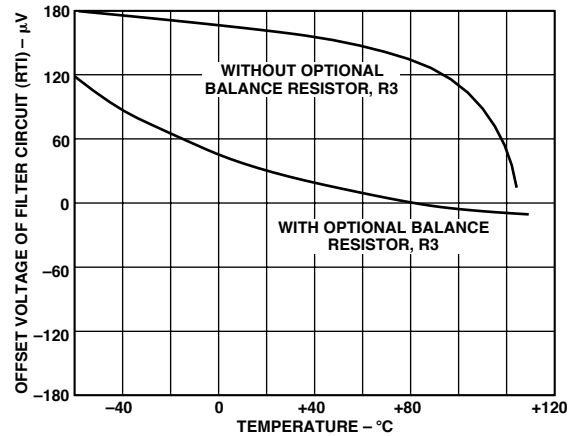


Figure 26.  $V_{OS}$  vs. Temperature Performance of the 1 Hz Filter

Table II. 1 Hz, 4-Pole, Low Pass Filter Recommended Component Values

Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

**NOTE**

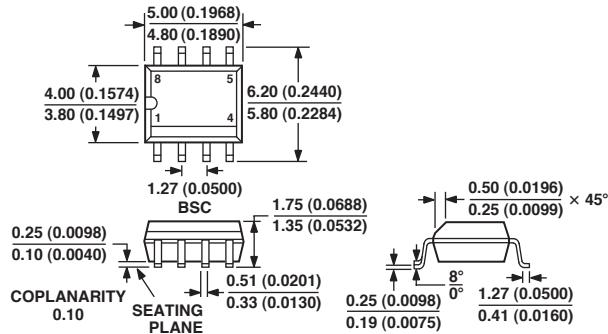
Specified Values are for a -3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly, i.e.: for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, C4 = 0.0205 μF.



OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]  
Narrow Body  
(RN-8)

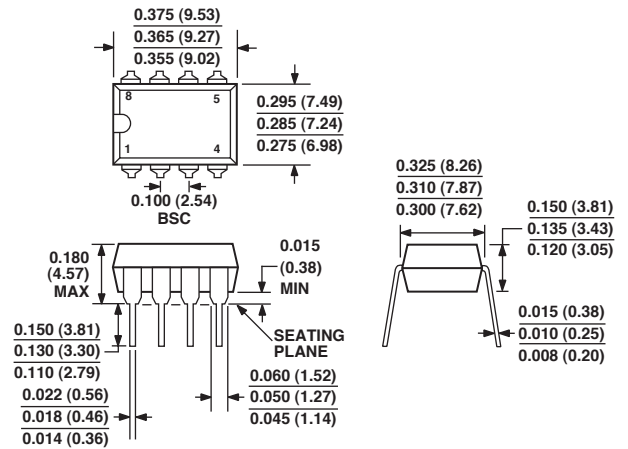
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual-in-Line Package [PDIP]  
(N-8)

Dimensions shown in inches and (millimeters).



COMPLIANT TO JEDEC STANDARDS MO-095AA  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES)

# AD706

## Revision History

Location	Page
<b>10/02--Data Sheet changed from REV. C to REV. D</b>	
Deleted 8-Lead CerDIP (Q-8) Package .....	Universal
Edits to FEATURES .....	1
Edits to PRODUCT DESCRIPTION .....	1
Edits to SPECIFICATIONS .....	2
Edits to ABSOLUTE MAXIMUM RATINGS .....	3
Edits to ORDERING GUIDE .....	3
Updated OUTLINE DIMENSIONS .....	15



