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LM3753/54

Scalable 2-Phase Synchronous Buck Controllers with Integrated FET Drivers and Linear Regulator Controller

General Description

The LM3753 and LM3754 are full featured single-output dual-phase voltage-mode synchronous PWM buck controllers. They can be configured to control from 2 to 12 interleaved power stages creating a single high power output. Both controllers utilize voltage-mode control with input voltage feed-forward for high noise immunity. An internal average current loop forces real time current sharing between phases during load transients.

The LM3753 supports a Tracking function, while the LM3754 supports adjustable Soft-Start. The LM3753 Tracking is always enabled, so the output is controlled both up and down. The Soft-Start function on the LM3754 can only drive the output upwards – it will not pull it down, therefore, pre-biased loads will not be discharged. Available in the 5 mm x 5 mm thermally enhanced 32-lead LLP package with a thermal pad.

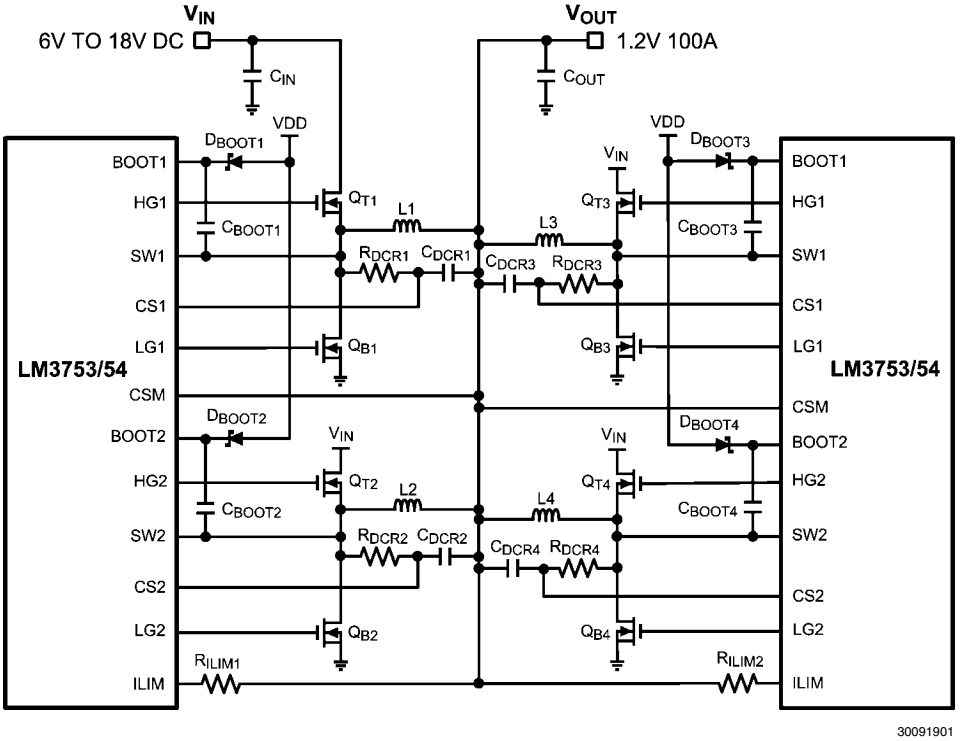
Features

- Wide input voltage range of 4.5V to 18V
- Up to 12 channels for 300A load
- System accuracy better than 1%
- 0.6V to 3.6V output voltage range
- Switching frequency from 200 kHz to 1 MHz
- Phase current sharing ±12% max over temperature
- Integrated 4.35V ±2.3% LDO
- Inductor DCR or sense resistor current sensing
- Interleaved switching for low I/O ripple current
- Integrated synchronous NFET drivers
- Programmable Soft-Start (LM3754) or Tracking (LM3753)
- Pre-biased startup (LM3754)
- Output voltage differential remote sensing
- Minimum controllable on-time of only 50 ns
- Programmable Enable and input UVLO
- Power Good flag
- OVP, UVP and hiccup over-current protection

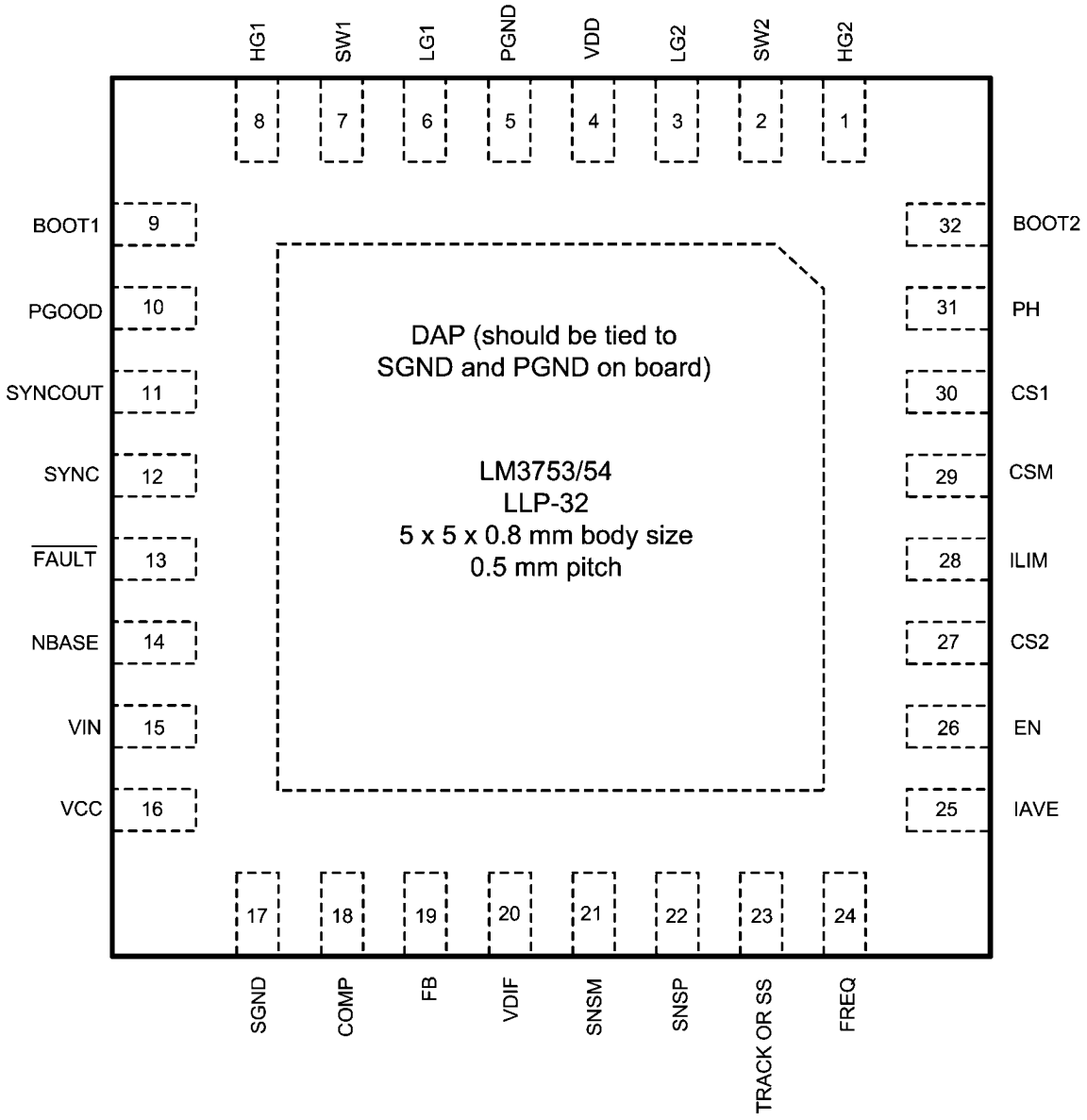
Applications

- CPUs, GPUs (graphic cards), ASICs, FPGAs, Large Memory Arrays, DDR
- High Current POL Converters
- Networking Systems
- Power Distribution Systems
- Telecom/Datacom DC/DC Converters
- Desktops, Servers and Workstations

Simplified Application



Connection Diagram



Top View
32-Lead LLP

Ordering Information

Order Number	TRACK/SS function	Package Type	NSC Package Drawing	Supplied As
LM3753SQ	TRACK	LLP-32	SQA32A	1000 Units / Reel
LM3753SQX	TRACK	LLP-32	SQA32A	4500 Units / Reel
LM3754SQ	SS Pre-Bias Protection	LLP-32	SQA32A	1000 Units / Reel
LM3754SQX	SS Pre-Bias Protection	LLP-32	SQA32A	4500 Units / Reel

Pin Descriptions

Pin Number	Pin Name	Description
1	HG2	Gate drive of the high-side N-channel MOSFET for Phase 2.
2	SW2	Switching node of the power stage of Phase 2.
3	LG2	Gate drive of the low-side N-channel MOSFETs for Phase 2.
4	VDD	Power supply for gate drivers. Decouple VDD to PGND with a ceramic capacitor. VDD can either be supplied by an external 5V ±10% bus, or by the internal regulator, which uses an external NPN pass device. If using the internal regulator, connect VDD to the emitter of the NPN pass device.
5	PGND	Power Ground. Tie PGND and SGND together on the board through the DAP.
6	LG1	Gate drive of the low-side N-channel MOSFETs for Phase 1.
7	SW1	Switching node of the power stage of Phase 1.
8	HG1	Gate drive of the high-side N-channel MOSFET for Phase 1.
9	BOOT1	Bootstrap of Phase 1 for the high-side gate drive power supply.
10	PGOOD	Power Good open-drain output. Active HIGH.
11	SYNCOUT	Synchronization Output. For multi-controller systems this pin should be connected to the SYNC pin of the next controller in daisy-chain configuration
12	SYNC	Synchronization Input. SYNCOUT of one controller is connected to SYNC of the next controller in a daisy-chain fashion. To synchronize the whole chain of controllers to an external clock, wire the external clock to the SYNC pin of the first controller of the chain (called the Master controller). Otherwise, connect the SYNC input of the Master controller to ground and all of the controllers will be controlled by the internal oscillator of the Master.
13	$\overline{\text{FAULT}}$	Input/Output. Wire the $\overline{\text{FAULT}}$ pin of all controllers together. $\overline{\text{FAULT}}$ gets pulled Low during startup, an over-current fault, or an over-voltage fault. $\overline{\text{FAULT}}$ = Low signals all controllers to stop switching and prepare for the next startup sequence. The first LM3753/54 in the system (the Master) supplies the $\overline{\text{FAULT}}$ pin pull-up current for all of the controllers.
14	NBASE	Connect to the base of external series-pass NPN if using the LM3753/54 internal LDO controller to generate VDD. Otherwise leave unconnected.
15	VIN	Input Voltage. Connect VIN to the input supply rail used to supply the power stages. This input is used to provide the feed-forward for the voltage control of V_{OUT} and for generating the internal VCC voltage.
16	VCC	Supply for internal control circuitry. Decouple VCC to PGND with a ceramic capacitor. When VIN > 5.5V, the internal LDO will supply 4.35V to this pin. When 4.5V < VIN < 5.5V, connect VIN to VCC. In this case the internal VCC LDO will turn off and VCC current will be supplied directly by VIN.
17	SGND	Signal Ground. Tie PGND and SGND together on the board through the DAP.
18	COMP	Error Amplifier Output. For the Master, a compensation network is placed between the COMP pin and the FB pin. The COMP pin of the Master should be connected to the SNSP pin of each of the Slaves. The COMP pin of each of the Slaves must be connected to its VDIF pin
19	FB	Feedback Input. This is the inverting input of the error amplifier. Connect the Master FB pin to the output voltage divider and compensation network. Connect each Slave FB pin to its own VCC pin. This will put that controller in Slave mode and disable its error amplifier.
20	VDIF	Output of the remote-sense differential amplifier. Connect the Master VDIF pin to the output voltage divider and compensation network. The Slave differential amplifier is used to buffer COMP from the Master controller. Connect each Slave VDIF pin to its own COMP pin.
21	SNSM	Inverting input of the remote-sense differential amplifier. Connect SNSM of the Master controller to PGND at the load point. On Slave controllers, the differential amplifier is used to buffer COMP from the Master controller. Connect SNSM of each Slave controller directly to the Master controller SGND pin.
22	SNSP	Non-inverting input of the remote-sense differential amplifier. Connect the SNSP of the Master controller to V_{OUT} at the load point. On Slave controllers, the differential amplifier is used to buffer COMP of the Master controller. Connect SNSP of each Slave controller to the Master controller COMP pin.

Pin Number	Pin Name	Description
23	TRACK (LM3753)	Tracking Input. Connect the TRACK pins of all of the controllers in the system together. Wire the TRACK pin to the external TRACK control signal. Tracking is always enabled on power-up, shutdown and brownout.
23	SS (LM3754)	Soft-Start. Connect the SS pins of all of the controllers in the system together. At the Master controller, connect a soft-start capacitor between SS and SGND. Only the Master controller supplies the pull up current to the SS capacitor.
24	FREQ	Frequency Adjust. A frequency adjust resistor and decoupling capacitor are connected between FREQ and SGND to program the switching frequency between 200 kHz to 1 MHz (each phase). These components must be supplied on the Master and Slaves, even if the system is synchronized to an external clock.
25	IAVE	Current Averaging. Connect a 4.02 kΩ, 1%, resistor between each controller's IAVE pin and SGND. In the case where one phase is not used, connect an 8.06 kΩ resistor. Connect a filter capacitor between IAVE and SGND at each controller,
26	EN	Enable Input. Used for VIN UVLO function, connect EN to the midpoint of a voltage divider from VIN to SGND. The EN pins of all controllers must be wired together. For an on/off EN function, wire the EN pins of all controllers together and control with an open drain output.
27	CS2	Positive current-sense input of Phase 2. Connect to the DCR network or the current-sense resistor of Phase 2. The negative current-sense input is the CSM pin.
28	ILIM	Current Limit Set. Connect a resistor between ILIM and CSM. The resistance between ILIM and CSM programs the current limit.
29	CSM	Negative current-sense input of the internal current-sense amplifiers. Connect to V_{OUT}.
30	CS1	Positive current-sense input of Phase 1. Connect to the DCR network or the current-sense resistor of Phase 1. The negative current-sense input is the CSM pin.
31	PH	Phase Select Input. Connect this pin to the middle of a resistor divider between VCC and SGND to program the number of phases in the system.
32	BOOT2	Bootstrap pin of Phase 2 for the high-side gate drive power supply.
	DAP	Die Attach Pad. Must be connected to PGND and SGND but cannot be used as the primary ground connection; do not place any traces or vias other than GND in the outer layer under the DAP; see AN-1187 application note.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN to SGND, PGND	−0.3V to 24V
SGND to PGND	−0.3V to 0.3V
VCC and VDD to VIN	+0.3V
VDD to PGND	−0.3V to 6V
PGOOD, $\overline{\text{FAULT}}$ to SGND	−0.3V to 6V
VCC, EN, SS, TRACK, SYNC, CS1, CS2, CSM, ILIM, SNSM, SNSP to SGND	−0.3V to 6V
FREQ, PH, FB to SGND	−0.3 to VCC + 0.3V
BOOT1, BOOT2 to PGND (*Note 2*)	−0.3V to 24V Peak
SW1, SW2 to PGND (*Note 2*)	−0.3VDC to 24V Peak −3V for less than 40 ns
BOOT1 to SW1, BOOT2 to SW2 (*Note 2*)	−0.3V to 6.0V Peak
SYNCOUT	±20 mA
PGOOD, $\overline{\text{FAULT}}$	±20 mA
VDIF	±5 mA
COMP	±4 mA
ESD Rating	
HBM (*Note 3*)	2 kV
Junction Temperature ($T_{J\text{-}MAX}$)	+150°C
Storage Temperature Range	−65°C to +150°C

Operating Ratings (*Note 1*)

VIN Low Range	4.5V to 5.5V
VIN High Range when using integrated VCC LDO	5.5V to 18V
VIN High Range when using integrated VDD linear regulator controller	6V to 18V
VCC External Supply Voltage	4.5V to 5.5V
VDD External Supply Voltage	4.5V to 5.5V
Output Voltage Range	0.6V to 3.6V
TRACK	0V to 5V
SYNC, EN	0V to 5.5V
SNSM	−0.25V to 1.0V
SNSP to SNSM	0V to 3.6V
IAVE	0V to 1.15V
CS1 and CS2 to CSM	−15 mV to 45 mV
CS1, CS2, ILIM and CSM to SGND	0V to 3.6V
ILIM to CSM	0V to 200 mV
Junction Temperature Range	−5°C to +125°C
Thermal Data	
Junction-to-Ambient Thermal Resistance (θ_{JA}), LLP-32 Package (*Note 4*)	26.4°C/W

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of −5°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated V_{VIN} = 12V, V_{VDD} = 5V, V_{VCC} = internal LDO, V_{EN} = 2V, R_{FRQ} = 78.7 kΩ, V_{PH} = 0V, V_{CS1} = V_{CS2} = V_{CSM} = V_{SS} = V_{TRACK} = V_{SNSP} = 1.8V, V_{ILIM} − V_{CSM} = 100 mV, V_{SNSM} = V_{SYNC} = 0V, $V_{SYNCOUT}$ floating.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
System Accuracy						
V_{OUT}	Output Voltage Accuracy Includes trimmed EA and diff amplifier offset and gain errors; 0.5 mA load at VDIF	V_{OUT} = 3.6V	**−0.65**	−0.11	**0.45**	%
		V_{OUT} = 2.5V	**−0.75**	−0.134	**0.6**	%
		V_{OUT} = 1.8V	**−0.9**	−0.165	**0.7**	%
		V_{OUT} = 0.6V	**−2.25**	−0.4	**1.25**	%
Phase Current Equalization						
ΔI_{PH}	Current Equalization (from average per phase current)	V_{CSM} = 1.8V, V_{CS1} = V_{CS2} = V_{CSM} + 30 mV, V_{IAVE} = 740 mV, V_{COMP} = 1.9V	**−12**		**12**	%
System Supplies and UVLO						
VIN						
I_{VIN}	VIN Operating Current	2-phase switching gate drivers unloaded		15		mA
$I_{VIN\text{-}Q}$	VIN Quiescent Current	V_{FB} = 650 mV, no PWM switching, NBASE is floating (no NPN)		9	**18**	mA
$I_{VIN\text{-}SD}$	VIN Shutdown Current	V_{EN} = 0V		200	**450**	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC						
V_{VCC}	VCC Linear Regulator Output Voltage	0 to 3 mA sourced to an external load; V_{VIN} = 5.5V to 18V	**4.25**	4.35	**4.45**	V
I_{VCC}	VCC Input Current from External Supply	V_{VIN} = 5.5V, V_{VCC} = 5.5V		10	**20**	mA
I_{VCC-SD}	VCC Input Shutdown Current from External Supply	V_{EN} = 0V, V_{VIN} = 12V, V_{VCC} = 5V		260		µA
$I_{VCC-LIM}$	VCC Output Current Limit	V_{VCC} = 2.5V	**9**	30	**53**	mA
		V_{VCC} = 0V		50		
V_{VCC-EN}	VCC UVLO Thresholds	V_{VCC} Rising	**4.04**	4.14	**4.24**	V
		V_{VCC} Falling	**3.9**	4	**4.1**	
$V_{VCC-HYS}$	VCC Threshold Hysteresis			140		mV
t_{D-VCC}	VCC UVLO/UVP Debounce Time			8		µs
VDD, NBASE, BOOT1, BOOT2, SW1, SW2						
V_{VDD}	VDD Controller Regulation Voltage	V_{VIN} = 6V to 18V	**4.6**	4.85	**5.1**	V
V_{NBASE}	VIN-to-NBASE Dropout	V_{VIN} – 5.5V, 700 mV source connected from VDD to NBASE, I_{NBASE} = 5 mA		330		mV
		V_{VIN} – 5.5V, 700 mV source connected from VDD to NBASE, I_{NBASE} = 1 mA		130		
$V_{NBASE-REG}$	NBASE Load Regulation	V_{VIN} = 18V, 700 mV source connected from VDD to NBASE, I_{NBASE} steps 1 mA to 5 mA		4		mV
I_{VDD}	VDD Operating Current from External Power Supply	V_{VDD} = V_{VIN} = V_{VCC} = 5.5V, f_{SW} = 300 kHz, Gate Drivers unloaded		1		mA
I_{VDD-SD}	VDD Shutdown Current	V_{EN} = 0V, V_{VIN} = 12V, V_{VDD} = 5V		2	**30**	µA
$I_{NBASE-CL}$	NBASE Current Limit	V_{NBASE} = V_{VDD} + 0.7V, ΔV_{VDD} = –100 mV	**5.8**	10		mA
		V_{NBASE} = V_{VDD} = 0V		20		
$I_{BOOT-SD}$	BOOT1, BOOT2 Shutdown Current	V_{EN} = 0V, $V_{SW1(2)}$ = 0V, V_{BOOT} – V_{SW} = 5V		4.5	**15**	µA
I_{BOOT}	BOOT1, BOOT2 Operating Current	$V_{BOOT1(2)}$ = 17.0V, $V_{SW1(2)}$ = 12.0V, f_{SW} = 300 kHz, Gate Drivers unloaded		650		µA
I_{SW}	SW1, SW2 Leakage Current with Pre-Biased Output	V_{VCC} = 0V, V_{EN} = 0V, $V_{SW1(2)}$ = 3.6V		3		µA
V_{VDD-TH}	VDD UVLO Thresholds	V_{VDD} Rising	**3.8**	4.02	**4.28**	V
		V_{VDD} Falling	**3.37**	3.71	**4.03**	V
$V_{VDD-HYS}$	VDD UVLO/UVP Hysteresis			310		mV
t_{D-VDD}	VDD UVLO/UVP Debounce Time			11		µs
Thermal Shutdown						
T_{J-SD}	Thermal Shutdown Threshold	Rising		160		°C
T_{J-HYS}	Thermal Shutdown Threshold Hysteresis			30		°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EN						
V_{EN-H}	HIGH Level Input Voltage		**1.51**			V
V_{EN-L}	LOW Level Input Voltage				**1.14**	V
V_{EN-TH}	EN Threshold	V_{VIN} = 4.5V to 18V, V_{VCC} = 4.5V (Rising)	**1.26**	1.39	**1.51**	V
		V_{VIN} = 4.5V to 18V, V_{VCC} = 4.5V (Falling)	**1.14**	1.25	**1.35**	V
V_{EN-HYS}	EN Threshold Hysteresis			140		mV
I_{EN}	EN Input Bias Current	V_{EN} = 1.5V		0.1		µA
		V_{EN} = 1.0V		0.4	**1.7**	
Reference, Feedback & Error Amplifier: FB, COMP						
V_{FB}	FB Voltage Under Regulation	V_{COMP} = 1.8V	**0.593**	0.599	**0.605**	V
$V_{FB-REG1}$	FB Voltage VIN Line Regulation	V_{VIN} = 5.5V to 18V		±0.01		%
$V_{FB-REG2}$	FB Voltage VCC Line Regulation	V_{VCC} = V_{VIN} = V_{VDD} = 4.5V to 5.5V (same source)		±0.15		%
I_{FB}	FB Input Bias Current			45	**130**	nA
V_{FB-PTH}	FB Pin Master/Slave Programming Threshold			3.2		V
A_{OL}	DC Gain	FB to COMP, V_{COMP} = V_{FB} + 1.0V		70		dB
f_{BW}	Error Amplifier Unity Gain Bandwidth	$R_{COMP-SGND}$ = 1.5 kΩ, $C_{COMP-SGND}$ = 50 pF		15		MHz
$V_{COMP-SLEW}$	Error Amplifier Slew Rate			6		V/µS
$V_{COMP-REG}$	COMP Load Regulation, Sourcing	V_{COMP} = 2.7V, ΔI_{COMP} = +1 mA, DC Gain = 40		−3		mV
PWM Ramp and Input Voltage Feed-Forward						
D_{MAX}	Maximum Duty Cycle Controlled by Clock	V_{VIN} = 6V, V_{COMP} = 3.5V	**81**			%
D_{FF}	Duty Cycle Controlled by VIN Feed-Forward	V_{VIN} = 9V, V_{COMP} = 2.2V		42		%
t_{ON-MIN}	Minimum Controllable On-Time			50		ns
$V_{RAMP-MIN}$	PWM Ramp Range	Ramp Minimum		1.3		V
$V_{RAMP-MAX}$		Ramp Maximum		2.8		V
V_{RAMP}	PWM Ramp Amplitude			1.5		V
Differential Amplifier: SNSP, SNSM, VDIF						
$V_{OS-INPUT}$	Input Offset Voltage	V_{SNSP} = 1.8V		3		mV
$R_{INPUT-SNSP}$	Input Resistance of SNSP			30		kΩ
A_{V-DIF}	Gain	V_{SNSP} = 0.6V to 3.6V	**0.996**	1	**1.004**	V/V
f_{BW-DIF}	3dB Bandwidth			2		MHz
$V_{DIF-REG1}$	VDIF Load Regulation, Sourcing	V_{VDIF} = 3.6V, I_{VDIF} = 0.5 mA	**−3**			mV
$V_{DIF-REG2}$	VDIF Load Regulation, Sourcing	V_{VDIF} = 0.6V, I_{VDIF} = 0.5 mA	**−3**			mV
Current-Sense, Current Limit and Hiccup Mode: CS1, CS2, CSM, ILIM						
V_{CS-OS}	Current-Sense Input Offset Voltage Range, $V_{CS1(2)}$ − V_{CSM}	V_{OUT} = 1.8V		±2		mV
I_{CS}	CS1, CS2 Input Bias Current	V_{CSM} = 3.6V, $V_{CS1(2)}$ − V_{CSM} = −15 mV and +40 mV	**−200**		**200**	nA
		V_{CSM} = 0.6V, $V_{CS1(2)}$ − V_{CSM} = −15 mV and +40 mV	**−450**		**450**	nA
I_{CSM}	CSM Input Source Bias Current	V_{CSM} = 0.6V and 3.6V, $V_{CS1(2)}$ − V_{CSM} = 40 mV		150	**240**	µA
I_{CSL}	CS1+ CS2 + CSM + ILIM Leakage Current with Pre-Biased Output	V_{VCC} = 0V, V_{EN} = 0V, V_{CSM} = V_{CS1} = V_{CS2} = V_{ILIM} = 3.6V		0.1		µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{BW-CS}	3dB Bandwidth, CS1(2) to PWM COMPARATOR Input			1.0		MHz
$I_{ILIM-SOURCE}$	ILIM Source Current	V_{ILIM} = 0.6V to 3.6V, V_{VIN} = 5.5V	**85**	94	**103**	µA
V_{CL}	Current Limit Threshold Voltage $V_{ILIM} - V_{CS1(2)}$	V_{ILIM} = 0.6V to 3.6V, V_{VIN} = 5.5V	**–2.5**	0	**4.6**	mV
t_{D-CL}	Current Limit Comparator Propagation Delay	V_{CS1} or V_{CS2} stepped from 0.9V to 1.1V, V_{ILIM} = 1V		200		ns
t_{D-ILIM}	Master or Slave Fast Current Limit Delay	V_{FB} = 280 mV, 1-phase over-current: V_{CS1} OR $V_{CS2} > V_{ILIM}$		7		Switch cycles
		V_{FB} = 280 mV, 2-phase over-current: V_{CS1} AND $V_{CS2} > V_{ILIM}$		3		Switch cycles
$t_{D-HICCUP}$	Master or Slave Over-Current Hiccup Mode Delay	1-phase over-current: V_{CS1} OR $V_{CS2} > V_{ILIM}$		446		Switch cycles
		2-phase over-current: V_{CS1} AND $V_{CS2} > V_{ILIM}$		223		Switch cycles
$t_{D-COOL-DOWN}$	Hiccup Over-Current Cool-Down Time			6		ms
Power Good: PGOOD, OVP, UVP						
V_{OVP}	OVP Threshold	V_{FB} rising edge	**125**	130	**135**	$\%V_{FB}$
$t_{D-RESTART}$	OVP Restart Delay			2		ms
$N_{OVP-LATCH}$	Number of OVP Events Before Latch-Off			7		
V_{UVP}	UVP Threshold	V_{FB} falling edge	**75**	80	**85**	$\%V_{FB}$
$V_{UVP-HYS}$	UVP Threshold Hysteresis			25		mV
$t_{D-OVP/UVP}$	OVP/UVP Debounce Time			5		µs
V_{PG-LO}	PGOOD Low Level	I_{PGOOD} = –4 mA		0.14	**0.25**	V
$I_{PG-LEAK}$	PGOOD Leakage Current	V_{PGOOD} = 5.5V		5	**300**	nA
$\overline{\text{FAULT}}$						
$I_{\overline{FAULT}}$	Internal Pullup Current in Master Mode			325		µA
$V_{OL-\overline{FAULT}}$	$\overline{\text{FAULT}}$ Output Low Level	$I_{\overline{FAULT}}$ sinking 500 µA		0.21		V
$V_{OH-\overline{FAULT}}$	$\overline{\text{FAULT}}$ Output High Level	$I_{\overline{FAULT}}$ sourcing 50 µA		VCC – 0.1		V
Oscillator and Synchronization (PLL): SYNC, SYNCOUT, FREQ						
f_{SW-MIN}	Minimum Switching Frequency	R_{FRQ} = 121 kΩ		200		kHz
f_{SW-MAX}	Maximum Switching Frequency	R_{FRQ} = 21.3 kΩ		1000		kHz
f_{SW}	Switching Frequency Accuracy	R_{FRQ} = 78.7 kΩ	**282**	300	**318**	kHz
f_{SYNC}	SYNC Frequency Capture Range	200 kHz to 1 MHz		±25		%
$V_{SYNC-RISE}$	SYNC Rising Threshold			1.46	**1.68**	V
$V_{SYNC-FALL}$	SYNC Falling Threshold		**1.12**	1.3		V
$t_{SYNC-MIN}$	SYNC Minimum Pulse Width			150		ns
I_{SYNC}	SYNC Bias Current (internal or external VCC)	V_{SYNC} = 0 to 5.5V	**–15**		**25**	µA
$V_{SYNCOUT-HI}$	SYNCOUT Logic High Level	Sourcing 10 mA, V_{VCC} = 4.5V external	**VCC – 0.42**			V
$V_{SYNCOUT-LO}$	SYNCOUT Logic Low Level	Sinking 10 mA, V_{VCC} = 4.5V external			**0.48**	V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PH_{RATIO}	V_{PH}/V_{VCC} Divider Ratio to Set Phase Number	2 & 4 Phases		0	**0.138**	
		3 Phases	**0.152**	3/14	**0.279**	
		5 Phases	**0.294**	5/14	**0.418**	
		6 Phases	**0.438**	7/14	**0.562**	
		8 Phases	**0.587**	9/14	**0.703**	
		10 Phases	**0.730**	11/14	**0.844**	
		12 Phases	**0.874**	1		
I_{PH}	PH Bias Current	V_{VCC} = 4.5V forced, V_{PH} = 0 to V_{VCC}	**–150**		**150**	nA
Φ_{HG1-N2}	HG1 to HG2 Phase Shift for 2, 4, 6, 8, 10 or 12-Phase Modes			180		°
Φ_{HG1-N3}	HG1 to HG2 Phase Shift for 3-Phase Mode			240		°
Φ_{HG1-N5}	HG1 to HG2 Phase Shift for 5-Phase Mode			216		°
Φ_{SYNC}	SYNC to SYNCOUT Phase Shift for N-phase Operation	N > 2		360/N		°
		N = 2		90		
$t_{SYNC-ERR}$	SYNC to SYNCOUT Phase Shift Error			5		ns
$t_{SYNC-HG}$	SYNC to HG1(2)			165		ns
Φ_{HG-ERR}	HG1 and HG2 Controller-to-Controller Phase Delay Error	300 kHz, 6-phase		5		°
Soft-Start (LM3754): SS, Pre-Biased Startup						
I_{SS}	SS Source Current	V_{SS} = 0.3V	**5.7**	10	**14.6**	µA
R_{DS-SS}	Soft-Start Pull-Down Resistance			750		Ohm
t_{LG-PW1}	First LG High Pulse Width during Soft-Start			460		ns
t_{LG-GT}	LG Asynchronous-to-Synchronous Gradual Transition Time			2		ms
$t_{D-EN-SW}$	EN-to-Switching Delay	Delay from EN = High to $\overline{FAULT}$ = High; no pre-bias		2		ms
Tracking (LM3753): TRACK						
V_{TRACK}	Tracking Range		0		V_{REF}	V
$V_{HYS-TRACK}$	TRACK Falling Voltage Hysteresis			50		mV
t_{SS-INT}	Internal SS Time during $\overline{Fault}$ Recovery	After $\overline{Fault}$		3.8		ms
I_{TRACK}	TRACK Input Bias Current	V_{TRACK} = 0.3V		5	**200**	nA
		V_{TRACK} = 5V		0.2		mA
t_{LG-PW1}	First LG = High Pulse Width during $\overline{Fault}$ Recovery			460		ns
t_{LG-GTF}	LG Asynchronous-to-Synchronous Gradual Transition Time during $\overline{Fault}$ Recovery			1.8		ms
$t_{D-EN-SW}$	EN-to-Switching Delay	Delay from EN = High to $\overline{FAULT}$ = High; no pre-bias; V_{TRACK} = 0.6V		2		ms

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Gate Drivers						
$I_{PK-HG-SOURCE}$	HG1 and HG2 Peak Source Current	Less than 100 ns		1.9		A
$R_{HG-SOURCE}$	HG1 and HG2 Source Resistance	$V_{BOOT} - V_{SW} = 5V$		2.5		Ω
$I_{PK-HG-SINK}$	HG1 and HG2 Peak Sink Current	Less than 100 ns		4		A
$R_{HG-SINK}$	HG1 and HG2 Sink Resistance	$V_{BOOT} - V_{SW} = 5V$		1		Ω
$I_{PK-LG-SOURCE}$	LG1 and LG2 Peak Source Current	Less than 100 ns		2.3		A
$R_{LG-SOURCE}$	LG1 and LG2 Source Resistance			2		Ω
$I_{PK-LG-SINK}$	LG1 and LG2 Peak Sink Current	Less than 100 ns		4		A
$R_{LG-SINK}$	LG1 and LG2 Sink Resistance			1		Ω
$R_{HG-PULLDOWN}$	HG-SW Pull-Down Resistor			16		kΩ
$R_{LG-PULLDOWN}$	LG-PGND Pull-Down Resistor			16		kΩ
$t_{D-HG-LG}$	HG Falling to LG Rising Cross-Conduction Protection Delay (Dead-Time)	SW node not switching		30		ns
$t_{D-LG-HG}$	LG Falling to HG Rising Delay			28		ns
$t_{DS-HG-LG}$	HG Falling to LG Rising Cross-Conduction Protection Delay (Dead-Time)	SW node switching		10		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For guaranteed specifications and conditions, see the Electrical Characteristics table.

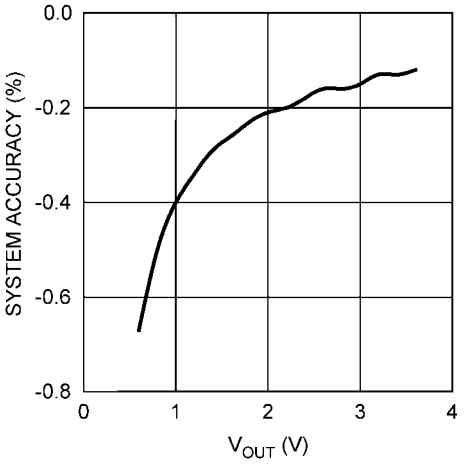
Note 2: Peak is the dc plus transient voltage including switching spikes.

Note 3: Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Applicable standard is JESD22-A114C. All pins pass 2 kV HBM except VDD, VIN and VCC which are rated for 1.5 kV.

Note 4: Tested on a four layer JEDEC board. Four vias provided under the exposed pad. See JEDEC standards JESD51-5 and JESD51-7.

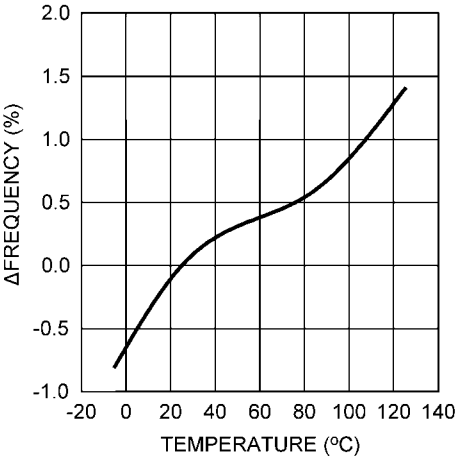
Typical Performance Characteristics

System Accuracy vs V_{OUT}



30091904

f_{SW} vs Temperature



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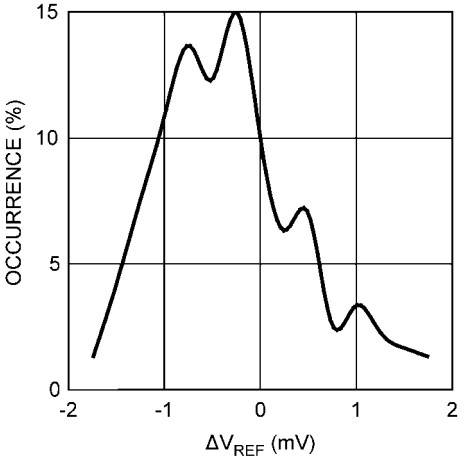
V_{REF} Deviation



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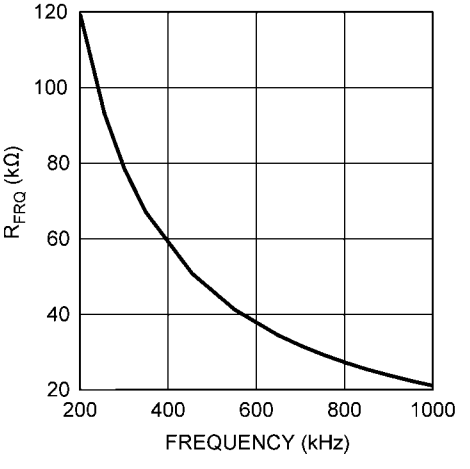
R_{FRQ} vs f_{SW}



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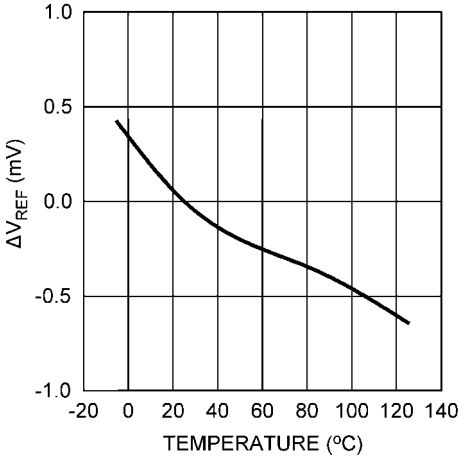
V_{REF} vs Temperature



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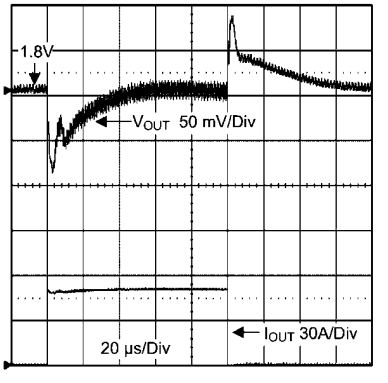
Load Step (High Slew)



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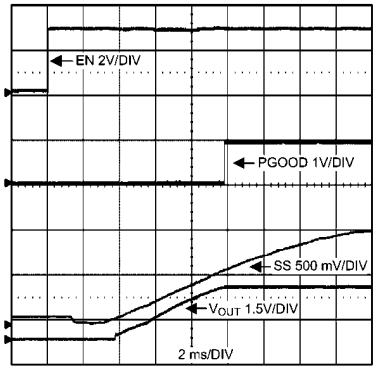
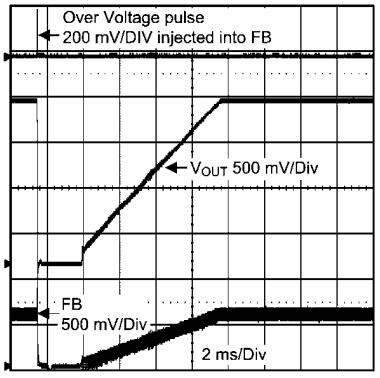
LM3754 (SS) Startup from 0V



30091910

Over-Voltage Fault



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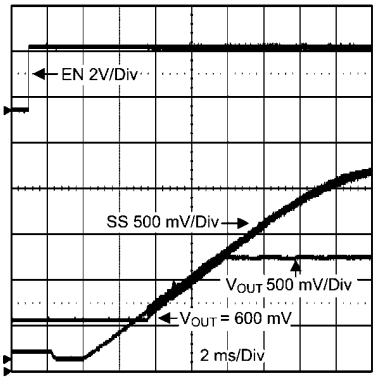
LM3754 (SS) Pre-Biased Output Startup



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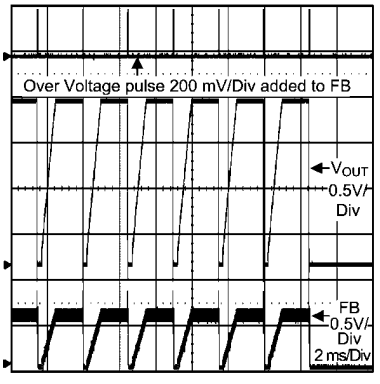
Repeated Over-Voltage Conditions



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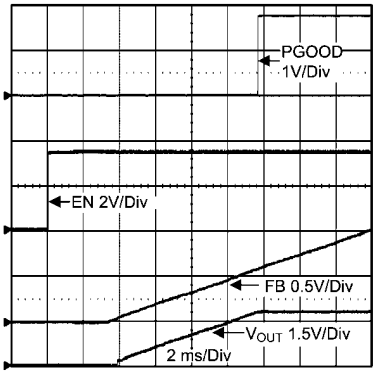
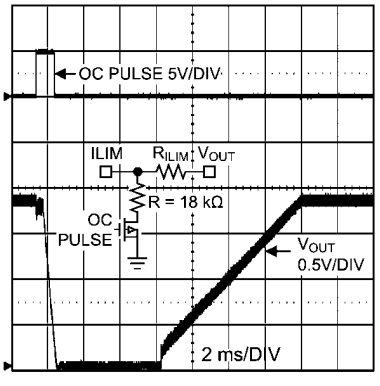
LM3753 (TRACK) Startup



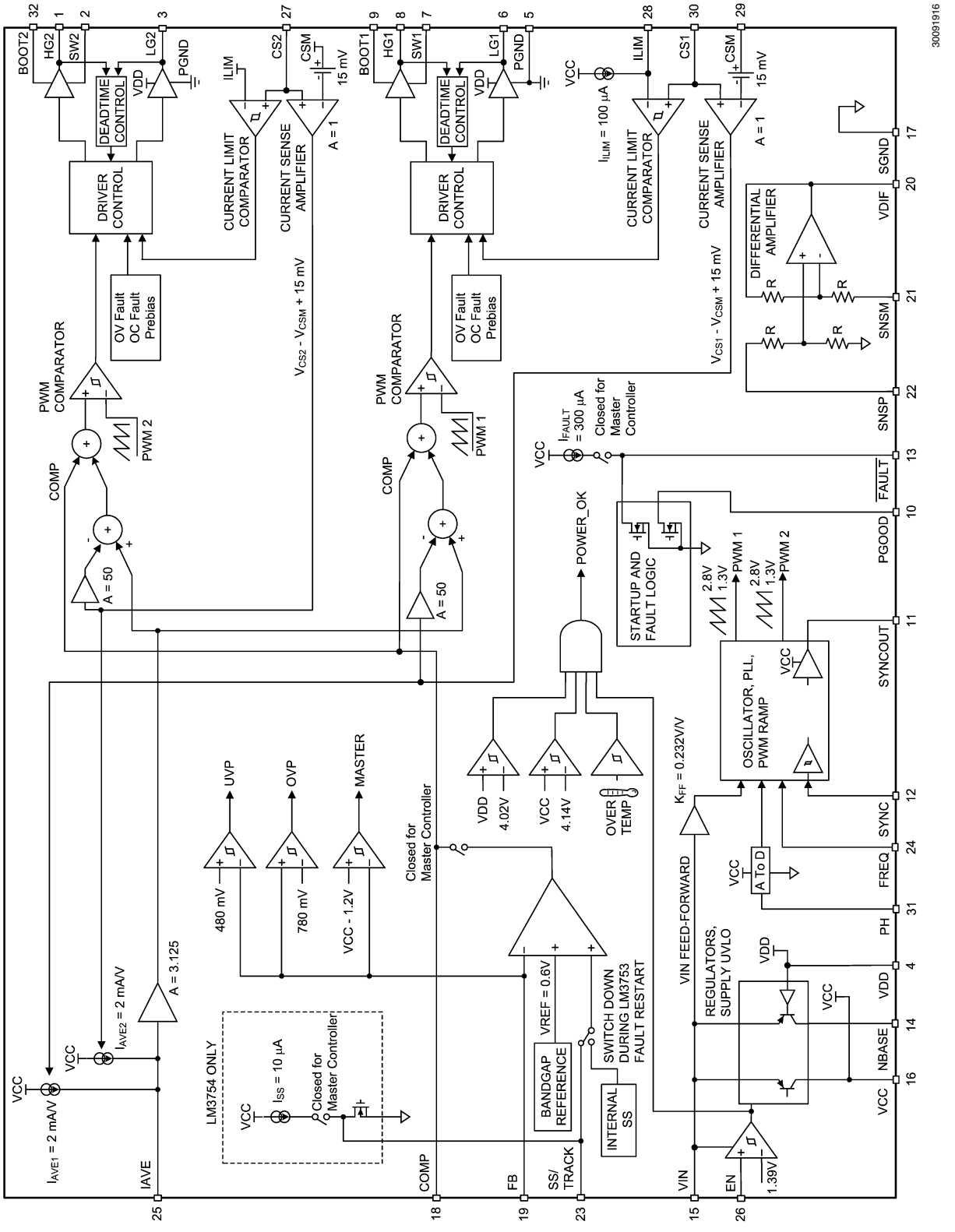
30091912

Over-Current Fault (Soft Short)



30091915

Block Diagram



Functional Description

GENERAL

The LM3753 and LM3754 are two-phase voltage-mode step-down (buck) switching regulator controllers. From one to six LM3753/54 controllers can be connected together to control from two to twelve phases (2, 3, 4, 5, 6, 8, 10, or 12 phases). Since external switching components can typically handle 25A per phase, a 12 phase system can supply a total of 300A.

Multiple controllers in a system communicate with each other and work together. They will startup and shut down together, each phase on each controller will share current equally, and all the phases will react in unison to fault conditions. In a multi-controller system, all controllers are the same part (all LM3753 or all LM3754). One controller functions as the Master and all the others act as Slaves. The Master and Slave are differentiated by how they are connected in the system. The Master controller senses the system output voltage and VIN (as well as SS or TRACK) and sets the target duty cycle for each phase on all of the controllers. The Master and Slave controllers monitor the current-sense information from each phase. Based on this current information, the controllers adjust the duty cycle on each phase up or down from the target level, in order to achieve optimal current sharing.

Each controller incorporates a phase locked loop (PLL) that communicates with the PLLs on the other controllers. By this means, the switching edges of the different phases are spread out equally within one switch period. For N phases operating at any switching frequency, the angle in degrees between one phase switching and the next is 360° / N. A SYNC pin is available that can be used to lock the Master switching frequency and phase to an external clock.

The LM3753 has a Tracking function. The output voltage will follow the TRACK pin, both up and down, whenever it is less than VREF. Synchronous switching is always enabled, except during fault recovery.

The LM3754 has a Soft-Start function. The Master controller sources 10 µA out of the SS pin so that the output voltage rise time is controlled by the size of the external SS capacitor. The LM3754 will not pull down a pre-biased load. The synchronous NFET switch is not turned on during the soft-start cycle until the SS ramp exceeds either the FB voltage or the internal reference voltage VREF. At this point a gradual transition to synchronous switching is initiated.

CONTROL ALGORITHM

The control architecture is primarily voltage-mode. An error amplifier amplifies the difference between the FB pin voltage and the internal reference voltage to generate a COMP signal. This signal is compared against a ramp that consists of a fixed value plus a term proportional to VIN which controls the duty cycle. In order to facilitate current sharing there is an inner current-sense loop. Information for the current through the inductor in each phase is sensed either with a sense resistor or with a DCR arrangement which uses the DC resistance of the inductor. This current-sense signal is connected to the CS pin (CS1 or CS2). The negative reference for current-sense is V_{OUT} which is common for both phases and connected to the controller's CSM pin. The controller amplifies the (CS1(2) – CSM) voltage difference for each phase, and compares it to the voltage on the IAVE pin, which tracks the average current of all phases. Any phase whose current is more than the average has its duty cycle decreased and vice versa. The IAVE signal is common to all controllers in a system. Each controller outputs a current onto the IAVE bus so that the total current on the bus is the sum of the current signals from all of the phases. An external resistor to ground translates this current signal to a voltage, which all of the controllers read back.

The LM3753/54 includes an uncommitted differential amplifier. On the Master controller this amplifier is used to remotely sense the converter's output voltage, typically at the load. On the Slave controllers this amplifier is used to buffer the Master controller's COMP signal and level shift it to the Slave controller's local ground.

POWER CONNECTIONS

The LM3753/54 has three supply pins, which are VIN, VCC, and VDD. It employs two ground pins, SGND and PGND. VDD and PGND are the power and ground for the gate driver stage that controls the HG and LG pins. The quiescent current drawn by VDD is very small – around 1 mA. To predict the VDD current requirement one can assume it is mostly switching current and use the standard formula:

$$I_{VDD} = (1 \text{ or } 2) \times f_{SW} \times Q_{TOTAL\_PHASE}$$

Q_{TOTAL_PHASE} is the sum of the high-side switch gate charge and the low-side gate charge. The (1 or 2) factor corresponds to one or two phases running. The low-side driver is powered directly from VDD. The high-side driver draws its power from VDD through the external bootstrap Schottky diode. The rest of the controller is powered by VCC and SGND.

The LM3753/54 has two on-board regulators, one to generate VCC and one to generate VDD. The VCC regulator is self-contained and only needs a 4.7 µF ceramic capacitor to SGND. The VDD regulator uses an external NPN pass device. This device should be sized to meet the VIN to VDD dropout requirements for the calculated I_{VDD}. The collector of this device goes to VIN, the base goes to NBASE and the emitter goes to VDD. VDD also needs a 4.7 µF bypass capacitor to PGND. The internal VIN to NBASE dropout is approximately 300 mV. The minimum VIN is calculated as:

$$VIN_{MIN} = VDD_{MIN} + V_{BE\_NPN} + 300 \text{ mV}$$

$$VDD_{MIN} = MAX(VDD_{UVLO}, V_{GATE\text{-}MIN})$$

VDD_{UVLO} is the controller's maximum VDD under-voltage lockout voltage, which is 4.06V. $V_{GATE\text{-}MIN}$ is the minimum required gate drive voltage for the power MOSFET switches. VIN_{MIN} is typically 5.5V to 6.0V. For VIN less than 5.5V, the regulators are omitted and the VCC and VDD pins are connected as shown in *Figure 3*.

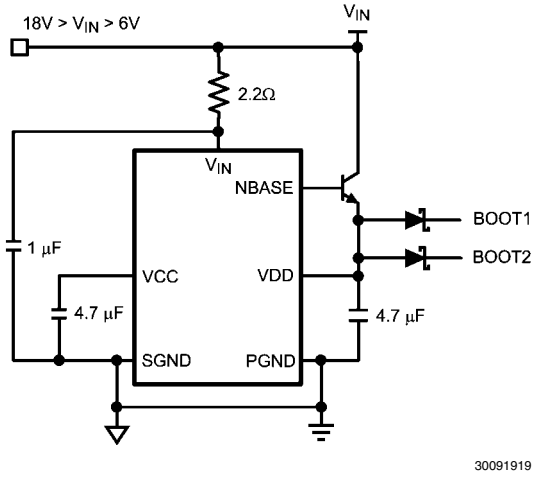


FIGURE 1. Power Connections Using the Internal Regulator

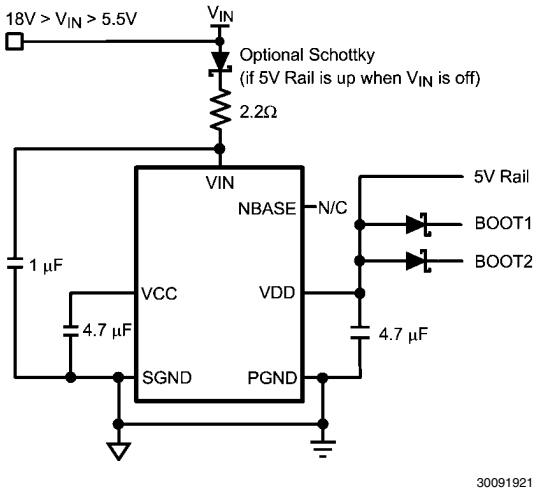


FIGURE 2. Power Connections Using a System 5V Rail

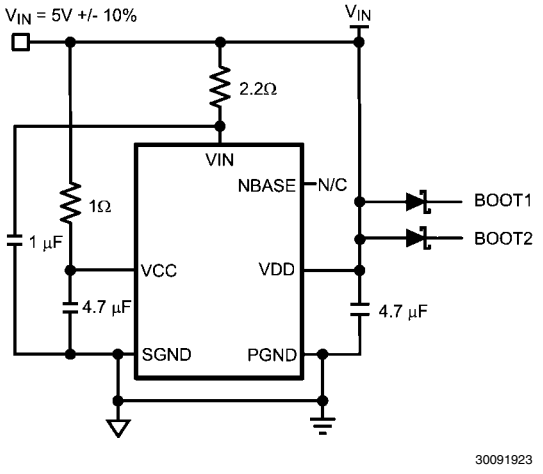


FIGURE 3. Power Connections for V_{IN} = 5V

UNDER-VOLTAGE LOCKOUTS and ENABLE

The LM3753/54 controller has internal under-voltage lockout (UVLO) detection on the VCC and VDD supplies. The under-voltage lockout on VIN is set using the EN pin threshold. Connect a voltage divider between VIN and SGND with the midpoint going to the EN pin. The division ratio and the EN pin threshold determine the VIN level that enables the controller. This divider should be used in all cases. If the system does not have a particular VIN under-voltage lockout requirement, the level is set to be below the minimum VIN level at the worst case combination of tolerances and operating conditions.

$$\frac{R_{UV2}}{R_{UV1}} = \frac{V_{IN\_UVLO}}{V_{EN}} - 1$$

To guarantee startup at the lowest input voltage, set the divider to the V_{EN-TH} rising max specification. For a higher accuracy VIN UVLO operation, the resistor divider minimum current should be 1 mA or higher. This will reduce the threshold error contribution of the EN pin bias current, which is guaranteed to be less than 1.7 µA over temperature. The enable pin can also be used as a digital on-off. To do this, the enable signal should be used to pull down the midpoint of the voltage divider using open-drain logic or a transistor. A customary implementation uses an external MOSFET.

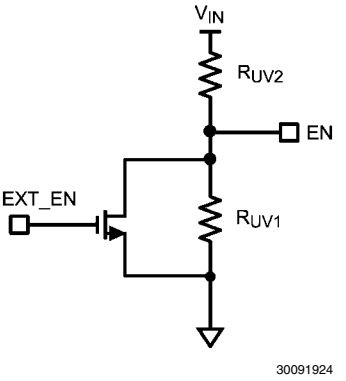


FIGURE 4. Input Voltage UVLO with External Enable

While the EN pin has a threshold hysteresis of 140 mV typical, a small noise-filtering capacitor may be added between the EN pin and SGND. This is particularly useful when the controller is turning on via the resistor divider by a slowly rising VIN rail.

STARTUP SEQUENCE

During the initial startup phase the LM3753 and LM3754 behave identically. When EN is below its threshold, the internal regulators are off and the controller is in a low power state. When EN crosses above its threshold the VCC regulator turns on. When VCC rises above its under-voltage lockout threshold the VDD regulator turns on. When VDD rises above its under-voltage lockout threshold the controller is ready to start.

If VDD or VCC is supplied externally and already sitting above its under-voltage lockout point, then the controller is ready for startup as soon as EN crosses above its threshold. Anytime VCC or VDD drops below its UV threshold, switching stops and the controller goes into a standby state. It will go through normal startup once the supplies recover.

When the controller is ready to start, it reads the voltage on the PH pin and determines how many phases are running in the system. By this means the phase delay from SYNC to SYNCOUT through the PLL is configured. Following this the oscillator and PLL turn on and pulses will be observed on SYNCOUT.

A 2 ms timer is initiated so that all of the PLLs in the system can synchronize up. As each controller times out, it stops pulling its $\overline{\text{FAULT}}$ pin low. At the end of this sequence, the $\overline{\text{FAULT}}$ bus rises and the controllers are ready to switch.

On both the LM3753 and LM3754, the error amplifier uses a different input stage when TRACK/SS is below VREF. During normal operation the error amplifier employs a low offset bipolar input stage. At startup, the input bias current of this stage is large enough in relation to the soft-start current to affect the soft-start timing. A MOS input stage is used during the soft-start or track phase which has a lower input bias current but a higher input offset voltage. A 40 mV offset is introduced when TRACK/SS is less than 70 mV. This offset forces the error amplifier output to be low during startup. The offset transitions progressively to zero as TRACK/SS moves from 0 to 70 mV.

TRACKING (LM3753)

The LM3753 implements a tracking function. The error amplifier amplifies the minimum of VREF or TRACK at the FB

pin. By means of the closed loop regulation through the switching stage, FB will be regulated to TRACK. When TRACK is below VREF, the LM3753 will control FB both up and down to follow TRACK. When TRACK is above VREF, FB will be regulated to VREF. A pre-biased output will be pulled down by the LM3753. Full synchronous switching is always employed on the LM3753, except for restart after a fault condition.

When the LM3753 is ready to switch, normally TRACK will be grounded and COMP will be low. LG will get pulled to VDD to turn on the synchronous switch. As TRACK slews above FB, COMP will slew up and LG will go high for 300 ns to charge the HG bootstrap capacitor. Following this HG begins switching. COMP will set the duty cycle with normal PWM control of HG and LG. The loop acts to have FB follow TRACK. If V_{OUT} is too high, it will get pulled down. An internal timer sets a 2 ms delay from the time of the first HG pulse, which occurs as soon as COMP slews above the PWM ramp bottom.

When the 2 ms times out, PGOOD goes high if FB is above the output under-voltage threshold on the Master, TRACK is above VREF, no fault conditions are present, and SYNC is toggling on the Slaves.

SOFT-START (LM3754)

The LM3754 implements a soft-start function, and operates so as to prevent discharge of a pre-biased output. The error amplifier amplifies the minimum of VREF or SS at the FB pin. By means of the closed loop regulation through the switching stage, FB will be regulated to SS. The Master controller sources 10 µA onto the SS pin, while the Slaves do not source any current. This sets the total soft-start current in a multi-controller system to 10 µA.

The SS pin is automatically pulled down to SGND prior to the onset of switching and during a restart from a fault condition. When SS is initially released, COMP is low and no switching occurs. Both LG and HG are held low while SS is below FB, which guarantees that a pre-biased load will not be pulled down. When SS crosses above either FB or VREF, COMP will slew up and switching will start. The first switching pulse is a 300 ns LG pulse to charge the external HG bootstrap capacitor. After this the LG pulse width is reduced to zero. This insures that V_{OUT} does not get pulled down while COMP slews up and the system loop is settling. Pulses on HG cause the high-side FET to turn-on so that FB tracks the SS pin as it slews up. During the switch cycle off-time the inductor current can only flow through the body diode of the synchronous switch. During each successive cycle the LG pulse width gradually increases. Over the course of 0.3 ms to 2.0 ms, depending on the amount of pre-bias, LG pulses get longer until full synchronous switching occurs. The internal timer waits 2 ms, regardless of duty cycle, for this transition in LG pulse width to complete.

Following this PGOOD goes high if FB is above the output under-voltage threshold on the Master, SS is above VREF, no fault conditions are present, and SYNC is toggling on the Slaves.

PHASE NUMBER SELECTION

The voltage at the PH pin determines the phase shift between the two phases of each controller and also the phase shift between the SYNC and SYNCOUT pulses in a Master-Slave configuration. This voltage is read at startup and the resulting phase configuration saved. The PH pin should be connected to the center of a resistor divider between VCC and SGND to select and program the required number of phases and the corresponding phase delays per *Table 1*. Each controller requires the same resistor divider at the PH pin.

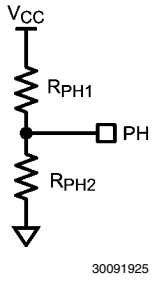


FIGURE 5. Phase Selection

TABLE 1. Phase Divider Resistors

Number Of Phases	Divide Ratio Target	R_{PH1} (± 1%)	R_{PH2} (± 1%)
2 & 4 Phases	0.000	Omit	0
3 Phases	0.214	7870Ω	2150Ω
5 Phases	0.357	6490Ω	3570Ω
6 Phases	0.5	4990Ω	4990Ω
8 Phases	0.643	3570Ω	6490Ω
10 Phases	0.786	2150Ω	7870Ω
12 Phases	1	0	Omit

OVER-CURRENT and OVER-VOLTAGE FAULTS

If any controller experiences a fault condition, it will pull the $\overline{\text{FAULT}}$ bus low and all of the controllers will stop switching. From the time when EN is low to the point where $\overline{\text{FAULT}}$ rises, both HG and LG are low so that the SW node of each phase is floating. The $\overline{\text{FAULT}}$ input may be pulled low externally through an open drain MOSFET to disable the system.

The LM3753/54 employs cycle-by-cycle current limiting. This occurs on each phase for both Master and Slave controllers. The current (that is the CS1(2) – CSM voltage) is continuously compared to the over-current set point (ILIM – CSM). Any time that the current-sense signal exceeds current limit, the cycle is ended.

In order to determine that a current fault has occurred, each controller counts the number of over-current pulses. When the sum of the counts for phase 1 and phase 2 reaches 446 an over-current fault is declared. The counter is reset after 16 consecutive switching cycles with no over-current on either phase.

There is a second method for achieving an over-current fault, which is meant to react to heavy shorts on V_{OUT}. The Master controller will determine that an over-current fault has occurred after 7 over-current cycles if the voltage at the FB pin is less than 50% of its target value. This feature is disabled during startup. Since the Slave controllers do not see the FB voltage, they cannot detect this type of fault.

Any controller which sees an over-current fault will respond by pulling the $\overline{\text{FAULT}}$ bus low. All of the controllers will react and stop switching. Both HG and LG on each phase will be pulled low. The inductor current in each phase will decay through the body diodes of the low-side switches. The controller which recognized the over-current fault will hold $\overline{\text{FAULT}}$ low for 6 ms, which determines the hiccup time. This allows the energy stored in the inductors to dissipate. After this, $\overline{\text{FAULT}}$ is released and all of the controllers will restart together.

The restart after fault process for the LM3754 is the same as the initial startup process. SS is pulled low and the system will go through a full soft-start cycle. Switching will resume when SS crosses above FB.

The restart after fault for the LM3753 is different from the initial startup. When an over-current fault occurs, TRACK is usually above VREF. In order to avoid V_{OUT} slewing up precipitously, a fixed time internal soft-start is connected to the error amplifier to control the rise of V_{OUT}. The low-side switch is not turned on until the internal SS exceeds FB or VREF, which allows V_{OUT} to remain high. The error amp will use as a reference the minimum of VREF, TRACK or the internal SS. Once switching ensues a gradual transition to fully synchronous operation occurs.

Over-voltage faults are only recognized by the Master controller. About 5 µs after FB crosses above the OVP threshold, which is 30% above VREF, the Master controller declares an over-voltage fault. It pulls the $\overline{FAULT}$ bus low and all of the controllers stop switching, with HG being low and LG being high. The low-side MOSFETs pull V_{OUT} down to remove the over-voltage condition. As soon as FB crosses below the under-voltage detect point, which is 20% below VREF, the LG outputs go low to turn off the low-side MOSFETs. This prevents the negative inductor current from ramping too high. The Master controller then waits 2 ms to allow any negative inductor current to transition into the high-side MOSFETs body diodes.

The restart from an over-voltage fault is the same as the restart from an over-current fault. In addition there is an over-voltage fault counter. On the seventh over-voltage fault, the system does not restart. It waits for power or EN to be cycled. This counter is reset to zero when power goes low or EN crosses below its threshold.

PGOOD and PGOOD DELAY

PGOOD is an open-drain logic output. It is asserted HIGH when the output voltage level is within the PGOOD window, which is typically –20% to +30%. In order to operate, the PGOOD output requires a pull-up resistor to an appropriate supply voltage. This voltage is typically the supply for an external monitoring circuit. The resistor is selected so that it limits the PGOOD sink current to less than 4 mA.

PGOOD is delayed from either power-up or VIN under-voltage lockout, and has three primary factors:

1) A synchronization delay, set to 2 ms after the slowest controller in the system recognizes a valid level on EN, VCC and VDD. This delay is timed out internally and allows for the phase lock loops to synchronize.

2) Soft-Start/Track up, in non-fault conditions.

3) Transition period from diode emulation mode to fully synchronous operation, set to 2 ms.

CURRENT SENSE and CURRENT LIMIT

The LM3753/54 senses current to enforce equal current sharing and to protect against over-current faults. There are two system options for sensing current; a current-sense resistor, or a DCR configuration which uses the DC resistance of the inductor. The current-sense resistor is more accurate but less efficient than the DCR configuration.

The input range of the differential current-sense signal (CS1(2) – CSM) is from –15 mV to +40 mV. The common mode range is the same as the controller's output range which is 0V to 3.6V. Two considerations determine the value of the current-sense resistor. If the resistor is too large there is an efficiency loss. If it is too small the current-sense signal to the controller will be too low. Choose a resistor that gives a full load current-sense signal of at least 25 mV. This is typically a resistor in the 1 mΩ to 2 mΩ range. The current-sense resistor is inserted between the inductor and the load. The load side of the resistor which is V_{OUT}, is connected to CSM, the negative current-sense input. This is the negative current-sense reference for both phases. The positive side of the current-sense resistor goes to CS1(2).

For the DCR configuration a series resistor-capacitor combination is substituted for the current-sense resistor. The resistor connects to the switch node (SW) and the capacitor connects to V_{OUT}. CSM is connected to V_{OUT} as with the sense resistor. CS1(2) is connected to the center point of the resistor and capacitor, so that the current-sense signal is developed across the capacitor. The voltage across the capacitor is a low pass filtered version of the voltage across the resistor-capacitor combination, in the same way the current through the inductor is a low pass filtered version of the voltage applied across the inductor and its intrinsic series resistance. Choose the DCR time constant (R_{DCR} x C_{DCR}) to be 1.0 to 1.5 times the inductor time constant (L / R_L). R_{DCR} is selected so that the CS pin input bias current times R_{DCR} does not cause a significant change in the CS voltage. The inductor time constant and the DCR time constant will skew over temperature since the components have different temperature coefficients. Critical applications may employ a correction circuit based on a positive temperature coefficient thermistor (PTC).

The over-current limit is set by placing a resistor between ILIM and CSM. The value of the resistor times the ILIM current of 94 µA sets the over-current limit.

CURRENT SHARING and CURRENT AVERAGING

The current sharing works by adjusting the duty cycle of each phase up or down to make the phase current equal to the average current. The maximum duty cycle shift is ±20%.

To determine the average current, each phase sources a current onto the IAVE bus proportional to its load current as measured by the current sense amplifier connected to the CS1(2) and CSM pins. The IAVE pins of all controllers are connected together and a resistance of 8 kΩ per phase (parallel) to SGND provides the proper voltage level for the IAVE bus. Each phase compares its current sense output to the IAVE bus and sums the resultant voltage into the common COMP signal to adjust the duty cycle for optimum current sharing.

IAVE forms the current sharing bus for the entire power converter. The IAVE pins of all controllers must be connected together. Filter capacitors with a time constant of R_{AV} x C_{AV} = 1 / f_{SW} are connected between IAVE and SGND of each controller. The parallel combination of the filter capacitors times the summing resistors (one set per controller) forms the time constant of the current sharing bus.

ERROR AMPLIFIER and LOOP COMPENSATION

The LM3753/54 uses a voltage mode PWM control method. This requires a TYPE III or 3 pole, 2 zero compensation for optimum bandwidth and stability. The error amplifier is a voltage type operational amplifier with 70 dB open loop gain and unity gain bandwidth of 15 MHz. This allows for sufficient phase boost at high control loop frequencies without degrading the error amplifier performance.

The error amplifier output COMP connections are different for Master and Slave controllers. For the Master, a compensation network is placed between the COMP pin and the FB pin. The COMP pin of the Master is connected to the SNSP pin of each Slave. The SNSM pin of each Slave is connected to the bot-

tom of the Master feedback divider at SGND. The COMP pin of each Slave is connected to its corresponding VDIF pin. This provides sufficient buffering of the master COMP signal for the internal summing of the current averaging circuit.

OSCILLATOR and SYNCHRONIZATION

A resistor and decoupling capacitor are connected between FREQ and SGND to program the switching frequency between 200 kHz to 1 MHz. These components must be supplied on each controller, even if the system is synchronized to an external clock.

The switching frequency and synchronization are controlled by the Master. The Master can switch in a free-running mode or be synchronized to an external clock. To synchronize the Master apply the external clock to the SYNC pin of the Master, otherwise ground this pin. The amplitude of the signal on the SYNC pin must be limited to be between 0V and VCC.

The value of the frequency setting resistor is determined as:

$$R_{FRQ} = \frac{\frac{1}{f_{SW}} - 142\ ns}{40.56\ pF}$$

A 1000 pF ceramic capacitor is used to provide sufficient decoupling. If the Master is synchronized set the resistor according the nominal applied frequency. If the signal on the SYNC pin is below 150 kHz the signal will be ignored and the device will revert to free-running mode. The SYNCOUT signal from the Master is applied to the first Slave's SYNC pin. The SYNCOUT pin of the first Slave is connected to the SYNC pin of the second Slave, and so on, in a daisy chain configuration. SYNCOUT of the last Slave (or the Master in a single controller system) is left unconnected.

The configuration of the system, namely the number of controllers and phases is programmed by the voltage on the PH pin. For each controller connect the midpoint of a resistor divider between VCC and SGND to the PH pin. The division ratios are given in the *Electrical Characteristics* table and nominal resistor values in *Table 1*. This sets the phase shift between SYNC and the SYNCOUT pin. Where an even number of phases (N) are employed, the phase delay from SYNC to SYNCOUT is 360°/N. The phase difference between the two phases on the same controller is 180°. For systems with an odd number of the phases, the HG2 and LG2 gate drivers on the last Slave are unconnected and the phase arrangement is set according to *Table 1*

DUTY CYCLE LIMITATION

The minimum controllable on-time is typically 50 ns. This limits the maximum V_{IN} , V_{OUT} and f_{SW} combination.

$$f_{SW} < (V_{OUT} / V_{IN}) \times 20\ MHz$$

The maximum guaranteed duty cycle is 81%. This limits the minimum V_{IN} to V_{OUT} ratio.

$$(V_{OUT} / V_{IN}) \times 1.25 < 0.81$$

The 1.25 term allows margin for efficiency and transient response.

THERMAL SHUTDOWN

The internal thermal shutdown circuit causes the PWM control circuitry to be reset and the NFET drivers to turn off all external power MOSFETs. The controller remains enabled and all bias circuitry remains on. After the die temperature falls below the lower hysteresis point, the controller will restart.

NFET SYNCHRONOUS DRIVERS

The LM3753/54 has two sets of gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Power to the high-side driver is supplied through the BOOT pin. For the high-side gate HG to turn on the high-side FET, the BOOT voltage must be at least one V_{GS} greater than VIN. This voltage is supplied from a local charge pump which consists of a Schottky diode and bootstrap capacitor, shown in *Figure 6*. For the Schottky, a rating of at least 250 mA and 30V is recommended. A dual package may be used to supply both BOOT1 and BOOT2 for each controller.

Both the bootstrap and the low-side FET driver are fed from VDD. The drive voltage for the top FET driver is about VDD – 0.5V at light load condition and about VDD at normal to full load condition.

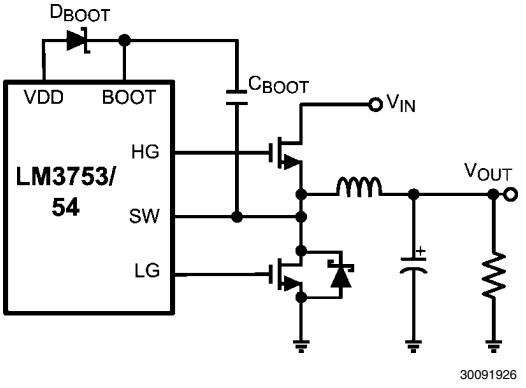


FIGURE 6. Bootstrap Circuit

REMOTE SENSE DIFFERENTIAL AMPLIFIER

The differential amplifier connected internally to the SNSP, SNSM and VDIF pins is a single stage unity gain Instrumentation amplifier. The differential gain is tightly controlled to within 0.4%.

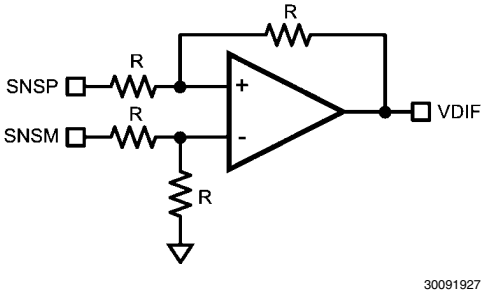


FIGURE 7. Differential Amplifier

On the master controller, the differential amplifier is used to provide Kelvin sensing of the output voltage at the load. This provides the most accurate sampling for load regulation.

On the slave controllers, the differential amplifier is used to sense the COMP signal of the master controller with respect to its signal ground and drive the COMP pin of that slave controller relative to its local signal ground. This allows the master controller to accurately provide the target duty cycle of the slave controllers.

The differential amplifier has a low output impedance to allow it to drive the COMP pins of the Slave controllers. This is necessary because the current sense signal is internally added

to COMP to provide the duty cycle adjustment for phase-to-phase current sharing.

Application Information

NUMBER of PHASES

The number of phases can be calculated by dividing the maximum output load current by 25A. Therefore a 120A load requirement will need at least 5 phases, or 3 controllers. It may be better to use 6 phases which will still require 3 controllers, but will reduce the maximum current/phase to 20A. Increasing the number of phases will also reduce the output voltage ripple and the input capacitor requirements. Note that the 25A/phase is dictated by external components and not by the LM3753/54. After the number of phases has been chosen, the PH pin on each controller should be programmed as discussed in the *Functional Description* under *PHASE NUMBER SELECTION*. The same number of phases must be selected for each controller.

POWERING OPTIONS

The power connections will be determined by the VIN range and the availability of an external 5V rail. This is discussed in detail in the *Functional Description* under *POWER CONNECTIONS*. For 12V input systems, the use of an external 5V rail to power the VDD bus can improve overall system efficiency.

MULTI-CONTROLLER SYSTEMS

For systems with more than 2 phases, there will be one controller configured as the Master and from 1 to 5 controllers configured as Slave.

The Master controller uses the differential amplifier to sense the output voltage at the load point. It also provides the common COMP signal used by all controllers, provides the loop compensation and synchronizes the system clock to an external clock if one is provided.

The SYNCOUT of the Master is connected to the SYNC input of the first Slave controller.

The Slave controllers are configured by tying the FB input to the VCC pin of that controller. Each Slave uses the differential amplifier to sense the COMP signal of the Master controller and drive its own COMP input. The SYNCOUT of each Slave controller is connected to the SYNC input of the next Slave controller.

All controllers have the same parallel RC components connected from the FREQ pin to local ground corresponding to the desired system clock even if synchronizing to an external clock.

Common connections for all controllers:

1) IAVE (each controller will have a parallel RC filter to local ground).

2) $\overline{\text{FAULT}}$

3) EN

4) SS (LM3754), TRACK (LM3753)

5) PGOOD

TRACKING (LM3753)

The LM3753 will track the output of an external power supply by connecting a resistor divider to the TRACK pin as shown in *Figure 8*. This allows the output voltage slew rate to be controlled for loads that require precise sequencing.

A value of 10 kΩ 1% is recommended for R_{T1} as a good compromise between high precision and low quiescent current through the divider. Note that the TRACK pin must finish at least 100 mV higher than the 0.6V reference to achieve the full accuracy of the LM3753 regulation. To meet this requirement the tracking voltage is offset by 150 mV. The output voltage will reach its final value at 80% of the external supply voltage. The tracking resistors are determined by:

$$0.75 = V_{EXT} \times \frac{R_{T1}}{R_{T1} + R_{T2}}$$

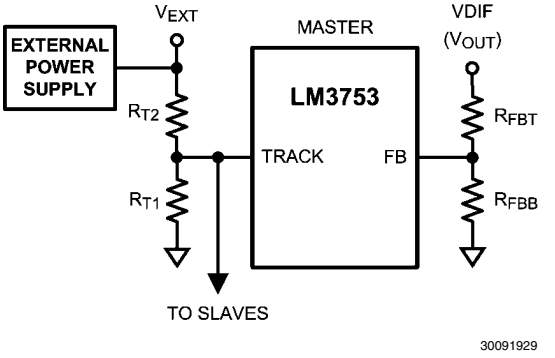


FIGURE 8. Tracking an External Supply

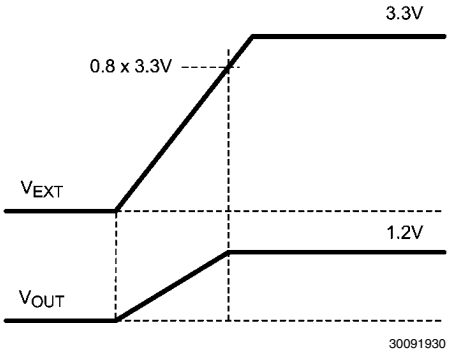


FIGURE 9. Tracking an External Supply

For equal slew rates, the relationship for the tracking divider is set by:

$$V_{OUT} = V_{EXT} \times \frac{R_{T1}}{R_{T1} + R_{T2}}$$

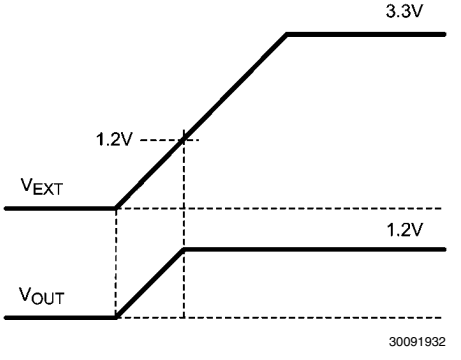


FIGURE 10. Tracking an External Supply with Equal Slew Rates

In order to track properly, the external power supply voltage must be higher than the LM3753 output voltage.

SOFT-START (LM3754)

To avoid current limit during startup, the soft-start time t_{SS} should be substantially longer than the time required to charge C_{OUT} to V_{OUT} at the maximum output current. To meet this requirement:

$$t_{SS} > \frac{V_{OUT} \times C_{OUT}}{I_{LIMIT} - I_{OUT}}$$

Choose a soft-start capacitor according to the formula:

$$C_{SS} = t_{SS} \times \frac{10\ \mu A}{0.6V}$$

Where C_{SS} is the soft-start capacitor and t_{SS} is the soft-start time.

External Components Selection

The following is a design example selecting components for the Typical Application Schematic of *Figure 20*. The circuit is designed for two controller 4-phase operation with 1.2V out at 100A from an input voltage of 6V to 18V. The expected load is a microprocessor or ASIC with fast load transients, and the type of MOSFETs used are in SO-8 or its equivalent packages such as PowerPAK ®, PQFN and LFPAK (LFPAK-i).

SWITCHING FREQUENCY

The selection of switching frequency is based on the tradeoff between size, cost, and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors will be needed. A higher switching frequency generally results in a smaller but less efficient solution. For this application a frequency of 300 kHz was selected as a good compromise between the size of the inductor and MOSFETs, transient response and efficiency. Following the equation given for R_{FRQ} in the *Functional Description* under *OSCILLATOR and SYNCHRONIZATION*, for 300 kHz operation a 78.7 kΩ 1% resistor is used for R_{FRQ}. A 1000 pF capacitor is used for C_{FRQ}.

OUTPUT INDUCTORS

The first criterion for selecting an output inductor is the inductance itself. In most buck converters, this value is based on the desired peak-to-peak ripple current, ΔI_L that flows in the inductor along with the load current. As with switching frequency, the selection of the inductor is a tradeoff between size and cost. Higher inductance means lower ripple current and hence lower output voltage ripple. Lower inductance results in smaller, less expensive devices. An inductance that gives a ripple current of 1/5 to 2/5 of the maximum output current is a good starting point. (ΔI_L = (1/5 to 2/5) x I_{OUT}). Minimum inductance is calculated from this value, using the maximum input voltage as:

$$L_{MIN} = \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \times \Delta I_L} \times D$$

By calculating in terms of amperes, volts, and megahertz, the inductance value will come out in micro henries. The inductor ripple current is found from the minimum inductance equation:

$$\Delta I_L = \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \times L_{ACTUAL}} \times D$$

The second criterion is inductor saturation current rating. The LM3753/54 has an accurately programmed peak current limit. During an output short circuit, the inductor should be chosen so as not to exceed its saturation rating at elevated temperature. For the design example, a standard value of 440 nH is chosen to fall within the ΔI_L = (1/5 to 2/5) x I_{OUT} range.

The dc loss in the inductor is determined by its series resistance R_L. The dc power dissipation is found from:

$$P_{DC} = I_{OUT}^2 \times R_L$$

The ac loss can be estimated from the inductor manufacturer's data, if available. The ac loss is set by the peak-to-peak ripple current ΔI_L and the switching frequency f_{SW}.

OUTPUT CAPACITORS

The output capacitors filter the inductor ripple current and provide a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM3753/54 that provides excellent performance. The best performance is typically obtained using aluminum electrolytic, tantalum, polymer, solid aluminum, organic or niobium type chemistries in parallel with ceramic capacitors. The ceramic capacitors provide extremely low impedance to reduce the output ripple voltage and noise spikes, while the aluminum or other capacitors provide a larger bulk capacitance for transient loading.

When selecting the value for the output capacitors the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple for a single phase can be approximated as:

$$\Delta V_O = \Delta I_L \times \sqrt{R_C^2 + \left(\frac{1}{8 \times f_{SW} \times C_O}\right)^2}$$

With all values normalized to a single phase, ΔV_O (V) is the peak to peak output voltage ripple, ΔI_L (A) is the peak to peak inductor ripple current, R_C (Ω) is the equivalent series resistance or ESR of the output capacitors, f_{SW} (Hz) is the switching frequency, and C_O (F) is the output capacitance. The amount of output ripple that can be tolerated is application specific. A general recommendation is to keep the output ripple less than 1% of the rated output voltage. *Figure 11* shows the output voltage ripple for multi-phase operation.

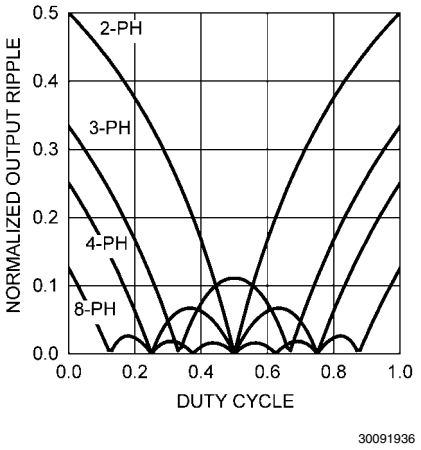


FIGURE 11. Multi-Phase Output Voltage Ripple

Based on the normalized single phase ripple, the worst case multi-phase output voltage ripple can be approximated as:

$$\Delta V_O(N) = \Delta V_O / N$$

Where N is the number of phases.

The output capacitor selection will also affect the output voltage droop and overshoot during a load transient. The peak transient of the output voltage during a load current step is dependent on many factors. Given sufficient control loop bandwidth an approximation of the transient voltage can be obtained from:

$$V_P = \frac{L \times \Delta I_O^2}{2 \times C_O \times V_L} + \frac{R_C^2 \times C_O \times V_L}{2 \times L}$$

With all values normalized to a single phase, V_P (V) is the output voltage transient and ΔI_O (A) is the load current step change. C_O (F) is the output capacitance, L (H) is the value of the inductor and R_C (Ω) is the series resistance of the output capacitor. V_L (V) is the minimum inductor voltage, which is duty cycle dependent.

For D < 0.5, $V_L = V_{OUT}$

For D > 0.5, $V_L = V_{IN} - V_{OUT}$

This shows that as the input voltage approaches V_{OUT}, the transient droop will get worse. The recovery overshoot remains fairly constant.

The loss associated with the output capacitor series resistance can be estimated as:

$$P_{CO} = R_C \times \frac{\Delta I_L^2}{\sqrt{12}}$$

Output Capacitor Design Procedure

For the design example V_{IN} = 12V, V_{OUT} = 1.2V, D = V_{OUT} / V_{IN} = 0.1, L = 440 nH, ΔI_L = 9A, ΔI_O = 20A and V_P = 0.12V.

To meet the transient voltage specification, the maximum R_C is:

$$R_C \le \frac{V_P}{\Delta I_O}$$

For the design example, the maximum R_C is 6 mΩ. Choose R_C = 3 mΩ as the design limit.

From the equation for V_P, the minimum value of C_O is:

$$C_O \ge \frac{L \times \Delta I_O^2}{V_P \times V_L} \times \frac{1}{1 + \sqrt{1 - \left(\frac{R_C \times \Delta I_O}{V_P}\right)^2}}$$

For D < 0.5, $V_L = V_{OUT}$

For D > 0.5, $V_L = V_{IN} - V_{OUT}$

With $R_C = V_P / \Delta I_O$ this reduces to:

$$C_O \ge \frac{L \times \Delta I_O^2}{V_P \times V_L}$$

With R_C = 0 this reduces to:

$$C_O \ge \frac{L \times \Delta I_O^2}{2 \times V_P \times V_L}$$

Since D < 0.5, $V_L = V_{OUT}$. With R_C = 3 mΩ, the minimum value for C_O is 476 µF.

The minimum control loop bandwidth f_C is given by:

$$f_C \ge \frac{\Delta I_O}{8 \times C_O \times V_P}$$

For the design example, the minimum value for f_C is 44 kHz. Two 220 µF, 5 mΩ polymer capacitors in parallel with two 22 µF, 3 mΩ ceramics per phase will meet the target output voltage ripple and transient specification.

INPUT CAPACITORS

The input capacitors for a buck regulator are used to smooth the large current pulses drawn by the inductor and load when the high-side MOSFET is on. Due to this large ac stress, input capacitors are usually selected on the basis of their ac rms current rating rather than bulk capacitance. Low ESR is beneficial because it reduces the power dissipation in the capacitors. Although any of the capacitor types mentioned in the *OUTPUT CAPACITORS* section can be used, ceramic capacitors are common because of their low series resistance. In general the input to a buck converter does not require as much bulk capacitance as the output.

The input capacitors should be selected for rms current rating and minimum ripple voltage. The equation for the rms current and power loss of the input capacitor in a single phase can be estimated as:

$$I_{CIN(RMS)} \approx I_O \times \sqrt{D \times (1 - D)}$$

$$P_{CIN} \approx I_O^2 \times D \times (1 - D) \times R_{CIN}$$

Where I_O (A) is the output load current and R_{CIN} (Ω) is the series resistance of the input capacitor. Since the maximum values occur at D = 0.5, a good estimate of the input capacitor rms current rating in a single phase is one-half of the maximum output current.

Neglecting the series inductance of the input capacitance, the input voltage ripple for a single phase can be estimated as:

$$\Delta V_{IN} = \frac{I_O \times D \times (1 - D)}{C_{IN} \times f_{SW}} + \left(I_O + \frac{\Delta I_L}{2}\right) \times R_{CIN}$$

By defining the maximum input voltage ripple, the minimum requirement for the input capacitance can be calculated as:

$$C_{IN} \geq \frac{I_O \times D \times (1 - D)}{\left(\Delta V_{IN} - \left(I_O + \frac{\Delta I_L}{2}\right) \times R_{CIN}\right) \times f_{SW}}$$

For multi-phase operation, the general equation for the input capacitor rms current is approximated as:

$$I_{CIN(RMS)} \approx I_O \times \sqrt{D \times \left(\frac{1}{N} - D\right)}$$

This is valid for D < 1 / N and repeats for a total of N times. I_O represents the total output current and N is the number of phases. *Figure 12* shows the input capacitor rms current as a function of the output current, duty cycle and number of phases.

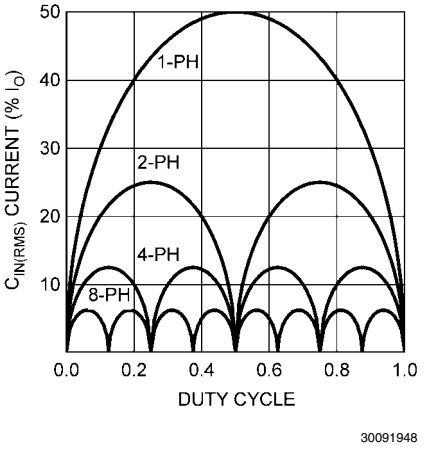


FIGURE 12. Input Capacitor RMS Current as a Function of Output Current

For multi-phase operation the maximum rms current can be approximated as:

$$I_{CIN(RMS)MAX} \approx 0.5 \times I_O / N$$

In most applications for point-of-load power supplies, the input voltage is the output of another switching converter. This output often has a lot of bulk capacitance, which may provide adequate damping.

When the converter is connected to a remote input power source through a wiring harness, a resonant circuit is formed by the line impedance and the input capacitors. If step input voltage transients are expected near the maximum rating of the LM3753/54, a careful evaluation of the ringing and possible overshoot at the device VIN pin should be completed. To minimize overshoot make $C_{IN} > 10 \times L_{IN}$. The characteristic source impedance and resonant frequency are:

$$Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \qquad f_S = \frac{1}{2 \times \pi \times \sqrt{L_{IN} \times C_{IN}}}$$

The converter exhibits a negative input impedance which is lowest at the minimum input voltage:

$$Z_{IN} = -\frac{V_{IN}^2}{P_{OUT}}$$

The damping factor for the input filter is given by:

$$\delta = \frac{1}{2} \times \left(\frac{R_{LIN} + R_{CIN}}{Z_S} + \frac{Z_S}{Z_{IN}}\right)$$

Where R_{LIN} is the input wiring resistance and R_{CIN} is the series resistance of the input capacitors. The term Z_S / Z_{IN} will always be negative due to Z_{IN}.

When δ = 1, the input filter is critically damped. This may be difficult to achieve with practical component values. With δ < 0.2, the input filter will exhibit significant ringing. If δ is zero or negative, there is not enough resistance in the circuit and the input filter will sustain an oscillation.

When operating near the minimum input voltage, an aluminum electrolytic capacitor across C_{IN} may be needed to damp the input for a typical bench test setup. Any parallel capacitor should be evaluated for its rms current rating. The current will split between the ceramic and aluminum capacitors based on the relative impedance at the switching frequency. Using a square wave approximation, the rms current in each capacitor is found from:

$$C1 = C_{IN1} \quad R1 = R_{CIN1} \quad C2 = C_{IN2} \quad R2 = R_{CIN2}$$

$$X_1 \approx \frac{1}{2.2 \times \pi \times f_{SW} \times C1}$$

$$X_2 \approx \frac{1}{2.2 \times \pi \times f_{SW} \times C2}$$

$$I_{CIN1(RMS)} = \frac{I_{CIN(RMS)} \times \sqrt{R2^2 + X2^2}}{\sqrt{(R1 + R2)^2 + (X1 + X2)^2}}$$

$$I_{CIN2(RMS)} = \frac{I_{CIN(RMS)} \times \sqrt{R1^2 + X1^2}}{\sqrt{(R1 + R2)^2 + (X1 + X2)^2}}$$

Input Capacitor Design Procedure

Ceramic capacitors are sized to support the required rms current. An aluminum electrolytic capacitor is used for damping. Find the minimum value for the ceramic capacitors from:

$$C_{IN} \geq \frac{I_O}{\Delta V_{IN} \times 4 \times N \times f_{SW}}$$

Allowing ΔV_{IN} = 0.6V for the design example, the minimum value is C_{IN} = 34.7 µF. Find the rms current rating from:

$$I_{CIN(RMS)MAX} \approx 0.5 \times I_O / N$$

Using the same criteria, the result is 12.5A rms. Manufacturer data for 4.7 µF, 25V, X7R capacitors in a 1210 package allows for 4A rms with a 20°C temperature rise. For the design example, using two ceramic capacitors for each phase will meet both the input voltage ripple and rms current target. Since the series resistance is so low at about 4 mΩ per capacitor, a parallel aluminum electrolytic is used for damping. A good

general rule is to make the damping capacitor at least five times the value of the ceramic. By sizing the aluminum such that it is primarily resistive at the switching frequency, the design is greatly simplified since the ceramic capacitors are primarily reactive. In this case the approximation for the rms current in the damping capacitor is:

$$I_{CIN2(RMS)} \approx \frac{I_{CIN(RMS)}}{2.2 \times \pi \times N \times f_{SW} \times R_{CIN2} \times C_{IN1}}$$

Where C_{IN2} is the damping capacitance, R_{CIN2} is its series resistance and C_{IN1} is the ceramic capacitance. A 470 µF, 25V, 0.06Ω, 1.19A rms aluminum electrolytic capacitor in a 10 mm x 10.2 mm package is chosen for the damping capacitor. Calculated rms current for the aluminum electrolytic is 0.67A.

MOSFETS

Selection of the power MOSFETs is governed by a tradeoff between cost, size and efficiency.

Losses in the high-side FET can be broken down into conduction loss, gate charge loss and switching loss. Conduction or I^2R loss is approximately:

$$P_{COND\_HI} = D \times (I_{OUT}^2 \times R_{DS(on)\_HI} \times 1.3)$$
(High-side FET)

$$P_{COND\_LO} = (1 - D) \times (I_{OUT}^2 \times R_{DS(on)\_LO} \times 1.3)$$
(Low-side FET)

In the above equations the factor 1.3 accounts for the increase in MOSFET $R_{DS(on)}$ due to self heating. Alternatively, the 1.3 can be ignored and the $R_{DS(on)}$ of the MOSFET estimated using the $R_{DS(on)}$ vs. Temperature curves in the MOSFET datasheets.

The gate charge loss results from the current driving the gate capacitance of the power MOSFETs, and is approximated as:

$$P_{DR} = V_{IN} \times (Q_{G\_HI} + Q_{G\_LO}) \times f_{SW}$$

Where Q_{G_HI} and Q_{G_LO} are the total gate charge of the high-side and low-side FETs respectively at the typical 5V driver voltage. Gate charge loss differs from conduction and switching losses in that the majority of dissipation occurs in the LM3753/54 and VDD regulator.

The switching loss occurs during the brief transition period as the FET turns on and off, during which both current and voltage is present in the channel of the FET. This can be approximated as:

$$P_{SW\_ON} = V_{IN} \times I_{L\_VL} \times \alpha \times R_{G\_ON} \times f_{SW} \times \left(\frac{Q_{GD}}{V_{DR} - V_{PLT2}} + C_{ISS} \times Ln\left(\frac{V_{DR} - V_{TH}}{V_{DR} - V_{PLT1}} \right) \right)$$

$$P_{SW\_OFF} = V_{IN} \times I_{L\_PK} \times \beta \times R_{G\_OFF} \times f_{SW} \times \left(\frac{Q_{GD}}{V_{PLT2}} + C_{ISS} \times Ln\left(\frac{V_{PLT2}}{V_{TH}} \right) \right)$$

Where Q_{GD} is the high-side FET Miller charge with a V_{DS} swing between 0 to V_{IN}; C_{ISS} is the input capacitance of the high-side MOSFET in its off state with $V_{DS} = V_{IN}$. α and β are fitting coefficient numbers, which are usually between 0.5 to 1, depending on the board level parasitic inductances and reverse recovery of the low-side power MOSFET body diode. Under ideal condition, setting α = β = 0.5 is a good starting point. Other variables are defined as:

$$I_{L\_VL} = I_{OUT} - 0.5 \times \Delta I_L$$

$$I_{L\_PK} = I_{OUT} + 0.5 \times \Delta I_L$$

$$V_{PLT1} \approx V_{TH} + \frac{I_{L\_VL}}{g_{mFET\_HI}}$$

$$V_{PLT2} \approx V_{TH} + \frac{I_{L\_PK}}{g_{mFET\_HI}}$$

$$R_{G\_ON} = 5 + R_{G\_INT} + R_{G\_EXT}$$

$$R_{G\_OFF} = 2 + R_{G\_INT} + R_{G\_EXT}$$

Switching loss is calculated for the high-side FET only. 5 and 2 represent the LM3753/54 high-side driver resistance in the transient region. R_{G_INT} is the gate resistance of the high-side FET, and R_{G_EXT} is the extra external gate resistance if applicable. R_{G_EXT} may be used to damp out excessive parasitic ringing at the switch node.

For this example, the maximum drain-to-source voltage applied to either MOSFET is 18V. The maximum drive voltage at the gate of the high-side MOSFET is 5V, and the maximum drive voltage for the low-side MOSFET is 5V. The selected MOSFET must be able to withstand 18V plus any ringing from drain to source, and be able to handle at least 5V plus ringing from gate to source. If the duty cycle of the converter is small, then the high-side MOSFET should be selected with a low gate charge in order to minimize switching loss whereas the bottom MOSFET should have a low $R_{DS(on)}$ to minimize conduction loss.

For a typical input voltage of 12V and output current of 25A per phase, the MOSFET selections for the design example are SIR850DP for the high-side MOSFET and 2 x SIR892DP for the low-side MOSFET.

A 2.2Ω resistor for the high-side gate drive may be added in series with the HG output. This helps to control the MOSFET turn-on and ringing at the switch node. Additionally, 0.5A Schottky diodes may be placed across the high-side MOSFETs. The external Schottky diodes have a much faster recovery characteristic than the MOSFET body diode, and help to minimize switching spikes by clamping the SW pin to VIN. Another technique to control ringing at the switch node is to place an RC snubber from SW to PGND directly across the low-side MOSFET. Typical values at 300 kHz are 1Ω and 680 pF.

To improve efficiency, 3A Schottky diodes may be placed across the low-side MOSFETs. The external Schottky diodes have a much lower forward voltage than the MOSFET body diode, and help to minimize the loss due to the body diode recovery characteristic.

EN and VIN UVLO

For operation at 6V minimum input, set the EN divider to enable the LM3753/54 at approximately 5.5V nominal. Values of R_{UV1} = 1.37 kΩ and R_{UV2} = 4.02 kΩ will meet the target threshold.

CURRENT SENSE

For resistor current sense, a 1 mΩ 1W resistor is used for a full scale voltage of 25 mV at 25A out.

For DCR sensing, R_S is equal to the inductor resistance of R_L = 0.32 mΩ plus an estimated trace resistance of 0.2 mΩ.. The full scale voltage is about 13 mV at 25A. For equal time constants, the relationship of the integrating RC is determined by:

$$R_{DCR} \times C_{DCR} = \frac{L}{R_L}$$

Choosing C_{DCR} = 0.15 µF:

$$R_{DCR} = 440\ nH / (0.15\ \mu F \times 0.52\ m\Omega) = 5.64\ k\Omega.$$

Using a standard value of 5.90 kΩ, the average current through R_{DCR} is calculated as 203 µA from:

$$I_{DCR} = V_{OUT} / R_{DCR}$$

I_{DCR} is sufficiently high enough to keep the CS input bias current from being a significant error term.

CURRENT LIMIT

For the design example, the desired current limit set point is chosen as 34.5A peak per phase, which is about 25% above the full load peak value. Using DCR sense with R_S = 0.52 mΩ:

$$R_{ILIM} = 34.5A \times 0.52\ m\Omega / 94\ \mu A = 191\Omega$$

For resistor sense, the relatively low output inductor value forms a voltage divider with the intrinsic inductance of the sense resistor. When the MOSFETs switch, this adds a step to the otherwise triangular current sense voltage. The step voltage is simply the input voltage times the inductive divider. With L = 440 nH and L_S = 1 nH, the step voltage is:

$$V_{LS} = 12V \times 1\ nH / 441\ nH = 27.2\ mV$$

Using the same method as DCR sense, an RC filter is added to recover the actual resistive sense voltage. Choosing C = 1 nF the resistor is calculated as:

$$R = 1\ nH / (1\ nF \times 1\ m\Omega) = 1\ k\Omega$$

The current limit resistor is then calculated as:

$$R_{ILIM} = 34.5A \times 1\ m\Omega / 94\ \mu A = 367\Omega$$

The closest standard value of 365Ω 1% is selected for the design example.

TRACK (LM3753)

For the design example, an external voltage of 3.3V is used as the controlling voltage. The divider values are set so that both voltages will rise together, with V_{EXT} reaching its final value just before V_{OUT}. Following the method in the *Application Information* under *TRACKING (LM3753)* and allowing for a 120 mV offset between FB and TRACK, standard 1% values are selected for R_{T1} = 10 kΩ and R_{T2} = 35.7 kΩ.

SOFT-START (LM3754)

To prevent over-shoot, the soft-start time is set to be longer than the time it would take to charge the output voltage at the maximum output current. Following the equations in the *Application Information* under *SOFT-START (LM3754)*:

$$t_{SS(MIN)} = (1.2V \times 484\ \mu F) / (34.5A - 25A) = 61\ \mu s$$

Choosing a value of C_{SS} = 0.1 µF, the soft-start time is:

$$t_{SS} = (0.1\ \mu F \times 0.6V) / 10\ \mu A = 6\ ms$$

VCC, VDD and BOOT

VCC is used as the supply for the internal control and logic circuitry. A 4.7 µF ceramic capacitor provides sufficient filtering for VCC.

C_{VDD} provides power for both the high-side and low-side MOSGET gate drives, and is sized to meet the total gate drive current. Allowing for ΔV_{VDD} = 100 mV of ripple, the minimum value for C_{VDD} is found from:

$$C_{VDD} \geq \frac{Q_{G\_HI} + Q_{G\_LO}}{\Delta V_{VDD}}$$

Using Q_{G_HI} = 2 x 10 nC and Q_{G_LO} = 4 x 21 nC per controller with a 5V gate drive, the minimum value for C_{VDD} = 1.04 µF. To use common component values, C_{VDD1} and C_{VDD2} are also selected as 4.7 µF ceramic.

A general purpose NPN transistor is sized to meet the requirements for the VDD supply. Based on the gate charge of 104 nC per controller, the required current is found from:

$$I_{GC} = Q_{G\_TOTAL} \times f_{SW}$$

At 300 kHz, I_{GC} = 31.2 mA per controller. For a two controller system, the minimum HFE for the transistor is determined by:

$$HFE_{MIN} = I_{GC\_TOTAL} / 5\ mA$$

The power dissipated by the transistor is:

$$P_R = (V_{IN} - V_{DD}) \times I_{GC\_TOTAL}$$

The transistor must support 62.4 mA with an HFE of at least 12.5 over the entire operating range. At 18V in the power dissipated is 0.8W. A CJD44H11 in a DPAK case is chosen for the design example. A 0.047 µF capacitor from base to PGND will improve the transient performance of the VDD supply.

C_{BOOT} provides power for the high-side gate drive, and is sized to meet the required gate drive current. Allowing for ΔV_{BOOT} = 100 mV of ripple, the minimum value for C_{BOOT} is found from:

$$C_{BOOT} \geq \frac{Q_{G\_HI}}{\Delta V_{BOOT}}$$

Using Q_{G_HI} = 10 nC per phase with a 5V gate drive, the minimum value for C_{BOOT} = 0.1 µF. C_{BOOT} is selected as 0.22 µF ceramic per phase for the design example. A 0.5A Schottky diode is used for D_{BOOT} at each controller.

PRE-LOAD RESISTOR

For normal operation, a pre-load resistor is generally not required. During an abnormal fault condition with the output completely disconnected from the load, the output voltage may rise. This is primarily due to the high-side driver off-state bias current, and reverse leakage current of the high-side Schottky clamp diode.

At room temperature with 12V input, the reverse leakage of each 0.5A Schottky diode is about 15 µA. With the EN pin high and the $\overline{FAULT}$ pin low, the bias current in each high-side driver is about 105 µA. Allowing for a 2 to 1 variation, the maximum value of resistor to keep the output voltage from rising above 5% of its nominal value is found from:

$$R = 0.05 \times 1.2V / 330\ \mu A = 182\Omega$$

A value of 120Ω is selected for the design example. This represents a 10 mA pre-load at the rated output voltage, which is 0.01% of the 100A full load current.

CONTROL LOOP COMPENSATION

The LM3753 uses voltage-mode PWM control to correct changes in output voltage due to line and load transients. Input voltage feed-forward is used to adjust the amplitude of the PWM ramp. This stabilizes the modulator gain from variations due to input voltage, providing a robust design solution. A fast inner current sharing circuit ensures good dynamic response to changes in load current.

The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, current sharing circuit, output filter and load. The second part is the error amplifier, which is a voltage type operational amplifier with a typical dc gain of 70 dB and a unity gain frequency of 15 MHz. *Figure 13* shows the power stage, error amplifier and current sharing components.

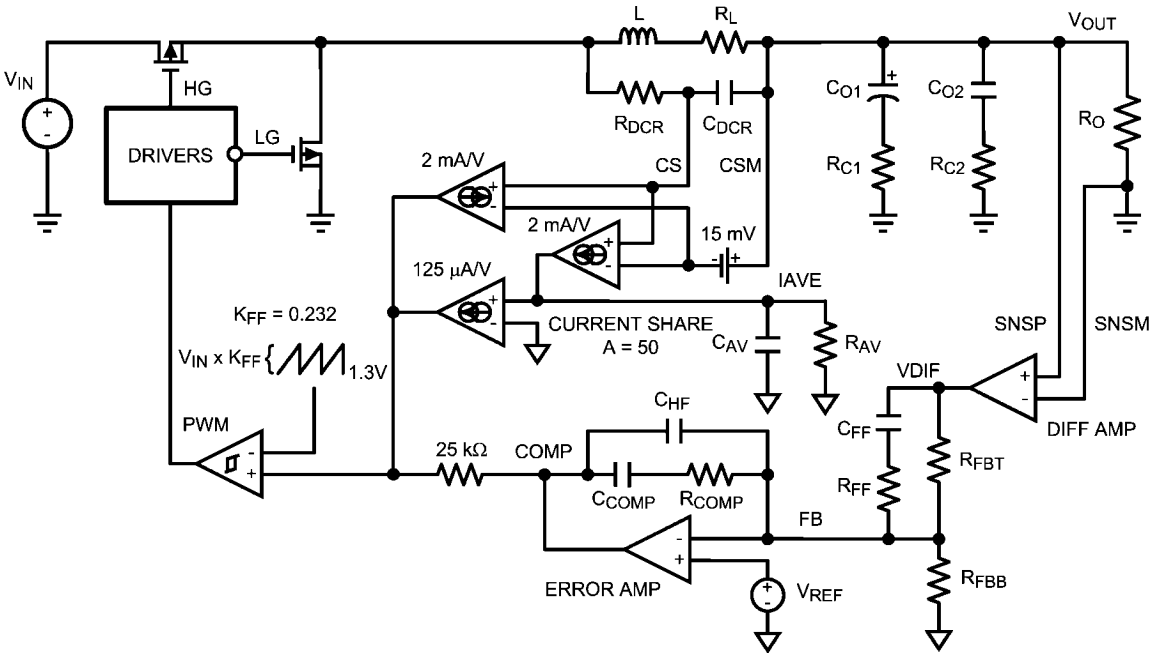


FIGURE 13. Power Stage, Error Amplifier and Current Sharing

The simplified power stage transfer function (also called the control-to-output transfer function) for the LM3753/54 can be written as:

$$\frac{\hat{v}_O}{\hat{v}_C} = A_{VP} \times \frac{1 + \frac{s}{\omega_Z}}{1 + \frac{s}{\omega_P \times Q_P} + \frac{s^2}{\omega_P^2}}$$

Where:

$$A_{VP} = \frac{K_m}{K_D} \qquad K_m = \frac{1}{(0.5 - D) \times R_i \times \frac{T}{L} + K_{FF}}$$

$$K_D = 1 + \frac{K_m \times R_i \times H_a(s)}{R_O} \qquad \omega_Z = \frac{1}{C_O \times R_C} \qquad \omega_P^2 = \frac{K_D}{L \times C_O}$$

$$\omega_P \times Q_P = \frac{K_D}{\frac{L}{R_O} + C_O \times (R_C + K_m \times R_i \times H_a(s))}$$

With:

$$D = \frac{V_O}{V_{IN}} \qquad R_i = A \times R_S$$

$$T = \frac{1}{f_{SW}} \qquad H_a(s) = \frac{s \times C_{AV} \times R_{AV}}{1 + s \times C_{AV} \times R_{AV}}$$

K_m is the dc modulator gain and R_i is the current-sharing gain. K_{FF} is the input voltage feed-forward term, which is internally set to a value of 0.232 V/V. The IAVE filter is accounted for by $H_a(s)$, which provides additional damping of the modulator transfer function.

R_{AV} sets the gain of the current averaging amplifier. A fixed value of 8 kΩ/phase must be used for proper scaling. Since the effective resistance is in parallel, each LM3753/54 should have a 4.02 kΩ 1% resistor at IAVE for 2-phase/controller operation. C_{AV} sets the IAVE filter time constant of the current sharing amplifier. For optimal performance of the current sharing circuit, the IAVE filter is designed to settle to its final value in five switching cycles. The optimal IAVE time constant is defined as:

$$T = C_{AV} \times R_{AV}$$

A value of $C_{AV} = 1/(R_{AV} \times f_{SW})$ per phase must be used for the optimal time constant. Each LM3753/54 should have a value of two times the normalized single phase value of C_{AV} at IAVE for 2-phase/controller operation. In this manner, the IAVE time constant maintains a fixed value of T for any number of phases.

Typical frequency response of the gain and the phase for the power stage are shown in *Figure 14* and *Figure 15*. It is designed for V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A per phase and a switching frequency of 300 kHz. For 2-phase operation R_{AV} = 4.02 kΩ and C_{AV} = 1000 pF. The power stage component values per phase are:

L = 0.44 µH, R_L = 0.52 mΩ, C_{O1} = 440 µF, R_{C1} = 2.5 mΩ, C_{O2} = 44 µF, R_{C2} = 1.5 mΩ, R_S = R_L = 0.52 mΩ and R_O = V_{OUT} / I_{OUT} = 48 mΩ.

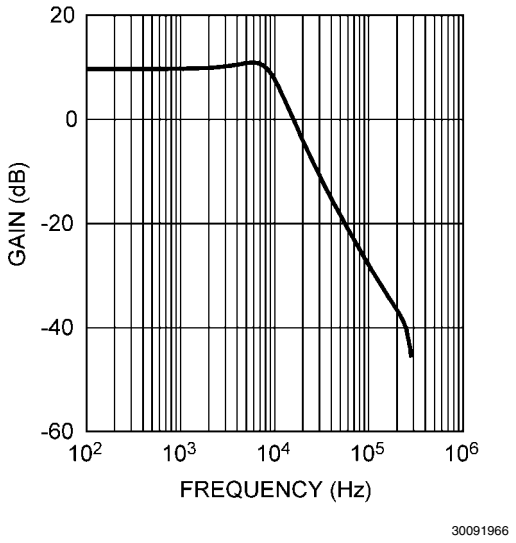


FIGURE 14. Power Stage Gain

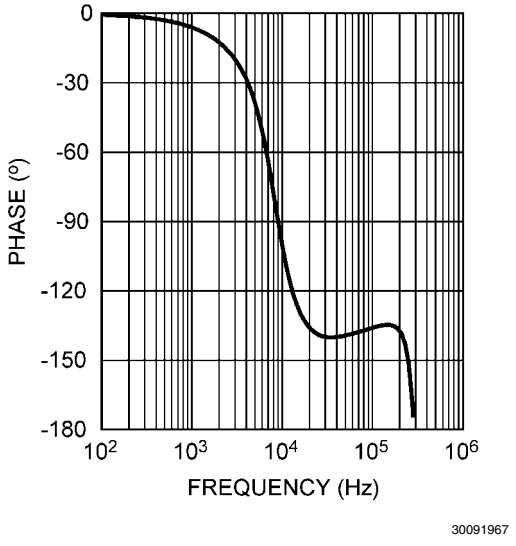


FIGURE 15. Power Stage Phase

Assuming a pole at the origin, the simplified equation for the error amplifier transfer function can be written in terms of the mid-band gain as:

$$\frac{\hat{v}_C}{\hat{v}_O} = -\frac{A_{VM}}{K_{HF}} \times \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{FP}}} \times \frac{1 + \frac{s}{\omega_{FZ}}}{1 + \frac{s}{\omega_{HF}}}$$

Where:

$$A_{VM} = \frac{R_{COMP}}{R_{FBT}} \qquad K_{HF} = 1 + \frac{C_{HF}}{C_{COMP}}$$

$$\omega_{ZEA} = \frac{1}{C_{COMP} \times R_{COMP}} \qquad \omega_{FZ} = \frac{1}{C_{FF} \times (R_{FF} + R_{FBT})}$$

$$\omega_{FP} = \frac{1}{C_{FF} \times R_{FF}} \qquad \omega_{HF} = \frac{C_{HF} + C_{COMP}}{C_{HF} \times C_{COMP} \times R_{COMP}}$$

In general, the goal of the compensation circuit is to give high gain, a bandwidth that is between one-fifth and one-tenth of the switching frequency, and at least 45° of phase margin.

Control Loop Design Procedure

Once the power stage design is complete, the power stage components are used to determine the proper frequency compensation. Knowing the dc modulator gain and assuming an ideal single-pole system response, the mid-band error amplifier gain is set by the target crossover frequency. Based on the ideal amplifier transfer function, the zero-pair is set to cancel the complex conjugate pole of the output filter. One pole is set to cancel the ESR of the output capacitor. The second pole is set equal to the switching frequency. A correction factor is used to accommodate the modulator damping when the output filter pole is within a decade of the target crossover frequency.

The compensation components will scale from the feedback divider ratio and selection of the bottom feedback divider resistor. A maximum value for the divider current is typically set at 1 mA. Using a divider current of 200 µA will allow for a reasonable range of values. For the bottom feedback resistor $R_{FBB} = V_{REF} / 200\ \mu A = 3\ k\Omega$. Choosing a standard 1% value of 3.01 kΩ, the top feedback resistor is found from:

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

For $V_{OUT} = 1.2V$ and $V_{REF} = 0.6V$, $R_{FBT} = 3.01\ k\Omega$.

Based on the previously defined power stage values, calculate general terms:

$$D = \frac{V_O}{V_{IN}} \qquad R_i = A \times R_S \qquad T = \frac{1}{f_{SW}}$$

$$K_m = \frac{1}{(0.5 - D) \times R_i \times \frac{T}{L} + K_{FF}}$$

For the design example D = 0.1, $R_i = 0.026\Omega$, T = 3.33 µs and $K_m = 3.22$.

Calculate the output filter pole frequency and the ESR zero frequency from:

$$\omega_P = \frac{1}{\sqrt{L \times C_O}} \qquad \omega_Z = \frac{1}{C_O \times R_C}$$

For the output filter pole using $C_O = C_{O1} + C_{O2}$, $\omega_P = 68.5$ krad/sec. Since $C_{O1} >> C_{O2}$, the ESR zero is calculated using C_{O1} and R_{C1} as $\omega_Z = 909$ krad/sec.

Choose a target crossover frequency f_C greater than the minimum control loop bandwidth from the *OUTPUT CAPACITORS* section. The optimum value of the crossover frequency is usually between 5 and 10 times the filter pole frequency. With $f_P = \omega_P / (2 \times \pi) = 10.9$ kHz, this places f_C between 54.5 kHz and 109 kHz. The upper limit for f_C is typically set at 1/5 of the switching frequency.

$$\omega_C = 2 \times \pi \times f_C \qquad \omega_{SW} = 2 \times \pi \times f_{SW}$$

Choosing $f_C = 60$ kHz for the design example $\omega_C = 377$ krad/sec. The switching frequency is $\omega_{SW} = 1.88$ Mrad/sec.

For output capacitors with very low ESR, if the target crossover frequency is more than 10 times the filter pole frequency, bandwidth limiting of the error amplifier may occur. See the *Comprehensive Equations* section to incorporate the error amplifier bandwidth into the design procedure.

For reference, the parallel equivalent C_O and R_C at any frequency can be calculated from:

$$C1 = C_{O1} \qquad R1 = R_{C1} \qquad C2 = C_{O2} \qquad R2 = R_{C2}$$

$$\omega = 2 \times \pi \times f \qquad X1 = \frac{1}{\omega \times C1} \qquad X2 = \frac{1}{\omega \times C2}$$

$$Z = \frac{\sqrt{R1^2 + X1^2} \times \sqrt{R2^2 + X2^2}}{\sqrt{(R1 + R2)^2 + (X1 + X2)^2}}$$

$$A = \tan^{-1}\left(\frac{X1}{R1}\right) + \tan^{-1}\left(\frac{X2}{R2}\right) - \tan^{-1}\left(\frac{X1 + X2}{R1 + R2}\right)$$

$$C_O = \frac{1}{\omega \times Z \times \sin(A)} \qquad R_C = Z \times \cos(A)$$

At the target crossover frequency X1 = 0.00603, X2 = 0.0603, Z = 0.00592 and A = 1.213. The parallel equivalent C_O = 478 µF and R_C = 2.1 mΩ.

Calculate the error amplifier gain coefficient and the compensation component values. The $(1 - \omega_P/\omega_C)$ term is the correction factor for the modulator damping.

$$G_C = \frac{\omega_C}{K_m \times \omega_P} \qquad C_{HF} = \frac{1}{\omega_{SW} \times G_C \times R_{FBT}}$$

$$C_{COMP} = C_{HF} \times \left(\frac{\omega_{SW}}{\omega_P} - 1\right) \times \left(1 - \frac{\omega_P}{\omega_C}\right)$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}}$$

$$R_{FF} = R_{FBT} \times \frac{\omega_P}{\omega_Z - \omega_P} \qquad C_{FF} = \frac{1}{\omega_Z \times R_{FF}}$$

For the design example, the calculated values are G_C = 1.71, C_{HF} = 103 pF, C_{COMP} = 2236 pF, R_{COMP} = 6527Ω, R_{FF} = 245 and C_{FF} = 4483 pF.

Using standard values of C_{HF} = 100 pF, C_{COMP} = 2200 pF, R_{COMP} = 6.2 kΩ, R_{FF} = 240Ω and C_{FF} = 4700 pF, the error amplifier plots of gain and phase are shown in *Figure 16* and *Figure 17*.

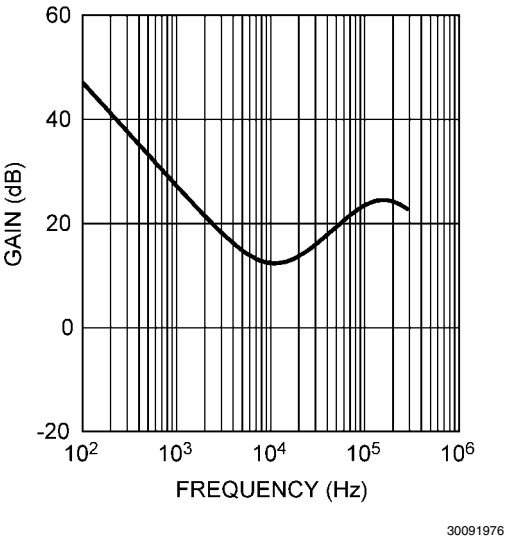


FIGURE 16. Error Amplifier Gain

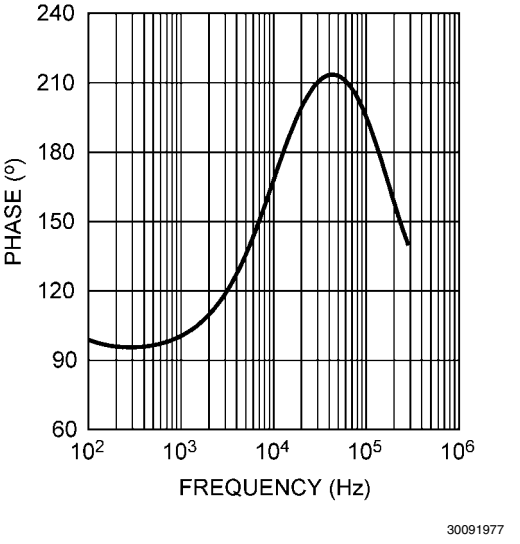


FIGURE 17. Error Amplifier Phase

The complete control loop transfer function is equal to the product of the power stage transfer function and error amplifier transfer function. For the Bode plots, the overall loop gain is the equal to the sum in dB and the overall phase is equal to the sum in degrees. Results are shown in *Figure 18* and *Figure 19*. The crossover frequency is 57 kHz with a phase margin of 73°.

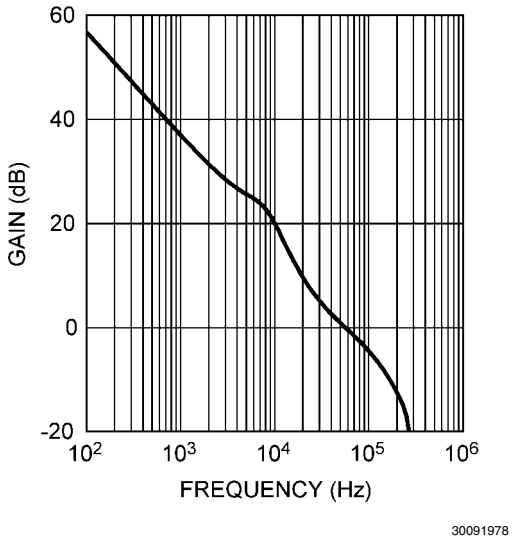


FIGURE 18. Control Loop Gain

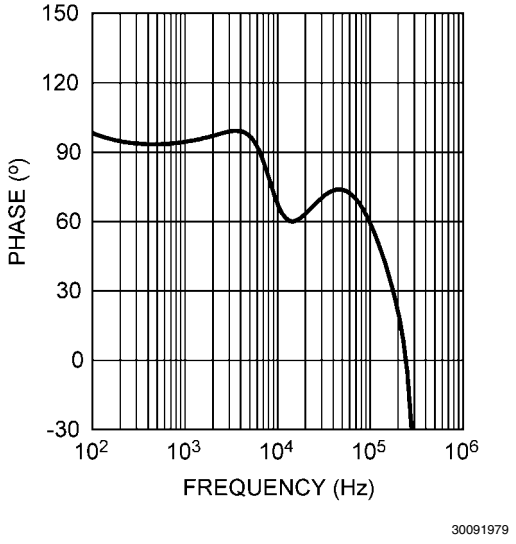


FIGURE 19. Control Loop Phase

For the small-signal analysis, it is assumed that the control voltage at the COMP pin is dc. In practice, the output ripple voltage is amplified by the error amplifier gain at the switching frequency, which appears at the COMP pin adding to the control ramp. This tends to reduce the modulator gain, which may lower the actual control loop crossover frequency. This effect is greatly reduced as the number of phases is increased.

Efficiency and Thermal Considerations

The buck regulator steps down the input voltage and has a duty ratio D of:

$$D = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta}$$

Where η is the estimated converter efficiency. The efficiency is defined as:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL\_LOSS}}$$

The total power dissipated in the power components can be obtained by adding together the loss as mentioned in the *OUTPUT INDUCTORS*, *OUTPUT CAPACITORS*, *INPUT CAPACITORS* and *MOSFETS* sections.

The highest power dissipating components are the power MOSFETs. The easiest way to determine the power dissipated in the MOSFETs is to measure the total conversion loss ($P_{IN} - P_{OUT}$), then subtract the power loss in the capacitors, inductors, LM3753/54 and VDD regulator. The resulting power loss is primarily in the switching MOSFETs. Selecting MOSFETs with exposed pads will aid the power dissipation of these devices. Careful attention to $R_{DS(on)}$ at high temperature should be observed.

If a snubber is used, the power loss can be estimated with an oscilloscope by observation of the resistor voltage drop at both the turn-on and turn-off transitions. Assuming that the RC time constant is << 1 / f_{SW}:

$$P = ½ \times C \times (V_P^2 + V_N^2) \times f_{SW}$$

V_P and V_N represent the positive and negative peak voltage across the snubber resistor, which is ideally equal to V_{IN}.

LM3753/54 and VDD REGULATOR OPERATING LOSS

These terms accounts for the currents drawn at the VIN and VDD pins, used for driving the logic circuitry and the power MOSFETs. For the LM3753/54, the VIN current is equal to the steady state operating current I_{VIN}. The VDD current is primarily determined by the MOSFET gate charge current I_{GC}, which is defined as:

$$I_{GC} = Q_{G\_TOTAL} \times f_{SW}$$

$$P_D = (V_{IN} \times I_{VIN}) + (V_{DD} \times I_{GC})$$

Q_{G_TOTAL} is the total gate charge of the MOSFETs connected to each LM3753/54. P_D represents the total power dissipated in each LM3753/54. I_{VIN} is about 15 mA from the *Electrical Characteristics* table. The LM3753/54 has an exposed thermal pad to aid power dissipation.

The power dissipated in the VDD regulator is determined by:

$$P_R = (V_{IN} - V_{DD}) \times I_{GC\_TOTAL}$$

I_{GC_TOTAL} is the sum of the MOSFET gate charge currents for all of the controllers.

Layout Considerations

To produce an optimal power solution with a switching converter, as much care must be taken with the layout and design of the printed circuit board as with the component selection. The following are several guidelines to aid in creating a good layout.

KELVIN TRACES for GATE DRIVE and SENSE LINES

The HG and SW pins provide the gate drive and return for the high-side MOSFETs. These lines should run as parallel pairs to each MOSFET, being connected as close as possible to the respective MOSFET gate and source. Likewise the LG and PGND pins provide the gate drive and return for the low-side MOSFETs. A good ground plane between the PGND pin and the low-side MOSFETs source connections is needed to carry the return current for the low-side gates.

The SNSP and SNSM pins of the Master should be connected as a parallel pair, running from the output power and ground sense points. Keep these lines away from the switch node

and output inductor to avoid stray coupling. If possible, the SNSP and SNSM traces should be shielded from the switch node by ground planes.

SGND and PGND CONNECTIONS

Good layout techniques include a dedicated ground plane, usually on an internal layer adjacent to the LM3753/54 and signal component side of the board. Signal level components connected to FB, TRACK/SS, FREQ, IAVE, EN and PH along with the VCC and VIN bypass capacitors should be tied directly to the SGND pin. Connect the SGND and PGND pins directly to the DAP, with vias from the DAP to the ground plane. The ground plane is then connected to the input capacitors and low-side MOSFET source at each phase.

MINIMIZE the SWITCH NODE

The copper area that connects the power MOSFETs and output inductor together radiates more EMI as it gets larger. Use just enough copper to give low impedance for the switching currents and provide adequate heat spreading for the MOSFETs.

LOW IMPEDANCE POWER PATH

In a buck regulator the primary switching loop consists of the input capacitor connection to the MOSFETs. Minimizing the area of this loop reduces the stray inductance, which minimizes noise and possible erratic operation. The ceramic input capacitors at each phase should be placed as close as possible to the MOSFETs, with the VIN side of the capacitors connected directly to the high-side MOSFET drain, and the PGND side of the capacitors connected as close as possible to the low-side source. The complete power path includes the input capacitors, power MOSFETs, output inductor, and output capacitors. Keep these components on the same side of the board and connect them with thick traces or copper planes. Avoid connecting these components through vias whenever possible, as vias add inductance and resistance. In general, the power components should be kept close together, minimizing the circuit board losses.

Comprehensive Equations

POWER STAGE TRANSFER FUNCTION

To include all terms, it is easiest to use the impedance form of the equation:

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{K_m \times Z_O}{Z_O + Z_L + K_m \times R_i \times H(s) \times H_a(s)}$$

Where:

$$K_m = \frac{1}{(0.5 - D) \times R_i \times \frac{T}{L} + K_{FF}}$$

$$Z_O = \frac{R_O \times (1 + s \times C_O \times R_C)}{1 + s \times C_O \times (R_O + R_C)} \qquad Z_L = s \times L + R_{DC}$$

$$R_{DC} = R_{DS(on)\_HI} \times D + R_{DS(on)\_LO} \times (1 - D) + R_L + R_S$$

With:

$$D = \frac{V_O}{V_{IN}} \qquad R_i = A \times R_S \qquad H(s) = \frac{s^2}{\omega_n^2}$$

$$T = \frac{1}{f_{SW}} \qquad H_a(s) = \frac{s \times C_{AV} \times R_{AV}}{1 + s \times C_{AV} \times R_{AV}} \qquad \omega_n = \frac{\pi}{T}$$

ERROR AMPLIFIER TRANSFER FUNCTION

Using a single-pole operational amplifier model, the complete error amplifier transfer function is given by:

$$\frac{\hat{v}_C}{\hat{v}_O'} = -G_{EA}(s) \times \frac{1}{1 + \left(\frac{1}{A_{OL}} + \frac{s}{\omega_{BW}}\right) \times \left(1 + G_{FB}(s)\right)}$$

Where the open loop gain A_{OL} = 3162 (70 dB) and the unity gain bandwidth $\omega_{BW} = 2 \times \pi \times f_{BW}$.

The ideal transfer function is expressed in terms of the mid-band gain as:

$$G_{EA}(s) = \frac{A_{VM}}{K_{HF}} \times \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{FP}}} \times \frac{1 + \frac{s}{\omega_{FZ}}}{1 + \frac{s}{\omega_{HF}}}$$

The feedback gain is then:

$$G_{FB}(s) = \frac{A_{VM}}{K_{HF} \times K_{FB}} \times \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{FP}}} \times \frac{1 + \frac{s}{\omega_{FB}}}{1 + \frac{s}{\omega_{HF}}}$$

Where:

$$A_{VM} = \frac{R_{COMP}}{R_{FBT}} \qquad K_{HF} = 1 + \frac{C_{HF}}{C_{COMP}}$$

$$\omega_{ZEA} = \frac{1}{C_{COMP} \times R_{COMP}} \qquad \omega_{FZ} = \frac{1}{C_{FF} \times (R_{FF} + R_{FBT})}$$

$$\omega_{FP} = \frac{1}{C_{FF} \times R_{FF}} \qquad \omega_{HF} = \frac{C_{HF} + C_{COMP}}{C_{HF} \times C_{COMP} \times R_{COMP}}$$

$$K_{FB} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}} \qquad \omega_{FB} = \frac{1}{C_{FF} \times (R_{FF} + K_{FB} \times R_{FBT})}$$

ERROR AMPLIFIER BANDWIDTH LIMIT

When the ideal error amplifier gain reaches the open loop gain-bandwidth limit, the phase goes to zero. To incorporate the amplifier bandwidth into the design procedure, determine the boundary limit with respect to the ESR zero frequency:

$$\omega_{ZB} = \left(\omega_{BW} \times K_m \times \omega_P^2\right)^{0.333}$$

Based on the relative ESR zero, the crossover frequency is set at 1/3 of the bandwidth limiting frequency.

If $\omega_Z > \omega_{ZB}$, calculate the optimal crossover frequency from:

$$f_C = \frac{1}{(2 \times \pi) \times 3} \times \left(\omega_{BW} \times K_m \times \omega_P{}^2 \right)^{0.333}$$

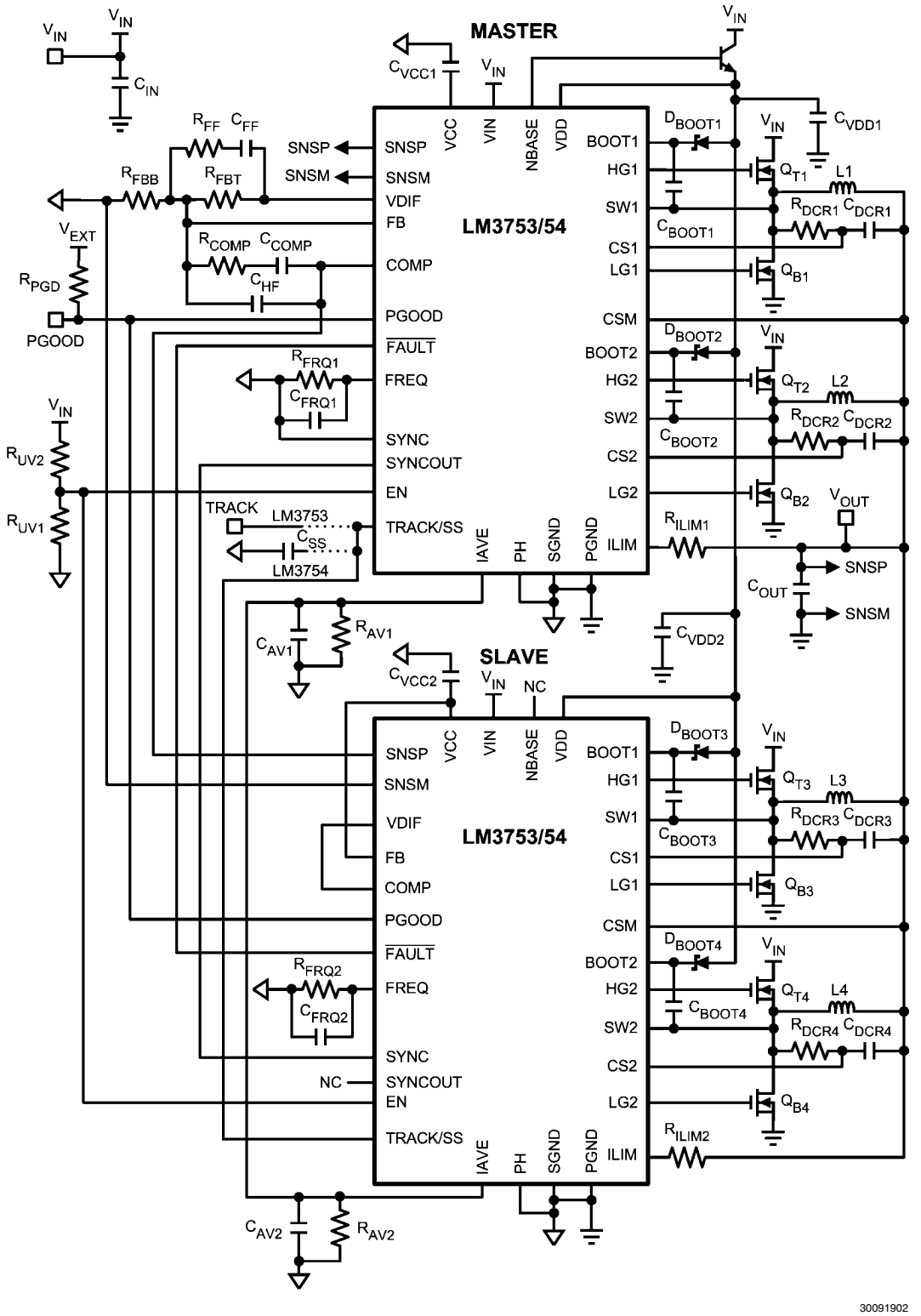
If $\omega_Z < \omega_{ZB}$, calculate the optimal crossover frequency from:

$$f_C = \frac{1}{(2 \times \pi) \times 3} \times \left(\frac{\omega_{BW} \times K_m \times \omega_P{}^2}{\omega_Z} \right)^{0.5}$$

Using this method, the maximum phase boost is achieved at the optimal crossover frequency.

In either case, the upper limit for f_C is typically set at 1/5 of the switching frequency.

Typical Application



All controllers in the system are the same part. The Master and Slave are differentiated by how they are connected in the system.

FIGURE 20. Typical Application

Design Examples

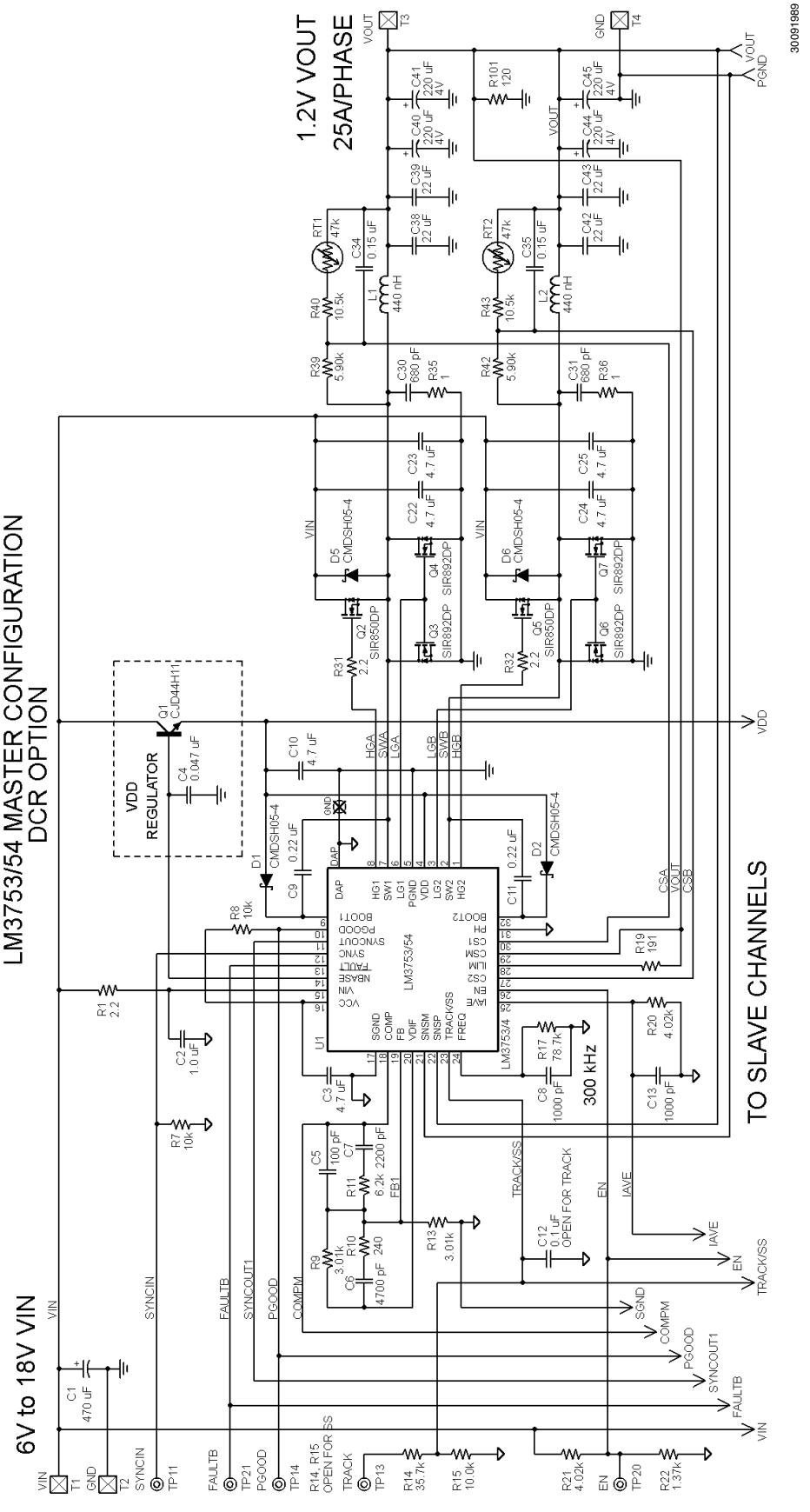


FIGURE 21. Master with DCR Sense

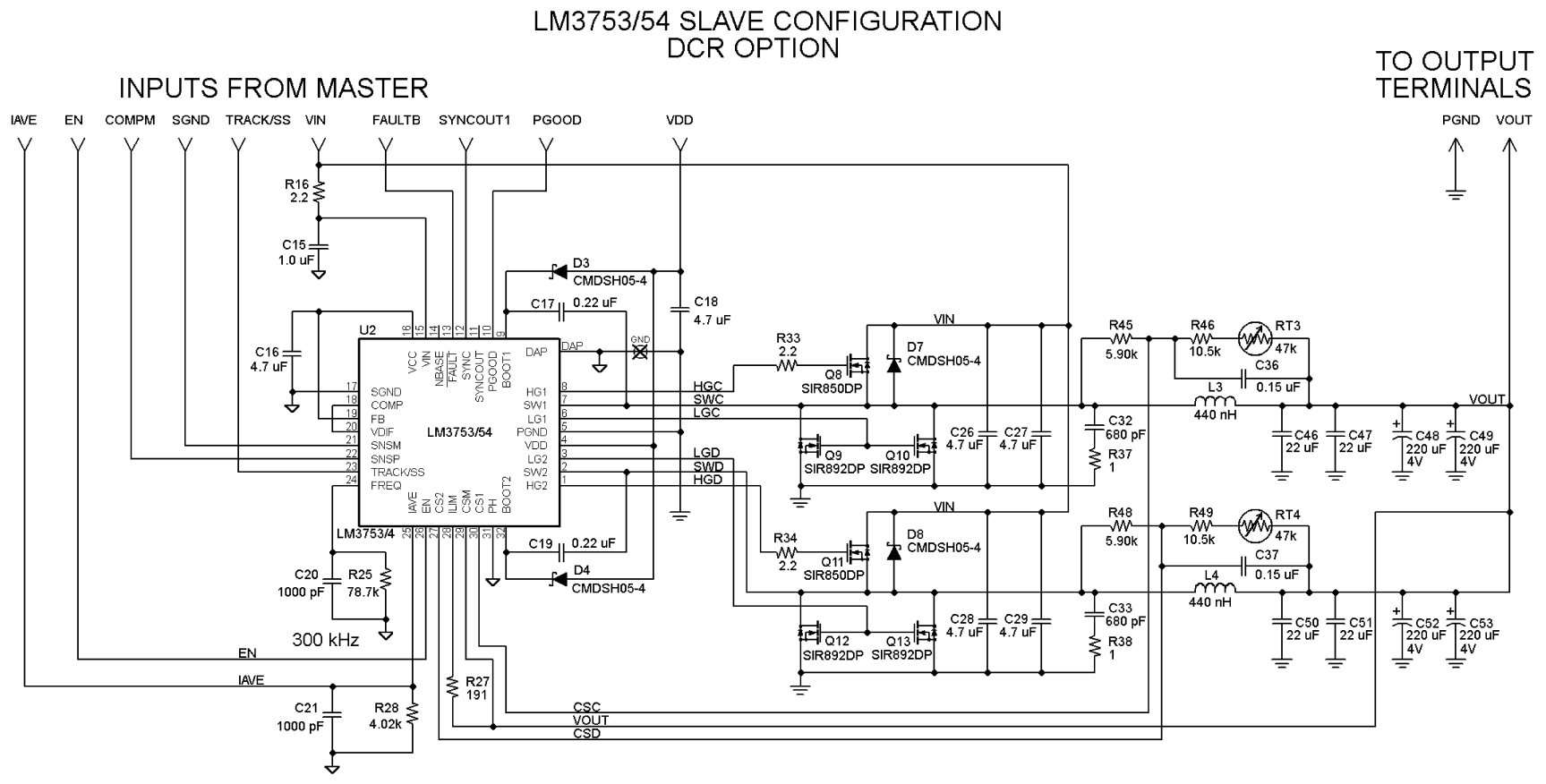


FIGURE 22. Slave with DCR Sense

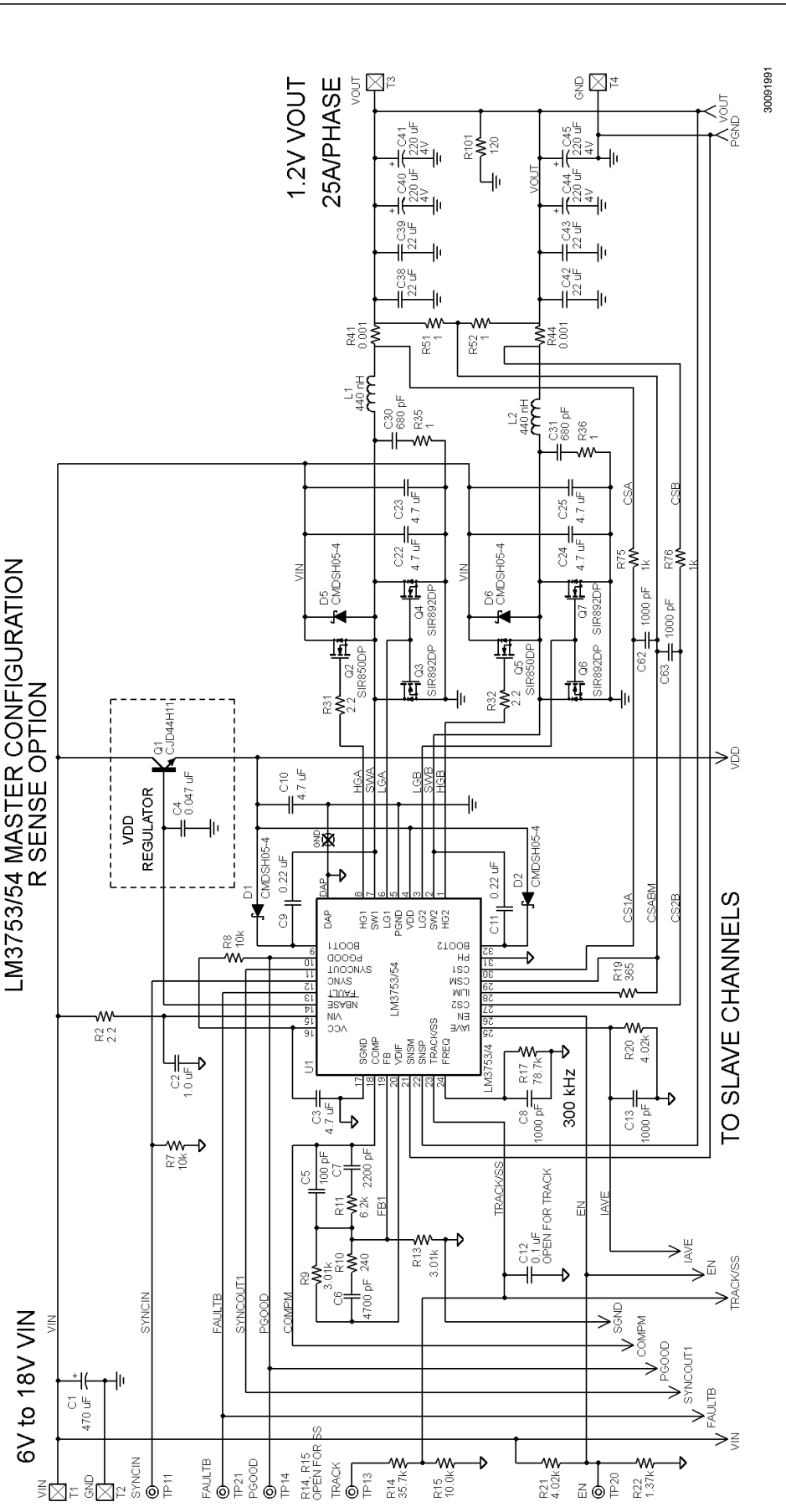


FIGURE 23. Master with Resistor Sense

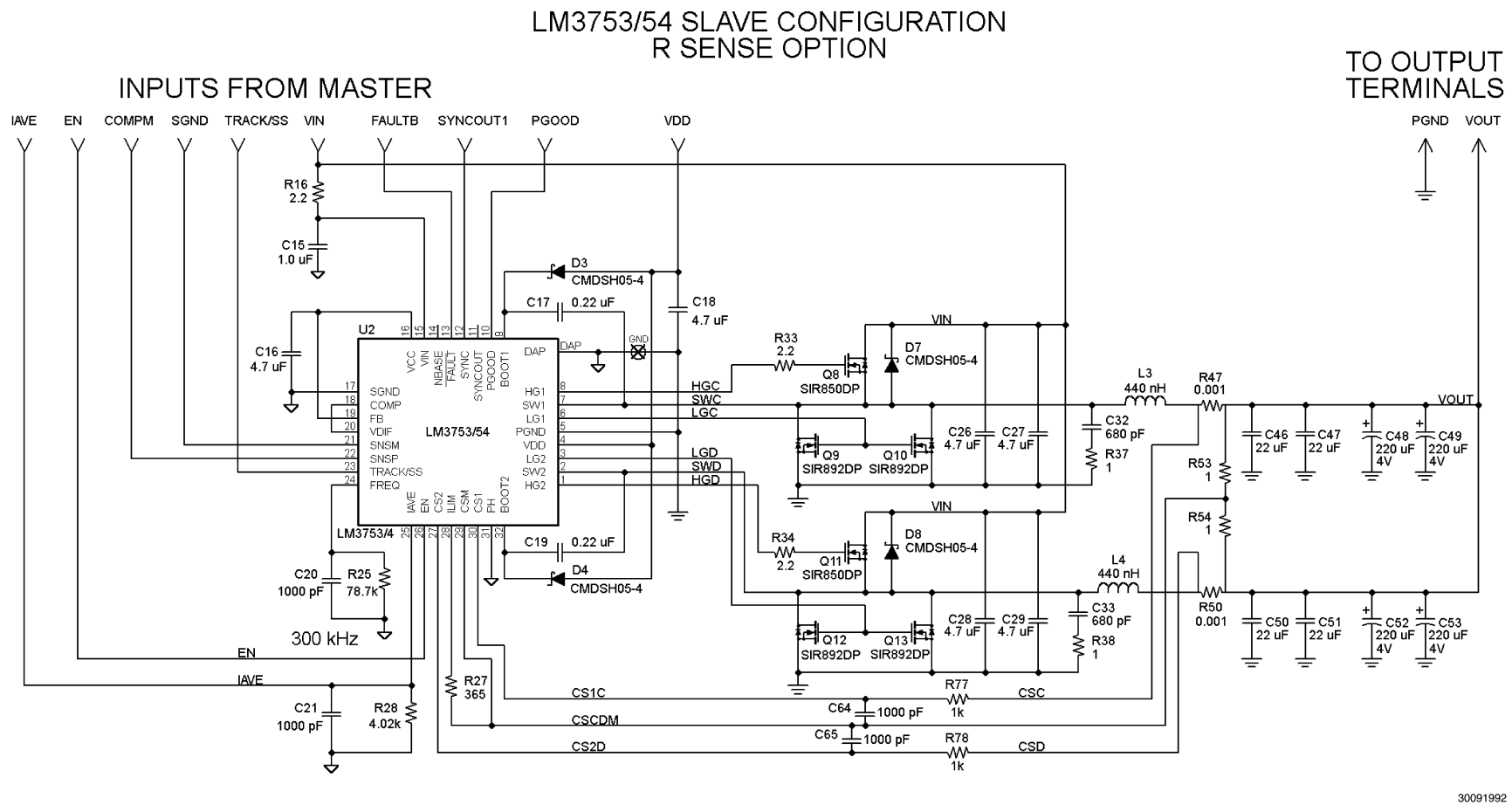
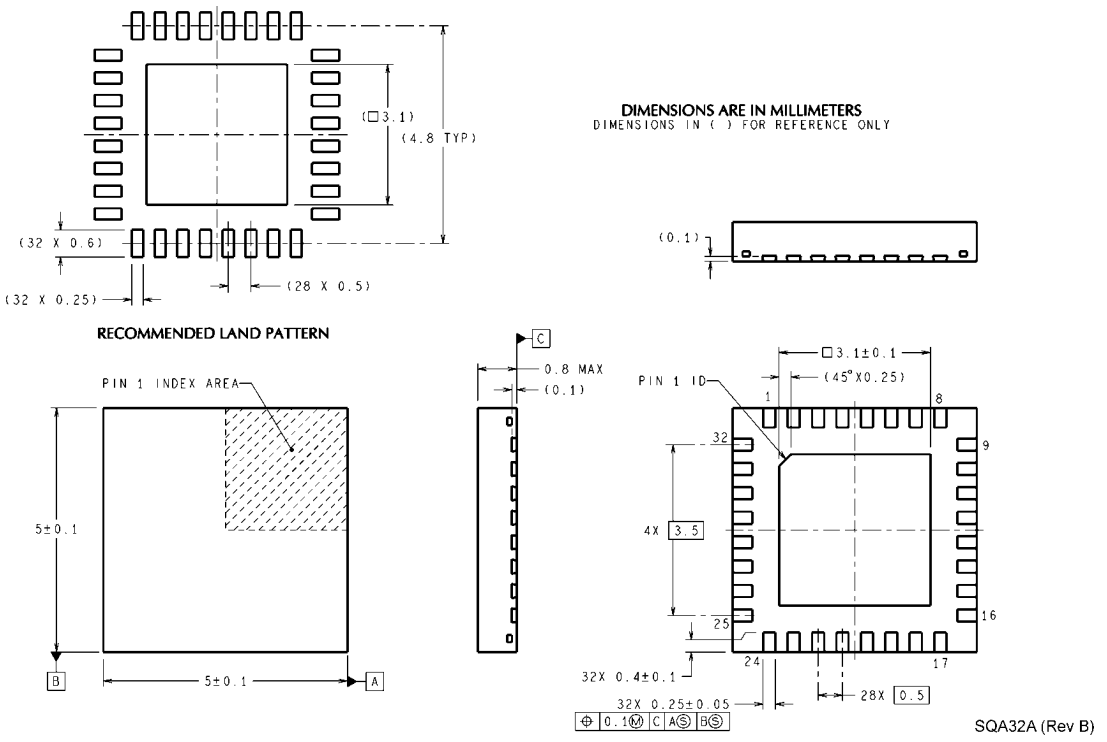


FIGURE 24. Slave with Resistor Sense

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

Notes

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