

# SN54AS867, SN54AS869 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

- Fully Programmable With Synchronous Counting and Loading
- SN74ALS867A and 'AS867 Have Asynchronous Clear; SN74ALS869 and 'AS869 Have Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Ripple-Carry Output for n-Bit Cascading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

## description

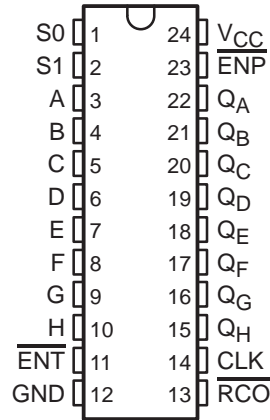
These synchronous, presettable, 8-bit up/down counters feature internal-carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable ( $\overline{\text{ENP}}$ ,  $\overline{\text{ENT}}$ ) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; they may be preset to any number between 0 and 255. The load-input circuitry allows parallel loading of the cascaded counters. Because loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

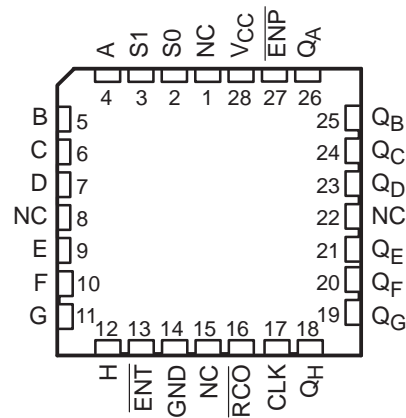
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Two count-enable ( $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$ ) inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both  $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$  must be low to count. The direction of the count is determined by the levels of the select (S0, S1) inputs as shown in the function table.  $\overline{\text{ENT}}$  is fed forward to enable RCO. RCO thus enabled produces a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow-carry pulse can be used to enable successive cascaded stages. Transitions at  $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$  are allowed regardless of the level of CLK. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the SN74ALS867A and 'AS867, changes at S0 and S1 that modify the operating mode have no effect on the Q outputs until clocking occurs. For the 'AS867 and 'AS869, any time  $\overline{\text{ENP}}$  and/or  $\overline{\text{ENT}}$  is taken high, RCO either goes or remains high. For the SN74ALS867A and SN74ALS869, any time  $\overline{\text{ENT}}$  is taken high, RCO either goes or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

SN54AS867, SN54AS869 . . . JT PACKAGE  
SN74ALS867A, SN74ALS869, SN74AS867,  
SN74AS869 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS867, SN54AS869 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

**SN54AS867, SN54AS869**  
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869**  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

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**description (continued)**

The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS867A, SN74ALS869, SN74AS867, and SN74AS869 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

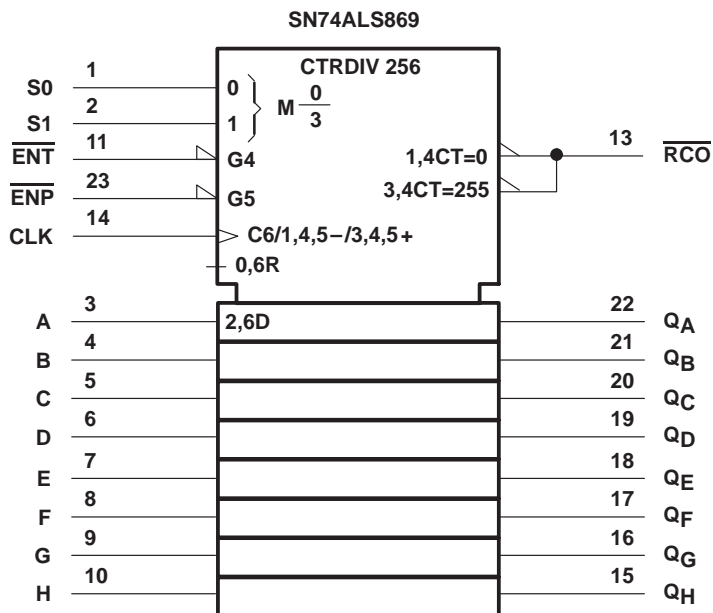
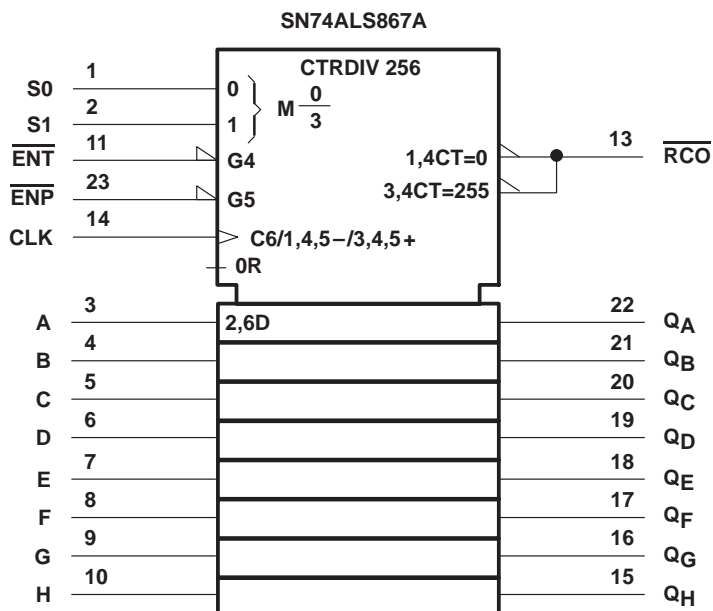
**FUNCTION TABLE**

<b>S1</b>	<b>S0</b>	<b>FUNCTION</b>
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

SN54AS867, SN54AS869  
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
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logic symbols†

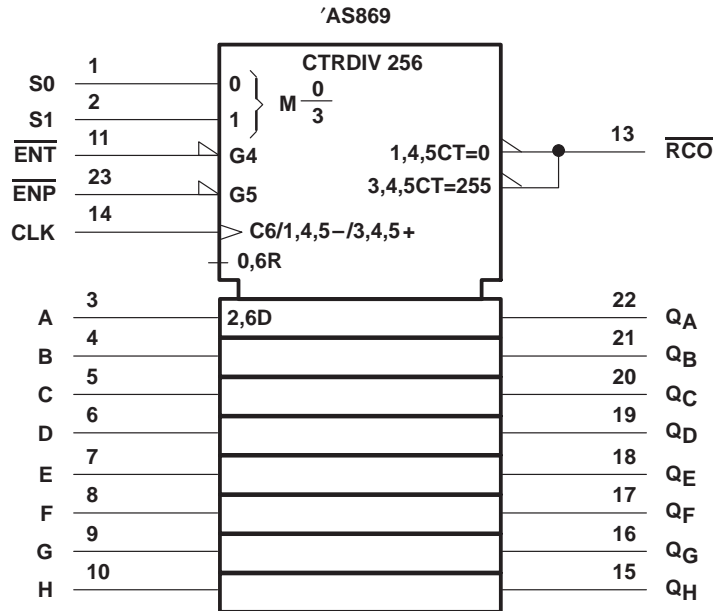
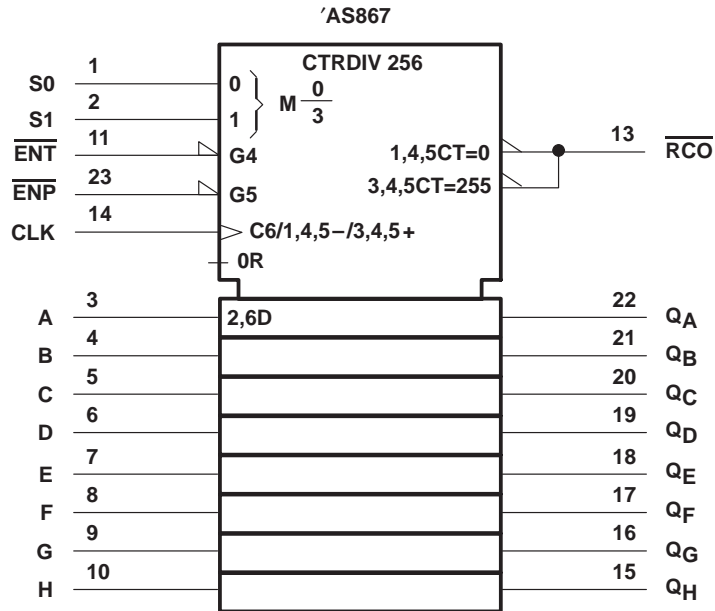


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869  
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

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logic symbols (continued)†

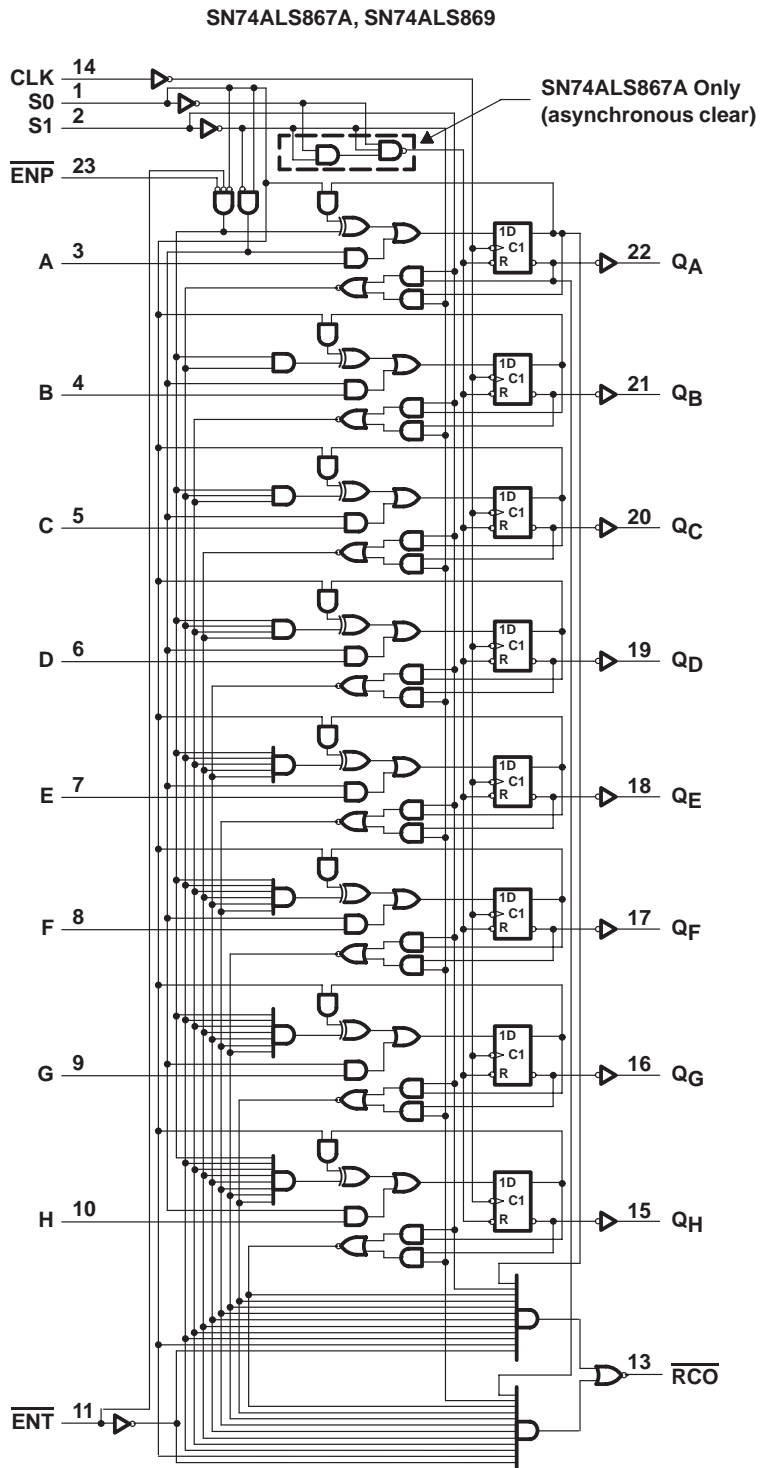


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869  
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
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logic diagram (positive logic)

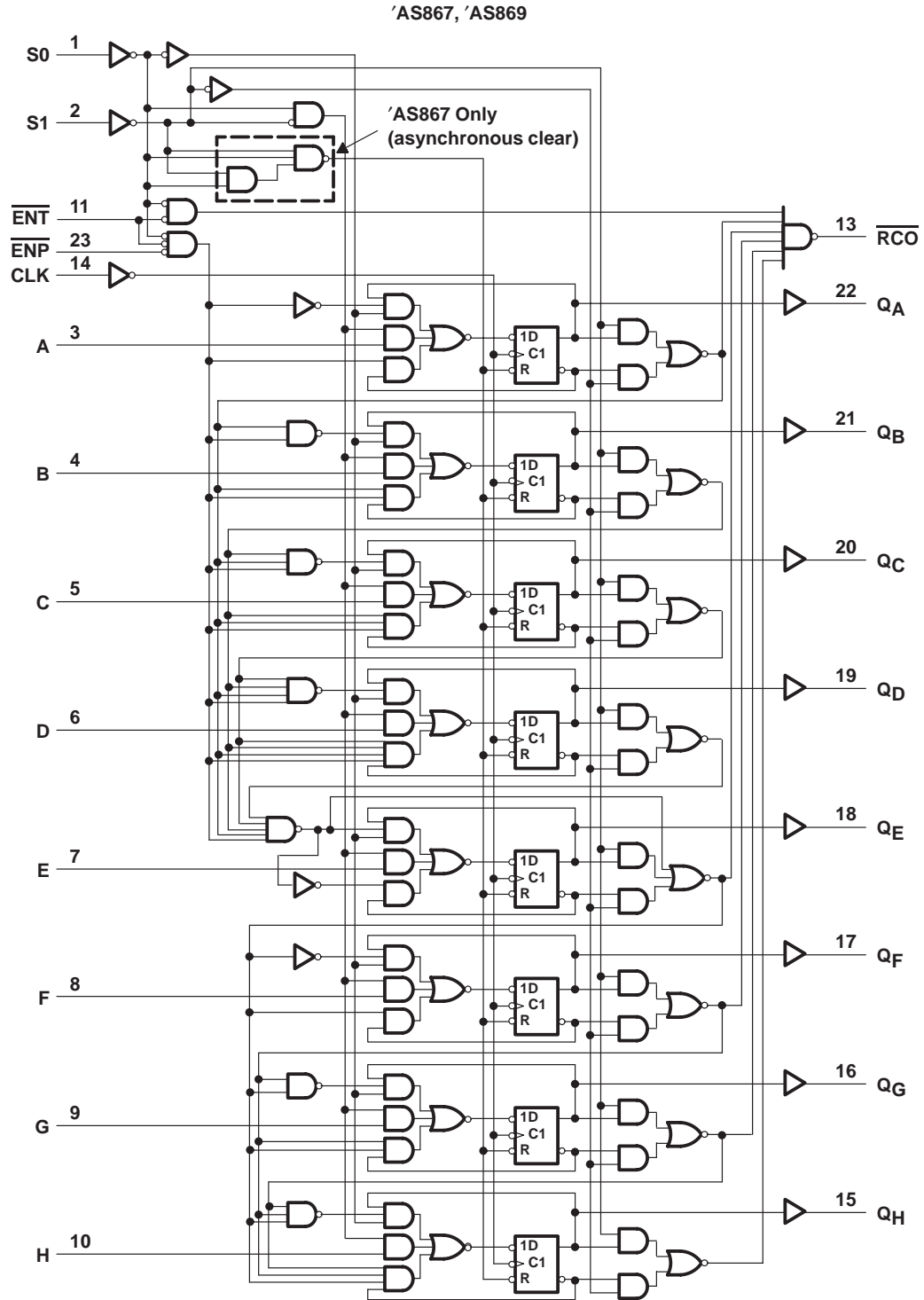


Pin numbers shown are for the DW, JT, and NT packages.

**SN54AS867, SN54AS869**  
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869**  
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**logic diagram (positive logic)**



Pin numbers shown are for the DW, JT, and NT packages.

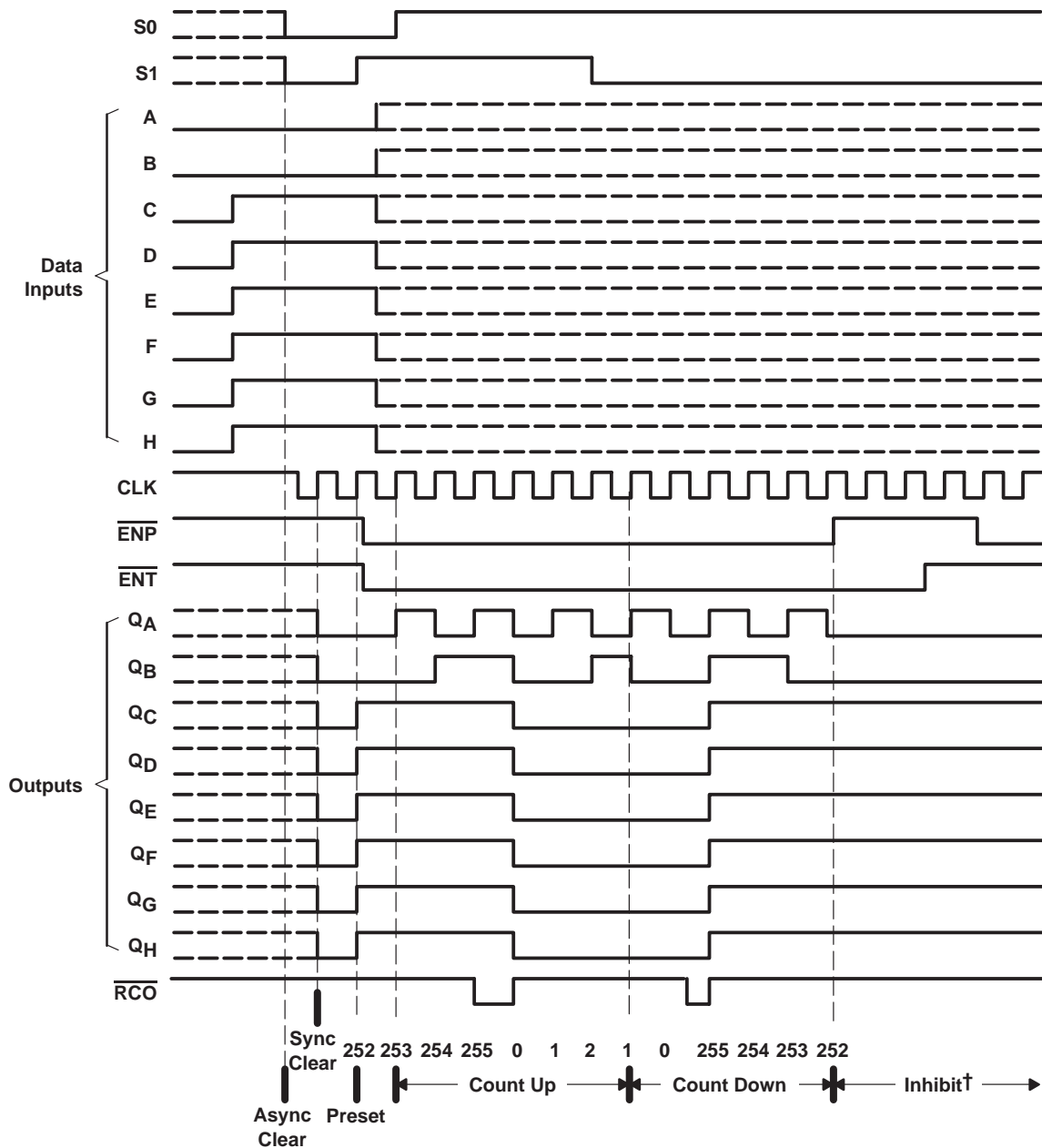


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**typical clear, preset, count, and inhibit sequences**

The following sequence is illustrated below:

1. Clear outputs to zero (SN74ALS867A and 'AS867 are asynchronous;  
 SN74ALS869 and 'AS869 are synchronous.)
2. Preset to binary 252
3. Count up to 253, 254, 255, 0, 1, and 2
4. Count down to 1, 0, 255, 254, 253, and 252
5. Inhibit



† ENT and ENP both must be low for counting to occur.

**SN54AS867, SN54AS869**  
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869**  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN74ALS867A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN74ALS867A			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–0.4	mA
$I_{OL}$	Low-level output current			8	mA
$f_{clock}$	Clock frequency	0		35	MHz
$t_{w(clock)}$	Pulse duration, CLK high or low	14			ns
$t_{w(clear)}$	Pulse duration of clear pulse, S0 and S1 low	10			ns
$t_{su}$	Setup time before CLK↑	Data inputs A–H	10		ns
		$\overline{ENP}$ or $\overline{ENT}$	15		
		S0 low and S1 high (load)	12		
		S0 high and S1 low (count down)	12		
		S0 and S1 high (count up)	12		
$t_h$	Hold time after CLK↑	S0 high after S1↑ or S1 high after S0↑	3		ns
		Data inputs A–H	0		
$T_A$	Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN74ALS867A			UNIT
		MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			–1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -0.4 mA$	$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 4 mA$	0.25	0.4	V
		$I_{OL} = 8 mA$	0.35	0.5	
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ , $V_I = 2.7 V$			20	μA
$I_{IL}$	$V_{CC} = 5.5 V$ , $V_I = 0.4 V$			–0.2	mA
$I_{O§}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	–30		–112	mA
$I_{CC}$	$V_{CC} = 5.5 V$		28	45	mA

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .





SN54AS867, SN54AS869  
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74ALS867A		
			MIN	MAX	
f <sub>max</sub>			35		MHz
t <sub>PLH</sub>	CLK	$\overline{RCO}$	4	14	ns
t <sub>PHL</sub>			4	14	
t <sub>PLH</sub>	CLK	Any Q	3	16	ns
t <sub>PHL</sub>			3	16	
t <sub>PLH</sub>	$\overline{ENT}$	$\overline{RCO}$	3	14	ns
t <sub>PHL</sub>			2	9	
t <sub>PHL</sub>	S0 or S1 (clear mode)	Any Q	8	26	ns
t <sub>PLH</sub>	S0 or S1 (count up/down)	$\overline{RCO}$	4	16	ns
t <sub>PHL</sub>			4	16	
t <sub>PLH</sub>	S0 or S1 (clear mode)	$\overline{RCO}$	4	16	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54AS867, SN54AS869**  
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869**  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN74ALS869	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN74ALS869			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-0.4	mA
$I_{OL}$	Low-level output current			8	mA
$f_{clock}$	Clock frequency	0		35	MHz
$t_{w(clock)}$	Pulse duration, CLK high or low	14			ns
$t_{su}$	Setup time before CLK↑	Data inputs A–H	10		ns
		$\overline{ENP}$ or $\overline{ENT}$	15		
		S0 and S1 low (clear)	13		
		S0 low and S1 high (load)	13		
		S0 high and S1 low (count down)	13		
		S0 and S1 high (count up)	13		
$t_h$	Hold time after CLK↑	S0 high after S1↑ or S1 high after S0↑	3		ns
		Data inputs A–H	0		
$T_A$	Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN74ALS869			UNIT
		MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -0.4 mA$	$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 4 mA$	0.25	0.4	V
		$I_{OL} = 8 mA$	0.35	0.5	
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ , $V_I = 2.7 V$			20	μA
$I_{IL}$	$V_{CC} = 5.5 V$ , $V_I = 0.4 V$			-0.2	mA
$I_{O}^{\S}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5 V$		28	45	mA

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



SN54AS867, SN54AS869  
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74ALS869		
			MIN	MAX	
f <sub>max</sub>			35		MHz
t <sub>PLH</sub>	CLK	$\overline{RCO}$	4	14	ns
t <sub>PHL</sub>			4	14	
t <sub>PLH</sub>	CLK	Any Q	3	16	ns
t <sub>PHL</sub>			3	16	
t <sub>PLH</sub>	$\overline{ENT}$	$\overline{RCO}$	3	14	ns
t <sub>PHL</sub>			2	9	
t <sub>PLH</sub>	S1 (count up/down)	$\overline{RCO}$	4	15	ns
t <sub>PHL</sub>			4	15	
t <sub>PLH</sub>	S0 (clear/load)	$\overline{RCO}$	4	16	ns
t <sub>PHL</sub>			4	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54AS867, SN54AS869**  
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869**  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS867	–55°C to 125°C
SN74AS867	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54AS867			SN74AS867			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			–2			–2	mA
$I_{OL}$	Low-level output current			20			20	mA
$f_{clock}^*$	Clock frequency	0		40	0		50	MHz
$t_{w(clock)}^*$	Pulse duration, CLK high or low	12.5			10			ns
$t_{w(clear)}^*$	Pulse duration of clear pulse, S0 and S1 low	12.5			10			ns
$t_{su}^*$	Setup time before CLK↑	Data inputs A–H	5		4			ns
		$\overline{ENP}$ or $\overline{ENT}$	9		8			
		S0 low and S1 high (load)	11		10			
		S0 and S1 low (clear)	11		10			
		S0 high and S1 low (count down)	42		40			
		S0 and S1 high (count up)	42		40			
$t_h^*$	Hold time after CLK↑			0			0	ns
$t_{skew}^*$	Skew time between S0 and S1 (maximum to avoid inadvertent clear)			8			7	ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54AS867, SN54AS869  
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54AS867		SN74AS867		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$		V	
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 20\text{ mA}$ , $V_{IL}$ on $\overline{ENT} = 0.7\text{ V}$	0.34		0.5			V	
						0.34 0.5		
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1		0.1	mA	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			40		40		$\mu\text{A}$
				20		20		
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-4		-4		mA
				-2		-2		
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30		-112	-30	-112	mA	
$I_{CC}$	$V_{CC} = 5.5\text{ V}$		134	195		134 195	mA	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$				UNIT
			SN54AS867		SN74AS867		
			MIN	MAX	MIN	MAX	
$f_{max}^*$			40		50		MHz
$t_{PLH}$	CLK	$\overline{RCO}$	5	31	5	22	ns
$t_{PHL}$			6	19	6	16	
$t_{PLH}$	CLK	Any Q	3	12	3	11	ns
$t_{PHL}$			4	16	4	15	
$t_{PLH}$	$\overline{ENT}$	$\overline{RCO}$	3	19	3	10	ns
$t_{PHL}$			5	21	5	17	
$t_{PLH}$	$\overline{ENP}$	$\overline{RCO}$	5	16	5	14	ns
$t_{PHL}$			5	21	5	17	
$t_{PHL}$	Clear (S0 or S1 low)	Any Q	7	23	7	21	ns

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54AS867, SN54AS869**  
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS869	–55°C to 125°C
SN74AS869	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54AS869			SN74AS869			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–2			–2	mA
$I_{OL}$	Low-level output current			20			20	mA
$f_{clock}^*$	Clock frequency			40			45	MHz
$t_w(\text{clock})^*$	Pulse duration, CLK high or low	12.5			11			ns
$t_{su}^*$	Setup time before CLK↑	Data inputs A–H	6		5			ns
		$\overline{ENP}$ or $\overline{ENT}$	10		9			
		S0 low and S1 high (load)	13		11			
		S0 and S1 low (clear)	13		11			
		S0 high and S1 low (count down)	52		50			
		S0 and S1 high (count up)	52		50			
$t_h^*$	Hold time after CLK↑			0			0	ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54AS867, SN54AS869  
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869  
**SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54AS869		SN74AS869		UNIT
			MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA			V <sub>CC</sub> - 2		V
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> - 2*				
V <sub>OL</sub>	$\overline{\text{RCO}}$	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, V <sub>IL</sub> on $\overline{\text{ENT}}$ = 0.7 V	0.34	0.5			V
	Other outputs				0.34	0.5	
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1	0.1	mA
I <sub>IH</sub>	$\overline{\text{ENT}}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			40	40	μA
	Other inputs				20	20	
I <sub>IL</sub>	$\overline{\text{ENT}}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V			-4	-4	mA
	Other inputs				-2	-2	
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30	-112	-30	-112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V	134	195	134	195	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			SN54AS869		SN74AS869		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			40		45	MHz	
t <sub>PLH</sub>	CLK	$\overline{\text{RCO}}$	6	35	6	35	ns
t <sub>PHL</sub>			6	20	6	18	
t <sub>PLH</sub>	CLK	Any Q	3	12	3	11	ns
t <sub>PHL</sub>			4	16	4	15	
t <sub>PLH</sub>	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	25	3	15	ns
t <sub>PHL</sub>			6	21	6	17	
t <sub>PLH</sub>	$\overline{\text{ENP}}$	$\overline{\text{RCO}}$	5	27	5	19	ns
t <sub>PHL</sub>			6	21	6	18	

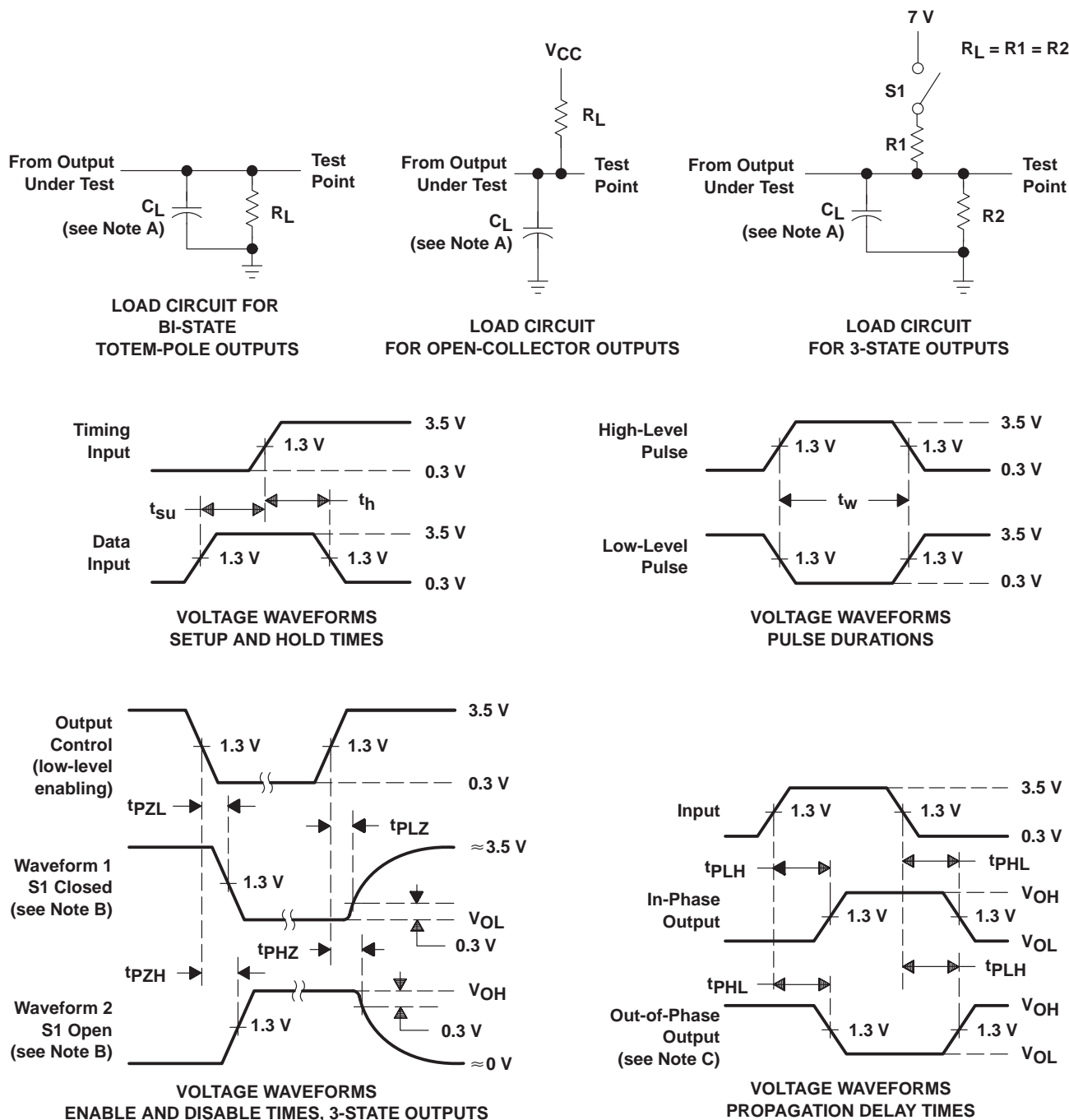
\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869  
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 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

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PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89526013A	NRND	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89526013A SNJ54AS 869FK	
5962-8952601KA	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8952601KA SNJ54AS869W	
5962-8952601LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8952601LA SNJ54AS869JT	<b>Samples</b>
5962-89668013A	NRND	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89668013A SNJ54AS 867FK	
5962-8966801KA	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8966801KA SNJ54AS867W	
5962-8966801LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT	<b>Samples</b>
SN54AS867JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS867JT	<b>Samples</b>
SN54AS869JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS869JT	<b>Samples</b>
SN74ALS867ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS867A	<b>Samples</b>
SN74ALS869DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869	<b>Samples</b>
SN74ALS869DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869	<b>Samples</b>
SN74AS867DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS867	<b>Samples</b>
SN74AS867DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS867	<b>Samples</b>
SN74AS867NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74AS869DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS869	<b>Samples</b>
SN74AS869NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SNJ54AS867FK	NRND	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										89668013A SNJ54AS 867FK	
SNJ54AS867JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT	Samples
SNJ54AS867W	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8966801KA SNJ54AS867W	
SNJ54AS869FK	NRND	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89526013A SNJ54AS 869FK	
SNJ54AS869JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8952601LA SNJ54AS869JT	Samples
SNJ54AS869W	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8952601KA SNJ54AS869W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AS867, SN54AS869, SN74AS867, SN74AS869 :**

- Catalog: [SN74AS867](#), [SN74AS869](#)
  
- Military: [SN54AS867](#), [SN54AS869](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Military - QML certified for Military and Defense Applications

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

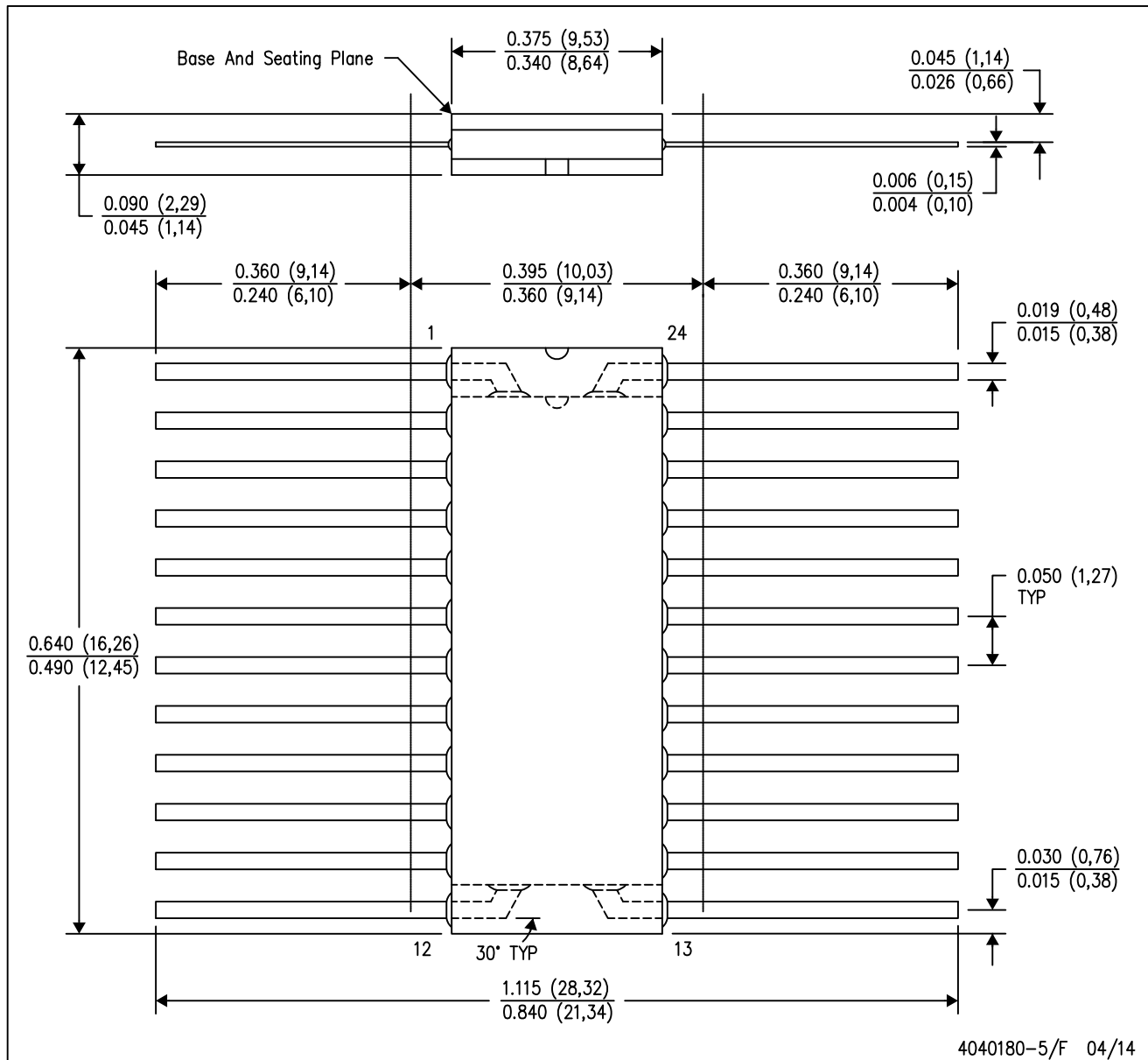
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



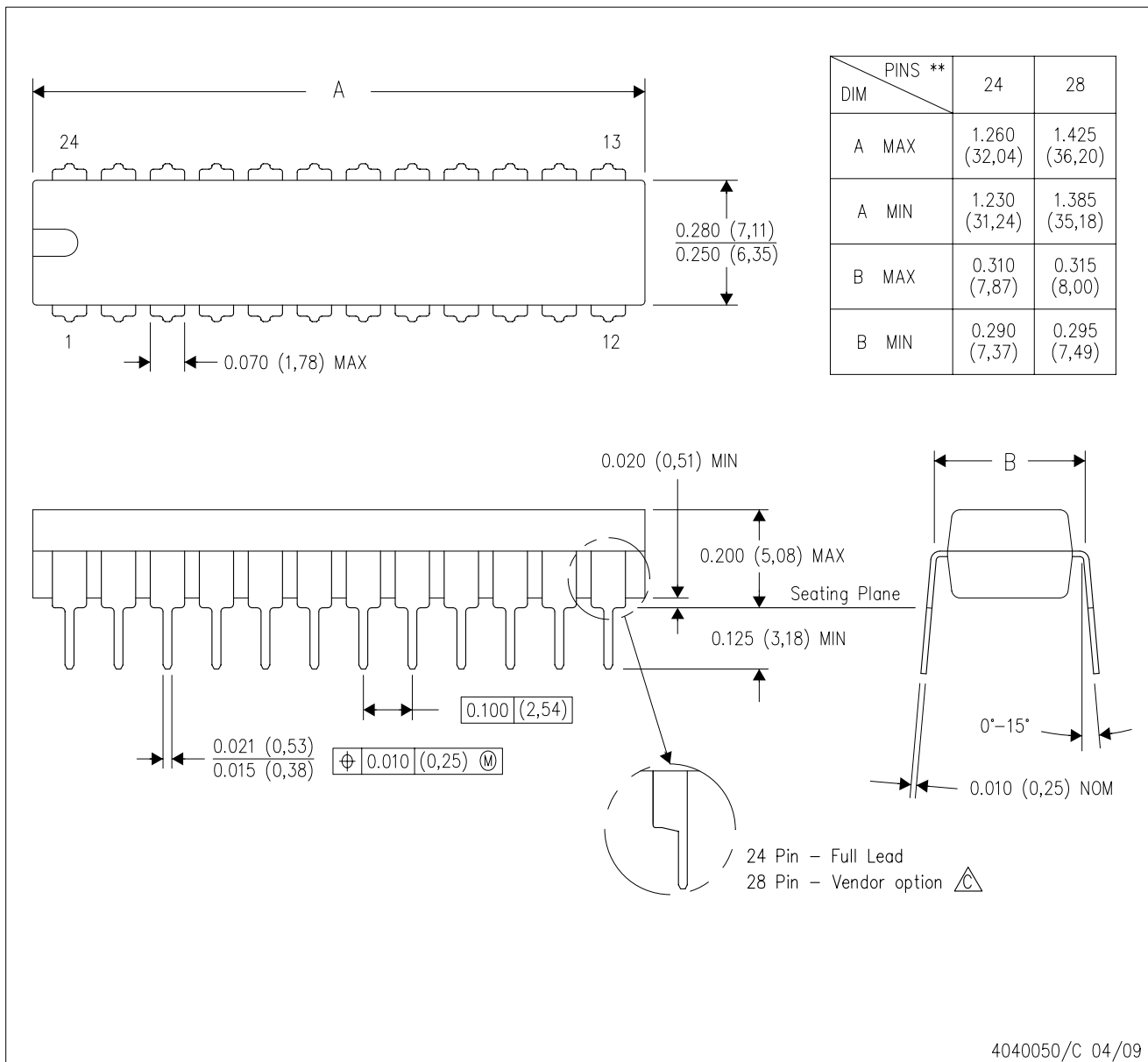
4040140/D 01/11


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.



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