FAIRCHILD SEMICONDUCTOR®

April 2013

DNP015
Green Mode Fairchild Power Switch (FPS™)

Features

mWSaver™ Technology

- Achieves Low No-Load Power Consumption: < 40 mW at 230 V_{AC} (EMI Filter Loss Included)
- Meets 2013 ErP Standby Power Regulation (< 0.5 W Consumption with 0.25 W Load) for ATX Power and LCD TV Power
- Eliminates X-Cap Discharge Resistor Loss with AX-CAP® Technology
- Linearly Decreased Switching Frequency at Light-Load Condition and Advanced Burst Mode Operation at No-Load Condition
- 700 V High-Voltage JFET Startup Circuit to Eliminate Startup Resistor Loss

Highly Integrated with Rich Features

- Internal Avalanche-Rugged 700 V SenseFET
- Built-in 5 ms Soft-Start
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Proprietary Asynchronous Jitter to Reduce EMI

Advanced Protection

- Internal Overload / Open-Loop Protection (OLP)
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Constant Power Limit (Full AC Input Range)
- Internal Latch Protection (OLP, V_{DD} OVP, OTP)
- Internal OTP Sensor with Hysteresis

Description

The DNP015 is a next-generation, Green Mode Fairchild Power Switch (FPS™) that incorporates Fairchild's innovative mWSaver™ technology, which dramatically reduces standby and no-load power consumption, enabling conformance to all worldwide Standby Mode efficiency guidelines. It integrates an advanced current-mode pulse width modulator (PWM) and an avalanche-rugged 700 V SenseFET in a single package, allowing auxiliary power designs with higher standby efficiency, reduced size, improved reliability, and lower system cost than prior solutions.

Fairchild Semiconductor's mWSaver™ technology offers best-in-class minimum no-load and light-load power consumption. An innovative Ax-CAP® method, one of the five proprietary mWSaver™ technologies, minimizes losses in the EMI filter stage by eliminating the X-cap discharge resistors while meeting IEC61010-1 safety requirements. mWSaver™ Green Mode gradually decreases switching frequency as load decreases to minimize switching losses.

Proprietary asynchronous jitter decreases EMI emission and built-in synchronized slope compensation allows stable peak-current-mode control over a wide range of input voltage. The proprietary internal line compensation ensures constant output power limit over the entire universal line voltage range.

Requiring a minimum number of external components, DNP015 provides a basic platform that is well suited for the cost-effective flyback converter design with low standby power consumption.

Applications

General-purpose switched-mode power supplies (SMPS) and flyback power converters, including:

- Auxiliary Power Supply for PC, Server, LCD TV, and Game Console
- SMPS for VCR, SVR, STB, DVD, and DVCD Player, Printer, Facsimile, and Scanner
- General Adapter
- LCD Monitor Power / Open-Frame SMPS

Ordering Information

Part Number	SenseFET	Operating Temperature Range	Package	Packing Method
DNP015	3 A / 700 V	-40°C to +105°C	8-Pin, Dual In-Line Package (DIP)	Tube

Application Diagram

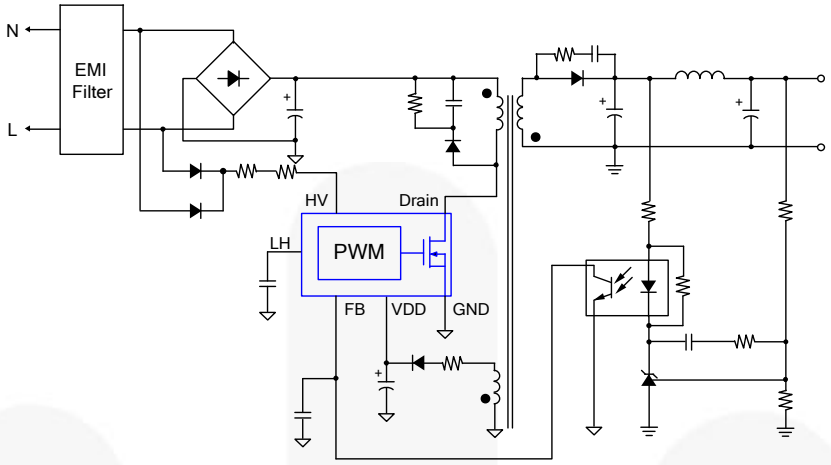


Figure 1. Typical Flyback Application

Output Power Table[1]

Product	230V$_{AC}$ ± 15%[2]		85-265V$_{AC}$	
	Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]
DNP015	17.5 W	25 W	13 W	19 W

Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100 / 115 V_{AC} with voltage doublers.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.

Block Diagram

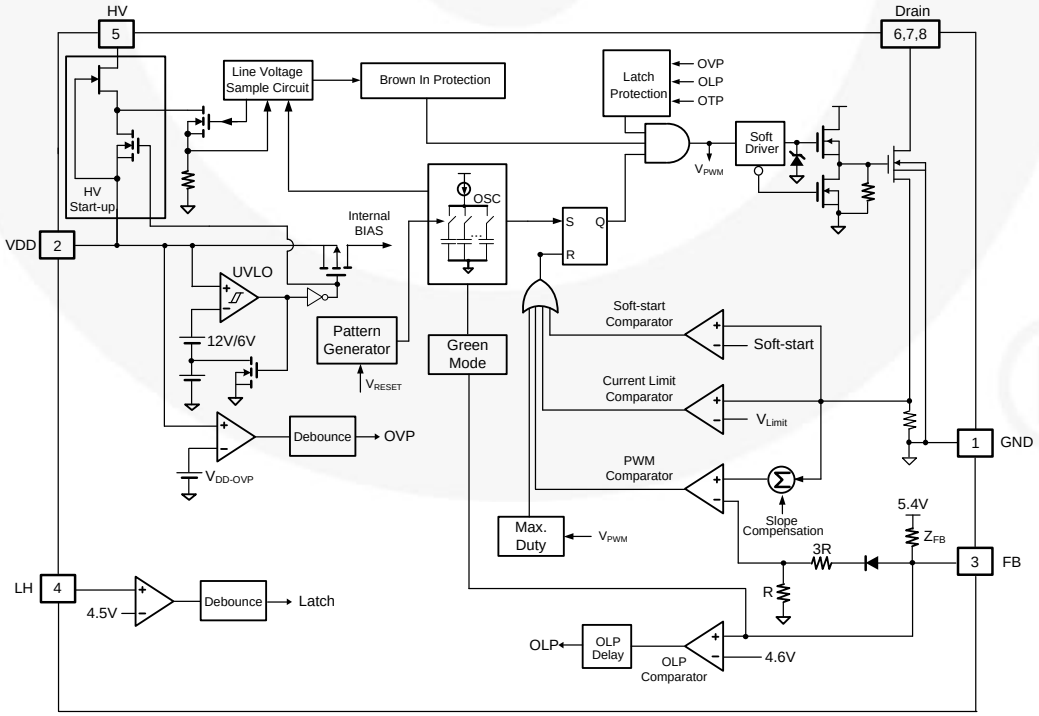
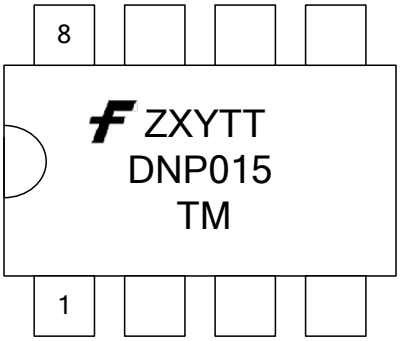


Figure 2. Internal Block Diagram

Pin Configuration



F – Fairchild logo
Z – Plant code
X – 1-digit year code
Y – 1-digit week code
TT – 2-digit die run code
T – Package type (N:DIP)
M – Manufacture flow code

Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin internally connects to the SenseFET source and signal ground of the PWM controller.
2	VDD	**Supply Voltage of the IC**. The holdup capacitor typically connects from this pin to ground. A rectifier diode in series with the transformer auxiliary winding connects to this pin to supply bias during normal operation.
3	FB	**Feedback**. The signal from the external compensation circuit connects to this pin. The PWM duty cycle is determined by comparing the signal on this pin and the internal current-sense signal.
4	LH	**Latch**. This pin is utilized for pull-HIGH latch protection by the external circuit, depending on the application.
5	HV	**Startup**. Typically, resistors in series with diodes from the AC line connect to this pin to supply internal bias and to charge the external capacitor connected between the VDD pin and the GND pin during startup. This pin is also used to sense the line voltage for brown-in and to detect AC line disconnection.
6	Drain	**SenseFET Drain**. This pin is designed to directly drive the transformer.
7		
8		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DRAIN}	Drain Pin Voltage[5,6]			700	V
I_{DM}	Drain Current Pulsed[7]			12	A
E_{AS}	Single-Pulsed Avalanche Energy[8]			230	mJ
V_{DD}	DC Supply Voltage			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{LH}	LH Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			700	V
P_D	Power Dissipation ($T_A < 50°C$)			1.55	W
T_J	Operating Junction Temperature		-40	Internally Limited[9]	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Soldering Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin	Human Body Model: JESD22-A114	5.50		kV
		Charged Device Model: JESD22-C101	2.00		
	Electrostatic Discharge Capability, All Pins Including HV Pin	Human Body Model: JESD22-A114	3.00		
		Charged Device Model: JESD22-C101	1.25		

Notes:

5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
7. Repetitive rating: pulse width is limited by maximum junction temperature.
8. L = 51 mH, starting T_J = 25°C.
9. Internally limited by Over-Temperature Protection (OTP), *refer to T_{OTP}*.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
R_{HV}	Resistor Connected to HV Pin for Full Range Input Detection	150	250	kΩ

Thermal Resistance Table

Symbol	Parameter	Typ.	Unit
θ_{JA}	Junction-to-Air Thermal Resistance	81	°C/W
ψ_{JT}	Junction-to-Package Thermal Resistance[10]	25	°C/W

Note:

10. Measured on the package top surface.

Electrical Characteristics

V_{DD}=15 V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SenseFET Section[11]						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D=250 µA, T_J=25°C	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = 700 V, V_{GS} = 0 V			50	µA
		V_{DS} = 560 V, V_{GS} = 0 V, T_C = 125°C			200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[12]	V_{GS} = 10 V, I_D = 1 A		4.00	4.75	Ω
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		315	410	pF
C_{OSS}	Output Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		47	61	pF
C_{RSS}	Reverse Transfer Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		9.0	24.0	pF
$t_{d(on)}$	Turn-On Delay	V_{DS} = 350 V, I_D = 1.0 A		11.2	33.0	ns
t_r	Rise Time	V_{DS} = 350 V, I_D = 1.0 A		34	78	ns
$t_{d(off)}$	Turn-Off Delay	V_{DS} = 350 V, I_D = 1.0 A		28.2	67.0	ns
t_f	Fall Time	V_{DS} = 350 V, I_D = 1.0 A		32	74	ns
Control Section						
VDD Section						
V_{DD-ON}	UVLO Start Threshold Voltage		11	12	13	V
$V_{DD-OFF1}$	UVLO Stop Threshold Voltage		5	6	7	V
$V_{DD-OFF2}$	Threshold Voltage of VDD Pin for HV Device Turn-On at Latch Mode		8	9	10	V
V_{DD-LH}	Threshold Voltage on VDD Pin for Latch-Off Release Voltage		3.5	4.0	4.5	V
I_{DD-ST}	Startup Supply Current	V_{DD-ON} – 0.16 V			30	µA
I_{DD-OP1}	Operating Supply Current with Normal Switching Operation	V_{DD}=15 V, V_{FB}=3 V			3.6	mA
I_{DD-OP2}	Operating Supply Current without Switching Operation	V_{DD}=15 V, V_{FB}=1 V			1.6	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection[11]			28		V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time[11]			150		µs
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	HV=120 V_{DC}, V_{DD}=0 V with 10 µF	1.5		5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV=700 V, V_{DD}=$V_{DD-OFF1}$+1 V			10	µA
V_{AC-ON}	Brown-in Threshold Level (V_{DC})	DC Voltage Applied to HV Pin through 200 kΩ	102	110	118	V
$K_{DISCHARGE}$	X-Cap Discharge Threshold	R=200 kΩ to HV Pin	60			%
t_{AC-OFF}	AC-Off Debounce Time for HV Discharge Function[11]			160		ms

Continued on the following page…

Electrical Characteristics

V_{DD}=15 V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Oscillator Section						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
		Hopping Range	±4.0	±6.0	±8.0	
t_{HOP}	Hopping Period(11)			20		ms
f_{OSC-G}	Green-Mode Frequency		20	23	26	kHz
DCY_{MAX}	Maximum Duty Cycle		80			%
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11 V to 22 V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation(11)	T_A=-40 to 105°C			5	%
Feedback Input Section						
A_V	Internal Voltage Dividing Factor of FB Pin(11)		1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Pull-Up Impedance of FB Pin		24	29	34	kΩ
$V_{FB-OPEN}$	FB Pin Pull-Up Voltage	FB Pin Open	5.2	5.4	5.6	V
V_{FB-OLP}	FB Voltage Threshold to Trigger Open-Loop Protection		4.3	4.6	4.9	V
t_{D-OLP}	Delay of FB Pin Open-Loop Protection		46	56	66	ms
V_{FB-N}	FB Voltage Threshold to Exit Green Mode	V_{FB} Rising	2.4	2.6	2.8	V
V_{FB-G}	FB Voltage Threshold to Enter Green Mode	V_{FB} Falling		V_{FB-N} - 0.1		V
V_{FB-ZDC}	FB Voltage Threshold to Enter Zero-Duty State	V_{FB} Falling	2.0	2.1	2.2	V
$V_{FB-ZDCR}$	FB Voltage Threshold to Exit Zero-Duty State	V_{FB} Rising		V_{FB-ZDC} + 0.1		V
LH Pin Section						
V_{LATCH}	Latch Comparator Reference Voltage		4.1	4.4	4.7	V
t_{LATCH}	Latch Mode Debounce Time				35	µs
$V_{LH-OPEN}$	LH Pin Open Voltage		3.0	3.5	4.0	V
Current-Sense Section(13)						
I_{LMT-FL}	Flat Threshold Level of Current Limit	Duty>40%	0.85	1.00	1.15	A
I_{LMT-VA}	Valley Threshold Level of Current Limit(11)	Duty=0%		I_{LMT-FL} - 0.2		A
t_{PD}	Current Limit Turn-Off Delay			100	200	ns
t_{LEB}	Leading-Edge Blanking Time		230	280	330	ns
t_{SS}	Soft-Start Time(11)			5		ms
Over-Temperature Protection Section (OTP)						
T_{OTP}	Junction Temperature Trigger OTP(11,14)			135		°C
ΔT_{OTP}	Hysteresis of OTP(11,15)			T_{OTP}-25		°C

Notes:

11. Guaranteed by design; not 100% tested in production.
12. Pulse test: pulse width ≤ 300 µs, duty ≤ 2%.
13. These parameters, although guaranteed, are tested in wafer-sort process.
14. When activated, the output is disabled and enters latch protection.
15. The threshold temperature for enabling the output again and resetting the latch after over-temperature protection has been activated.

Typical Characteristics

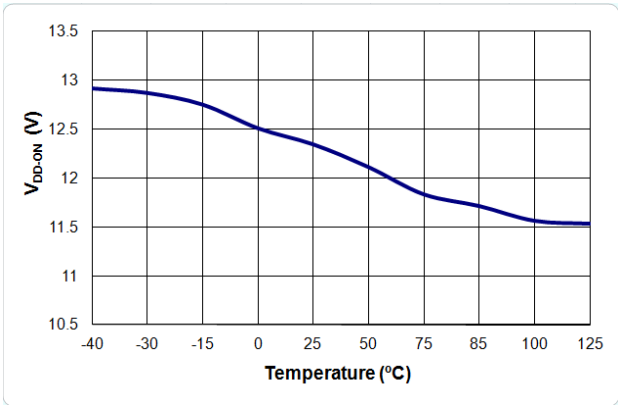


Figure 4. V_{DD-ON} vs. Temperature

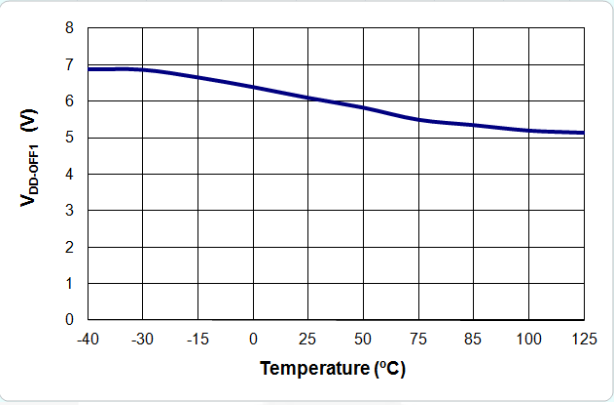


Figure 5. $V_{DD-OFF1}$ vs. Temperature

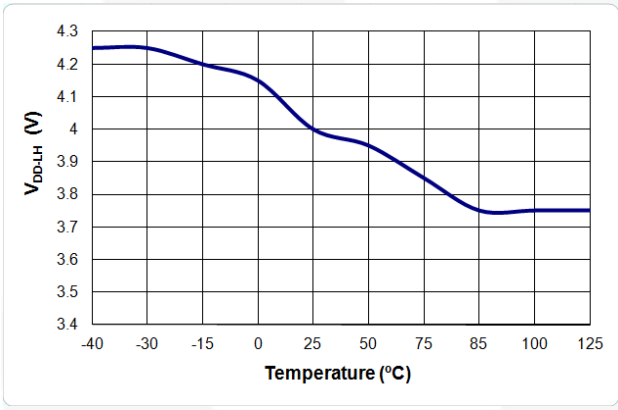


Figure 6. V_{DD-LH} vs. Temperature

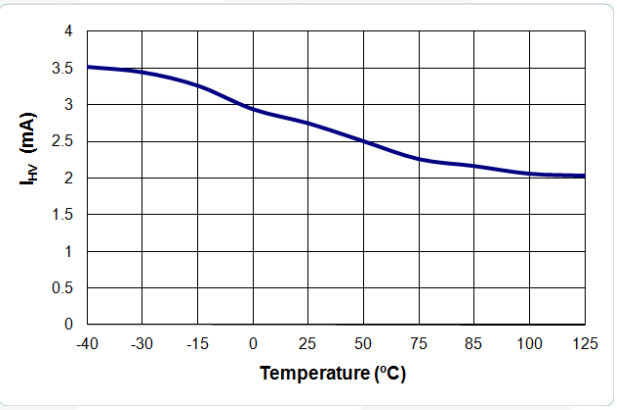


Figure 7. I_{HV} vs. Temperature

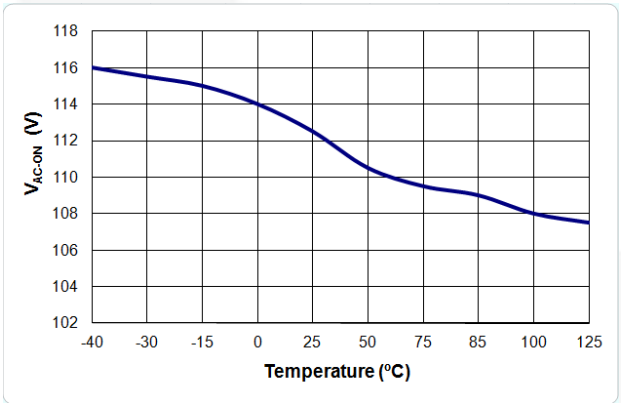


Figure 8. V_{AC-ON} vs. Temperature

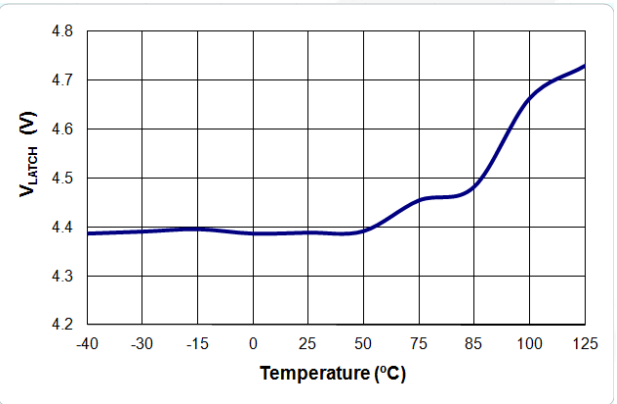


Figure 9. V_{LATCH} vs. Temperature

Typical Characteristics

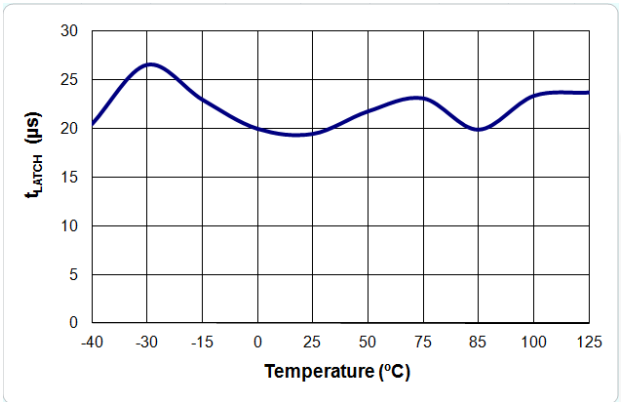


Figure 10. t_{LATCH} vs. Temperature

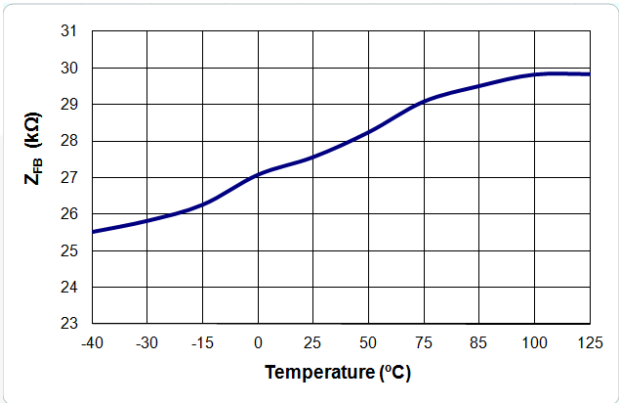


Figure 11. Z_{FB} vs. Temperature

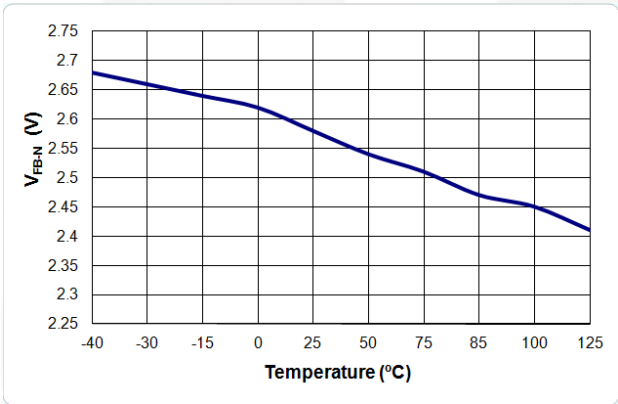


Figure 12. V_{FB-N} vs. Temperature

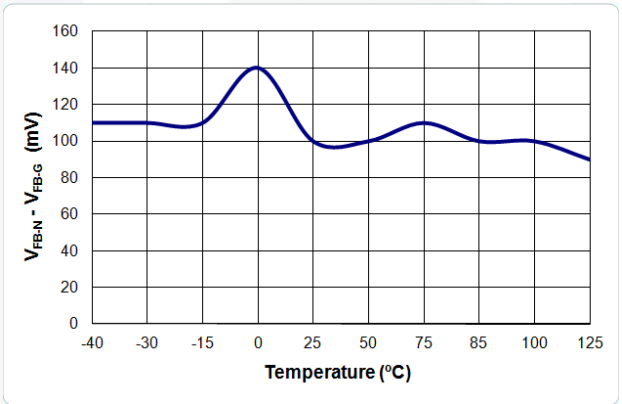


Figure 13. V_{FB-N} - V_{FB-G} vs. Temperature

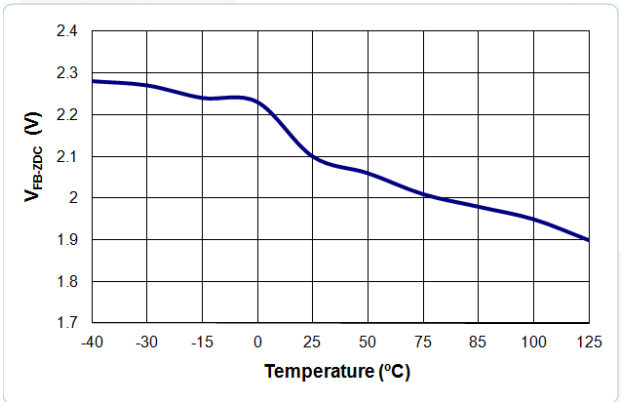


Figure 14. V_{FB-ZDC} vs. Temperature

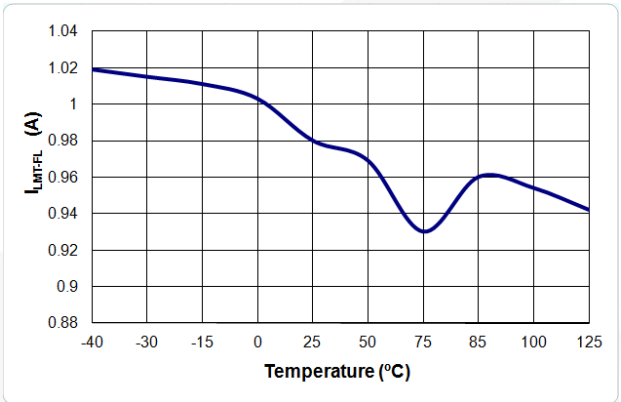


Figure 15. I_{LMT-FL} vs. Temperature

Functional Description

Startup Operation

The HV pin is typically connected to the AC line input through two external diodes and one resistor (R_{HV}), as shown in Figure 16. When the AC line voltage is applied, the V_{DD} hold-up capacitor is charged by the line voltage through the diodes and resistor. After V_{DD} voltage reaches the turn-on threshold voltage (V_{DD-ON}), the startup circuit charging the V_{DD} capacitor is switched off and V_{DD} is supplied by the auxiliary winding of the transformer. Once the DNP015 starts, it continues operation until V_{DD} drops below 6 V ($V_{DD-OFF1}$). The IC startup time with a given AC line input voltage is:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi} - V_{DD-ON}} \quad (1)$$

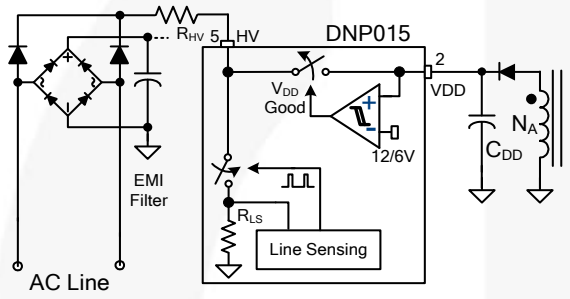


Figure 16. Startup Circuit

Brown-in Function

The HV pin can detect the AC line voltage using a switched voltage divider that consists of external resistor (R_{HV}) and internal resistor (R_{LS}), as shown in Figure 16. The internal line-sensing circuit detects the real RMS value of the line voltage using a sampling circuit and peak-detection circuit. Because the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize power consumption in light-load condition.

Based on the detected line voltage, brown-in threshold is determined. Since the internal resistor (R_{LS}) of the voltage divider is much smaller than R_{HV}, the thresholds are given as:

$$V_{BROWN-IN}(RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-ON}}{\sqrt{2}} \quad (2)$$

PWM Control

The DNP015 employs current-mode control, as shown in Figure 17. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. A synchronized positive slope is added to the SenseFET current information to guarantee stable current-mode control over a wide range of input voltage. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

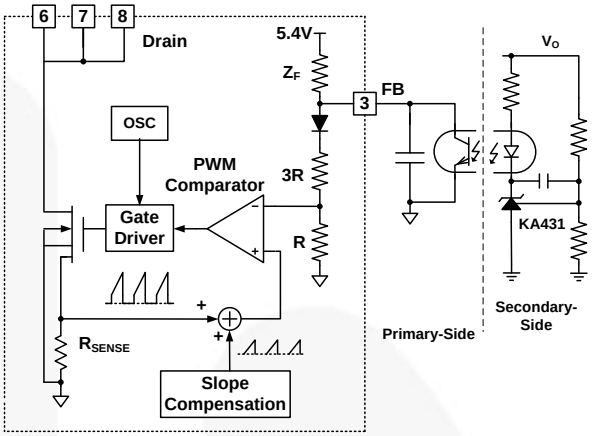


Figure 17. Current Mode Control

Soft-Start

The internal soft-start circuit progressively increases the pulse-by-pulse current-limit level of the MOSFET during startup to establish the correct working conditions for transformers and capacitors, as shown in Figure 18. The current limit levels have nine steps, as shown in Figure 19. This prevents transformer saturation and reduces stress on the secondary diode during startup.

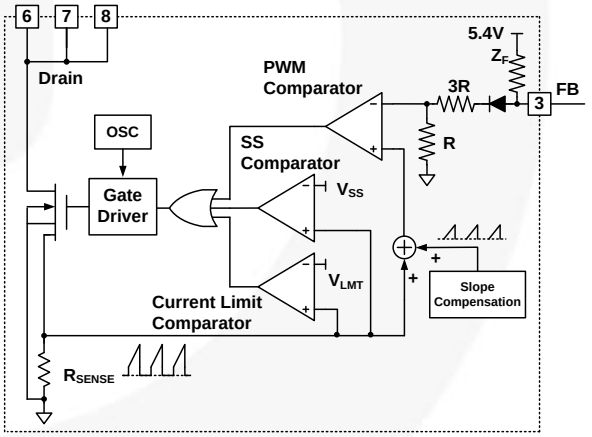


Figure 18. Soft-Start and Current-Limit Circuit

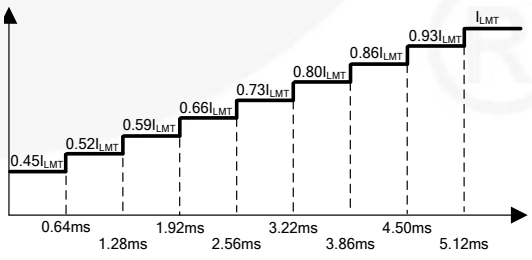


Figure 19. Current Limit Variation During Soft-Start

H/L Line Compensation for Constant Power Limit

To maintain constant limited output power, regardless of the line voltage condition, a special current-limit profile with sample-and-hold is used (as shown in Figure 20). The current-limit level is sampled and held at the falling edge of the gate drive signal, as shown in Figure 21. Then the sampled current-limit level is used for the next switching cycle. The sample-and-hold function prevents sub-harmonic oscillation in current-mode control.

The current-limit level increases as the duty cycle increases, which reduces the current limit as duty cycle decreases. This allows a lower current-limit level for high-line voltage condition where the duty cycle is smaller than that of low line. Therefore, the limited maximum output power can remain constant even for a wide input voltage range.

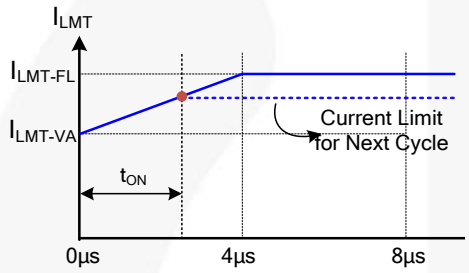


Figure 20. I_{LMT} vs. PWM Turn-On Time

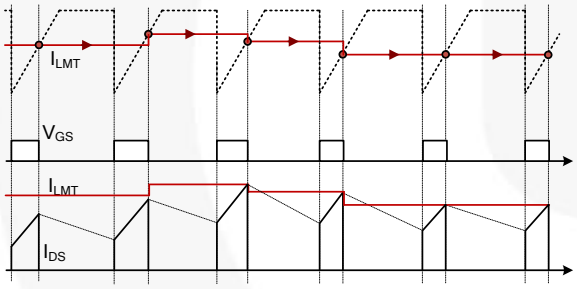


Figure 21. Current Limit Variation with Duty Cycle

mWSaver™ Technology

AX-CAP® Elimination of X-Cap Discharge Resistors

The EMI filter in the front end of the switched-mode power supply (SMPS) typically includes a capacitor across the AC line connector, as shown in Figure 22. Most of the safety regulations, such as UL1950 and IEC61010-1, require the capacitor be discharged to a safe level within a given time after being unplugged from the power outlet. Typically, a discharge resistor across the capacitor is used to ensure the capacitor is discharged naturally, which introduces power loss. As power level increases, the EMI filter capacitor tends to increase, requiring a smaller discharge resistor to maintain the same discharge time. This typically results in more power dissipation in high-power applications. The innovative AX-CAP technology intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the AX-CAP® discharge circuit is disabled during normal operation, the power loss in the EMI filter can be virtually removed.

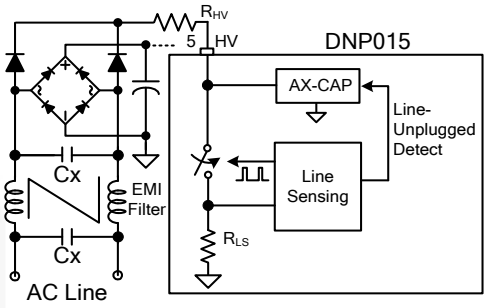


Figure 22. AX-CAP® Circuit

Green Mode

The DNP015 modulates the PWM frequency as a function of FB voltage, as shown in Figure 23. Since the output power is proportional to the FB voltage in current-mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 100 kHz. Once V_{FB} decreases below V_{FB-N} (2.6 V), the PWM frequency linearly decreases from 100 kHz to 23 kHz to reduce switching losses at light-load condition. As V_{FB} decreases to V_{FB-G} (2.5 V), the switching frequency is fixed at 23 kHz.

As V_{FB} falls below V_{FB-ZDC} (2.1 V), the DNP015 enters Burst Mode, where PWM switching is disabled. Then the output voltage starts to drop, causing the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$, switching resumes. Burst Mode alternately enables and disables switching, reducing switching loss to reduce power consumption, as shown in Figure 24.

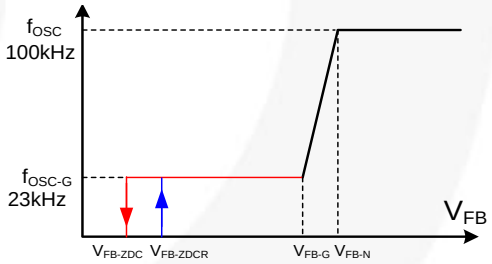


Figure 23. PWM Frequency

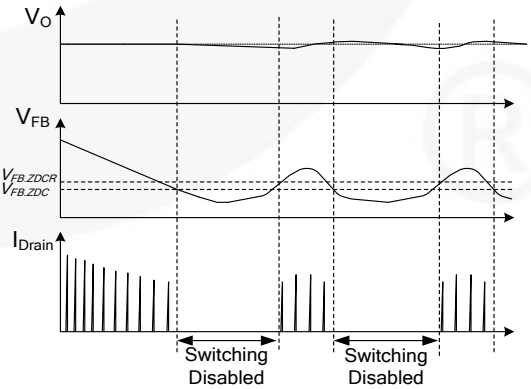


Figure 24. Burst-Mode Operation

Protections

Protection functions include Overload / Open-Loop Protection (OLP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP). All the protections are implemented as Latch Mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{DD} to fall and "hiccup" between 9 V and 12 V. As long as AC input is unplugged; V_{DD} falls to 4 V, the latch can be released, and the HV startup circuit charges V_{DD} up to 12 V voltage; allowing restart.

Open-Loop / Overload Protection (OLP)

Because of the pulse-by-pulse current-limit capability, the maximum peak current through the SenseFET is limited and maximum input power is limited. If the output consumes more than the limited maximum power, the output voltage (V_O) drops below the set voltage. Then the current through the opto-coupler LED and the transistor become virtually zero and FB voltage is pulled HIGH, as shown in Figure 25. If feedback voltage is above 4.6 V for longer than 56 ms, OLP is triggered.

This protection is also triggered when the feedback loop is open due to a soldering defect.

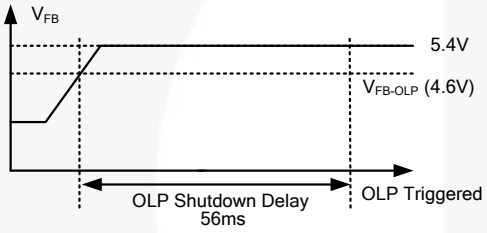


Figure 25. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes virtually zero. Then feedback voltage climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. Since V_{DD} voltage is proportional to the output voltage by the transformer coupling, the over voltage of output is indirectly detected using V_{DD} voltage. The OVP is triggered when V_{DD} voltage reaches 28 V. Debounce time (typically 150 µs) is applied to prevent false triggering by switching noise.

Over-Temperature Protection (OTP)

The SenseFET and the control IC are integrated in one package. This makes it easier for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds approximately 135°C, the OTP is triggered and the MOSFET remains off.

Physical Dimensions

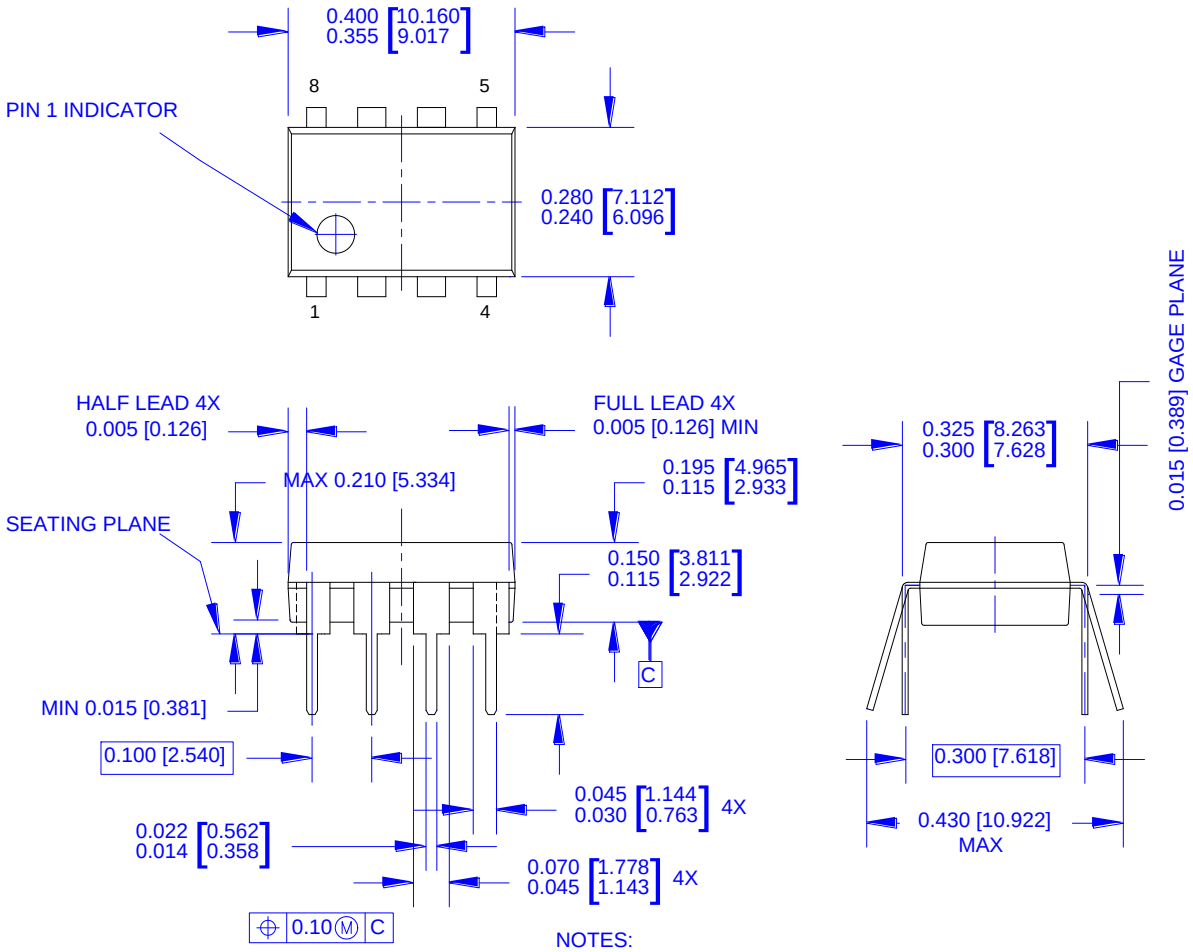


Figure 26. 8-pin Dual In-Line Package (DIP)

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