

## FEATURES/BENEFITS

- Pin and function compatible to the 74F821/3 74FCT821/3 and 74FCT821T/3T
- Industrial temperature  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- CMOS power levels:  $<7.5\text{mW}$  static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

### FCT 821T, 823T

- JEDEC-FCT spec compatible
- $I_{OL} = 48\text{mA}$  Ind.,  $32\text{mA}$  Mil.

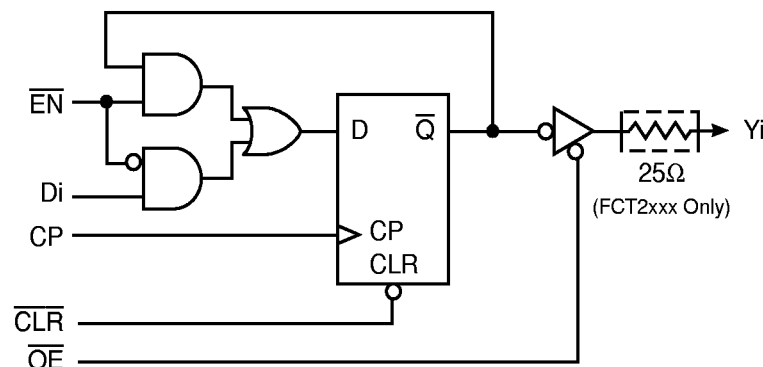
### FCT 2821T, 2823T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- $I_{OL} = 12\text{mA}$  Ind.

## DESCRIPTION

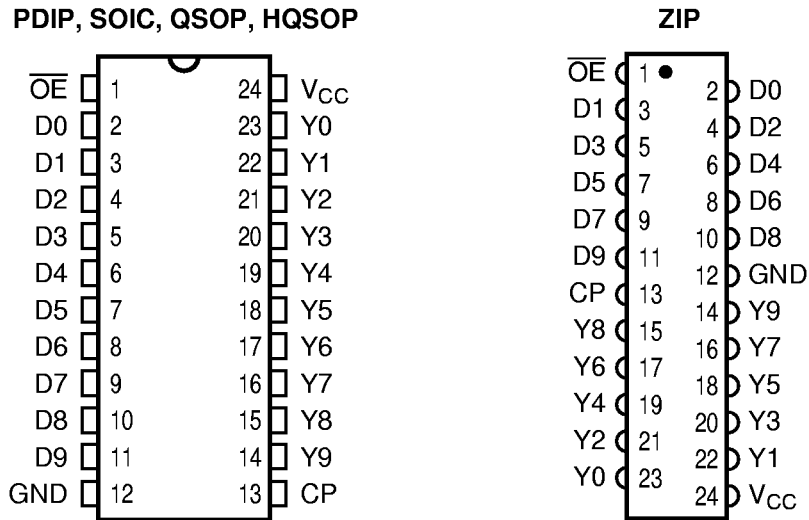
The QSFCT821T/823T and QSFCT2821T/2823T are 10- and 9-bit high-speed CMOS TTL-compatible buffered registers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2821/3 devices are  $25\Omega$  resistor output versions useful for driving transmission lines and reducing system noise. The 2821/3 series parts can replace the 821/3 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

**Figure 1. Functional Block Diagram**



**FCT821/2821 - 10-BIT REGISTER**

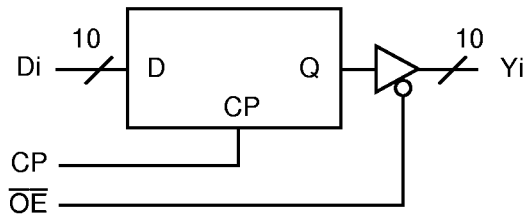
**Figure 2. Pin Configurations (All Pins Top View)**



**Table 1. Pin Description**

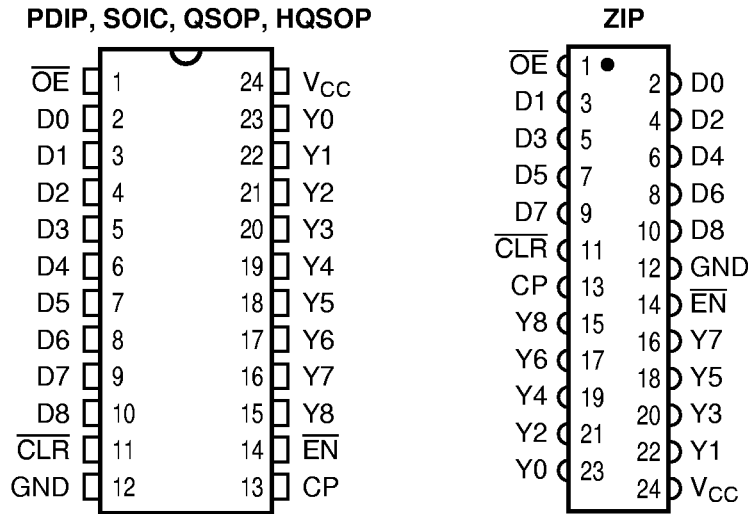
Name	I/O	Description
D <sub>i</sub>	I	Data Inputs
Y <sub>i</sub>	O	Data Outputs-Three State
CP	I	Clock Pulse
$\overline{OE}$	I	Output Enable

**Figure 3. FCT821 Logic Symbol**



**FCT823/2823 - 9-BIT REGISTER**

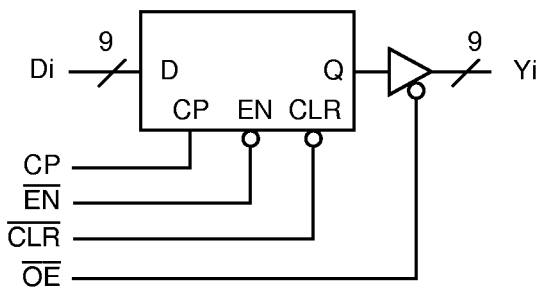
**Figure 4. Pin Configurations (All Pins Top View)**



**Table 2. Pin Description**

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
$\overline{OE}$	I	Output Enable
CP	I	Clock Pulse
$\overline{EN}$	I	Clock Enable
$\overline{CLR}$	I	Asynchronous Reset

**Figure 5. FCT823 Logic Symbol**



**Table 3. Function Table**

Inputs					Int.	O/P	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	Di	CP	Qi	Yi	
H	X	L	L	↑	L	Hi-Z	High Z
H	X	L	H	↑	H	Hi-Z	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load

**Note:** For the 821, the HI-Z and Load functions only apply as the  $\overline{EN}$  and  $\overline{CLR}$  are not present in these devices.

**Table 4. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to 7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**Table 5. Capacitance<sup>(1)</sup>**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins <sup>(2)</sup>	SOIC	QSOP	PDIP	ZIP	Unit
1, 3-11, 13	4	4	5	7	pF
15-22	6	6	7	9	pF
2, 14, 23	8	8	9	10	pF

**Notes:**

1. Capacitance is characterized but not tested.
2. Pin reference for 24-pin package.

**Table 6. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , freq = 0 $0V \leq V_{IN} \leq 0.2V$ or $V_{CC}-0.2V \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4V$ , freq = 0 <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4V$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**Table 7. DC Electrical Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0V \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}$ , $0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$ , $0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}$ , $V_{OUT} = \text{GND}$ <sup>(2,3)</sup>	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2XXX)	$V_{CC} = \text{Min.}$ , $V_{OUT} = 2.0V$ <sup>(3)</sup>	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}$ , $I_{IN} = -18\text{mA}$ , $T_A = 25^\circ\text{C}$ <sup>(3)</sup>	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -15\text{mA}$ (MIL) $I_{OH} = -24\text{mA}$ (IND)	2.4 2.4	—	—	V
$V_{OL}$	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}$ $I_{OL} = 32\text{mA}$ (MIL) $I_{OL} = 48\text{mA}$ (IND)	— —	—	0.50 0.50	V
$V_{OL}$	Output LOW Voltage (FCT2XXX- 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— —	—	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2XXX- 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0V$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**QS54/74FCT821T, 823T, 2821T, 2823T**

**Table 8. Switching Characteristics Over Operating Range**

Industrial  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$       Military  $T_A = -55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$   
 $C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		821A 823A 2821A 2823A		821B 823B 2821B 2823B		821C 823C		821D 823D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PHL}$ $t_{PLH}$	Clock to Y Delay $\overline{OE} = \text{LOW}$ , 821/3	Ind Mil	— —	10 11.5	— —	7.5 8.5	— —	6.0 7.0	— —	5.3 —	ns
$t_{PHL}$ $t_{PLH}$	Clock to Y Delay <sup>(2,3)</sup> $\overline{OE} = \text{LOW}$ , 821/3	Ind Mil	— —	20 20	— —	15 16	— —	12.5 13.5	— —	12.5 —	ns
$t_{PHL}$ $t_{PLH}$	Clock to Y Delay $\overline{OE} = \text{LOW}$ , 2821/3	Ind Mil	— —	10 11.5	— —	7.5 8.5	— —	6.0 —	— —	5.3 —	ns
$t_{PHL}$ $t_{PLH}$	Clock to Y Delay <sup>(2,3)</sup> $\overline{OE} = \text{LOW}$ , 2821/3	Ind Mil	— —	20 20	— —	15 16	— —	12.5 —	— —	12.5 —	ns
$t_S$	Data to CP Setup Time	Ind Mil	4.0 4.0	— —	3.0 3.0	— —	3.0 3.0	— —	3.0 —	— —	ns
$t_H$	Data to CP Hold Time	Ind Mil	2.0 2.0	— —	1.5 1.5	— —	1.5 1.5	— —	1.5 —	— —	ns
$t_{ENS}$	$\overline{EN}$ to CP Setup Time	Ind Mil	4.0 4.0	— —	3.0 3.0	— —	3.0 3.0	— —	3.0 —	— —	ns
$t_{ENH}$	$\overline{EN}$ to CP Hold Time	Ind Mil	2.0 2.0	— —	0.0 0.0	— —	0.0 0.0	— —	0.0 —	— —	ns

**Notes:**

1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3.  $C_{LOAD} = 300\text{pF}$

**QS54/74FCT821T, 823T, 2821T, 2823T**

**Table 9. Timing Requirements Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		821A 823A 2821A 2823A		821B 823B 2821B 2823B		821C 823C		821D 823D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLR}$	$\overline{CLR}$ to Y Delay 823	Ind Mil	— —	11 12	— —	9.0 9.5	— —	8.0 8.5	— —	7.0 —	ns
$t_{CLR}$	$\overline{CLR}$ to Y Delay 2823	Ind Mil	— —	11 12	— —	9.0 9.5	— —	8.0 —	— —	7.0 —	ns
$t_{REC}$	$\overline{CLR}$ to CP Setup Time	Ind Mil	6.0 7.0	— —	6.0 6.0	— —	6.0 6.0	— —	6.0 —	— —	ns
$t_{PWH}$ $t_{PWL}$	Clock Pulse Width <sup>(2)</sup> HIGH or LOW	Ind Mil	7.0 7.0	— —	6.0 6.0	— —	6.0 6.0	— —	6.0 —	— —	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to Yi, 821/3	Ind Mil	— —	12 13	— —	8.0 9.0	— —	7.0 8.0	— —	6.5 —	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(2,3)</sup> $\overline{OE}$ to Yi, 821/3	Ind Mil	— —	23 25	— —	15 16	— —	12.5 13.5	— —	12.5 —	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to Yi, 2821/3	Ind Mil	— —	12 13	— —	8.0 9.0	— —	7.0 —	— —	6.5 —	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(2,3)</sup> $\overline{OE}$ to Yi, 2821/3	Ind Mil	— —	23 25	— —	— —	— —	— —	— —	— —	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2,4)</sup> $\overline{OE}$ to Yi	Ind Mil	— —	7.0 8.0	— —	6.5 7.0	— —	6.2 6.2	— —	6.2 —	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2)</sup> $\overline{OE}$ to Yi	Ind Mil	— —	9.0 10	— —	7.5 8.0	— —	6.5 6.5	— —	6.5 —	ns

**Notes:**

1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3.  $C_{LOAD} = 300\text{pF}$ .
4.  $C_{LOAD} = 5\text{pF}$ .