Octal D-Type Flip-Flop with 3-State Output

MC74VHCT574A

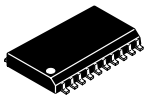
The MC74VHCT574A is an advanced high speed CMOS octal flip–flop with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

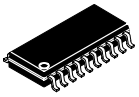
The VHCT574A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: f_{max} = 140MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–05

DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	No Change
H	X	X	Z

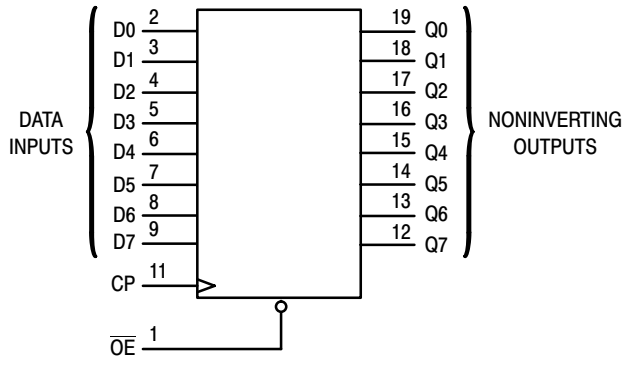


Figure 1. Logic Diagram

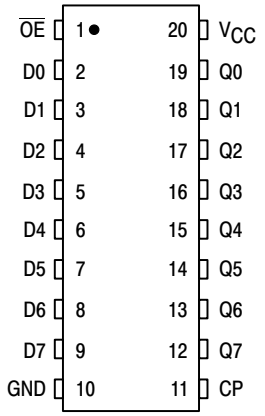


Figure 2. Pin Assignment

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF	90 85	140 130		80 95		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Q	V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		7.0	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance, Output in High–Impedance State			9				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	25	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = – 40 to 85°C	Unit
			Typ	Limit	Limit	
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 5.0 ± 0.5 V		6.5	8.5	ns
t_h	Minimum Hold Time, CP to D	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns
t_w	Minimum Pulse Width, CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns

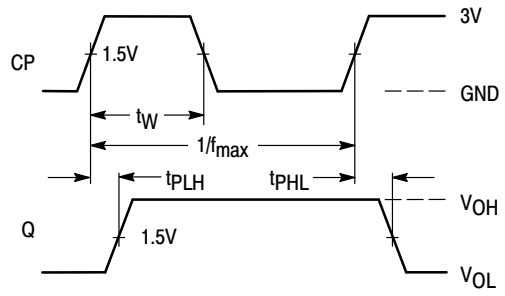


Figure 3. Switching Waveform

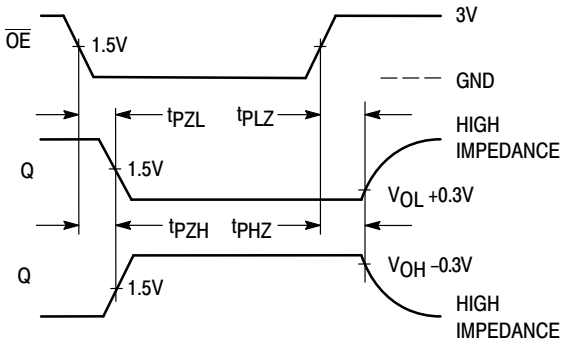


Figure 4. Switching Waveform

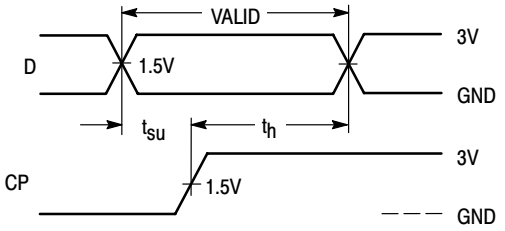
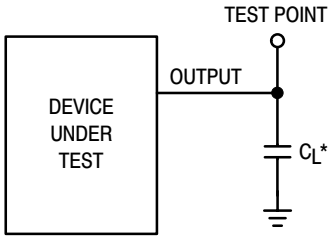
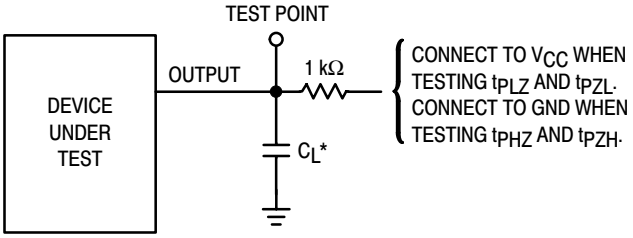


Figure 5. Switching Waveform



*Includes all probe and jig capacitance

Figure 6. Test Circuit



*Includes all probe and jig capacitance

Figure 7. Test Circuit

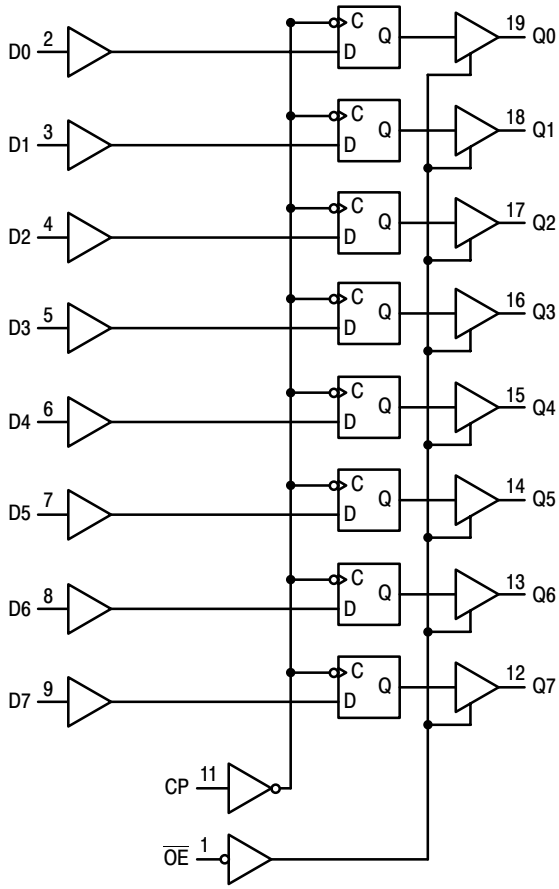


Figure 8. Expanded Logic Diagram