FAIRCHILD SEMICONDUCTOR®

June 2007

DM74ALS169B
Synchronous Four-Bit Up/Down Counters

Features

- Switching specifications at 50pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- ESD inputs

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The DM74ALS169B is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either HIGH or LOW. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be LOW to count. The direction of the count is determined by the level of the up/down input. When the input is HIGH, the counter counts UP; when LOW, it counts DOWN. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the Q_A output when counting UP, and approximately equal to the low portion of the Q_A when counting DOWN. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

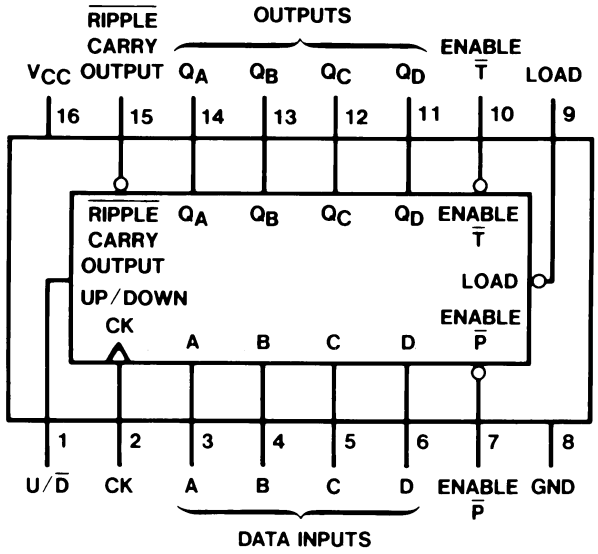
The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Ordering Information

Order Number	Package Number	Package Description
DM74ALS169BM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

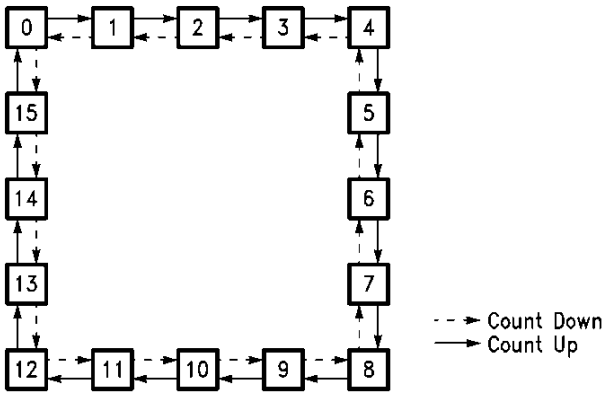
Connection Diagram



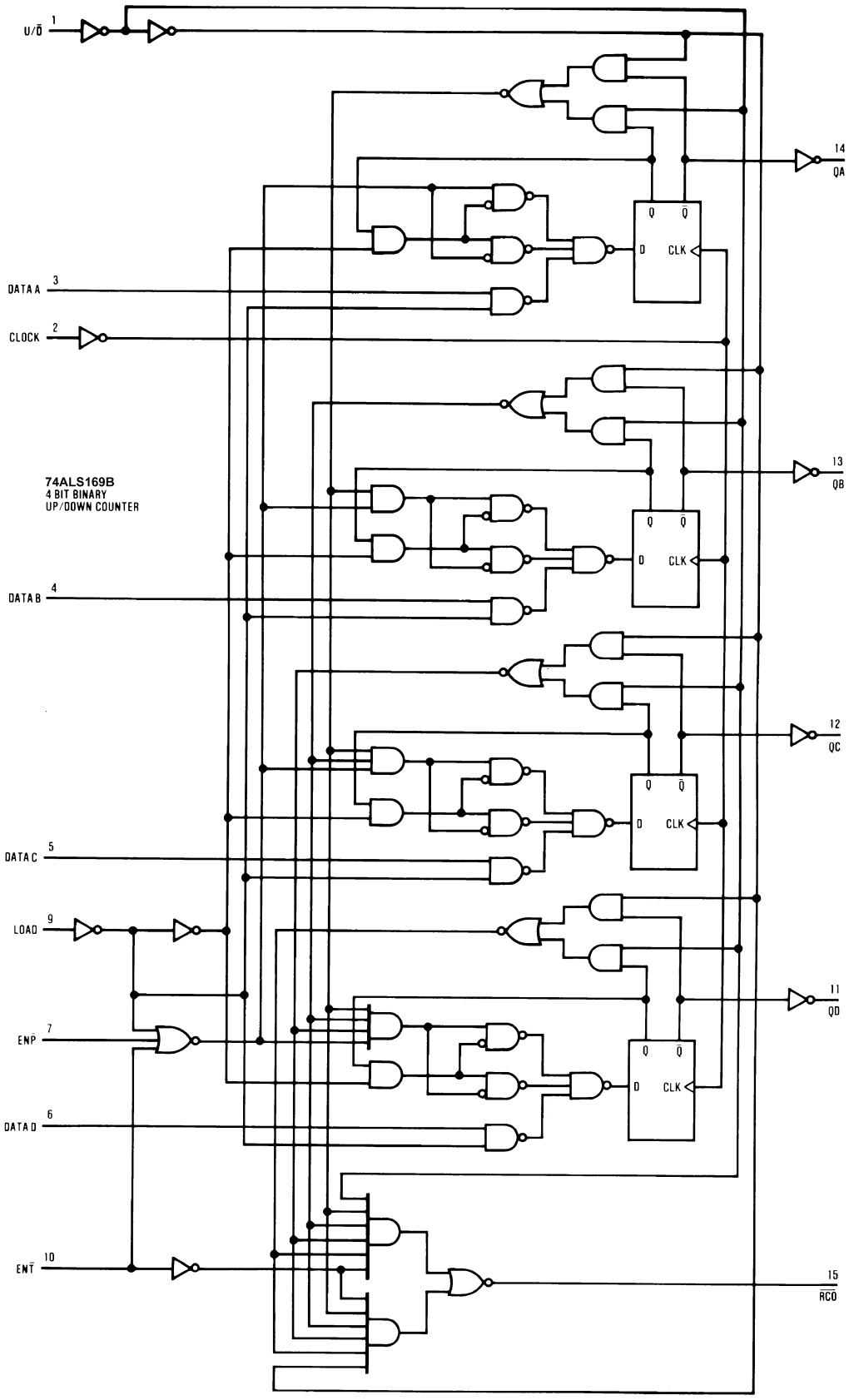
Mode Select Table

LOAD	$E\overline{P}$	$E\overline{T}$	$U/\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

State Diagram



Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	7V
V_I	Input Voltage	7V
T_A	Operating Free Air Temperature Range	0°C to +70°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
θ_{JA}	Typical Thermal Resistance	106.8°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				–0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency		0		40	MHz
t_{SU}	Setup Time(1)	Data: A, B, C, D	15↑	6		ns
		En $\overline{P}$, En $\overline{T}$	15↑	8		
		$\overline{Load}$	15↑	8		
		U/$\overline{D}$	15↑	10		
t_H	Hold Time(1)	Data: A, B, C, D	0↑	–3		ns
		En $\overline{P}$, En $\overline{T}$	0↑	–3		
		$\overline{Load}$	0↑	–4		
		U/$\overline{D}$	0↑	–4		
t_W	Width of Clock Pulse		13			ns

Note:

1. The symbol (↑) indicates that the rising edge of the clock is used as reference.

Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = –18mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –0.4mA, V_{CC} = 4.5V to 5.5V	V_{CC} – 2			V
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 8mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			–0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	–30		–112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V		15	25	mA

Switching Characteristics

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions	From	To	Min.	Max.	Units
f_{MAX}	Maximum Clock Frequency				40		MHz
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF	Clock	$\overline{\text{Ripple}}$ Carry	3	20	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	$\overline{\text{Ripple}}$ Carry	6	20	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		Clock	Any Q	2	15	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	Any Q	5	20	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		En T	$\overline{\text{Ripple}}$ Carry	2	13	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		En T	$\overline{\text{Ripple}}$ Carry	3	16	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		$U/\overline{D}$(2)	$\overline{\text{Ripple}}$ Carry	5	19	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		$U/\overline{D}$(2)	$\overline{\text{Ripple}}$ Carry	5	19	ns

Note:

2. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

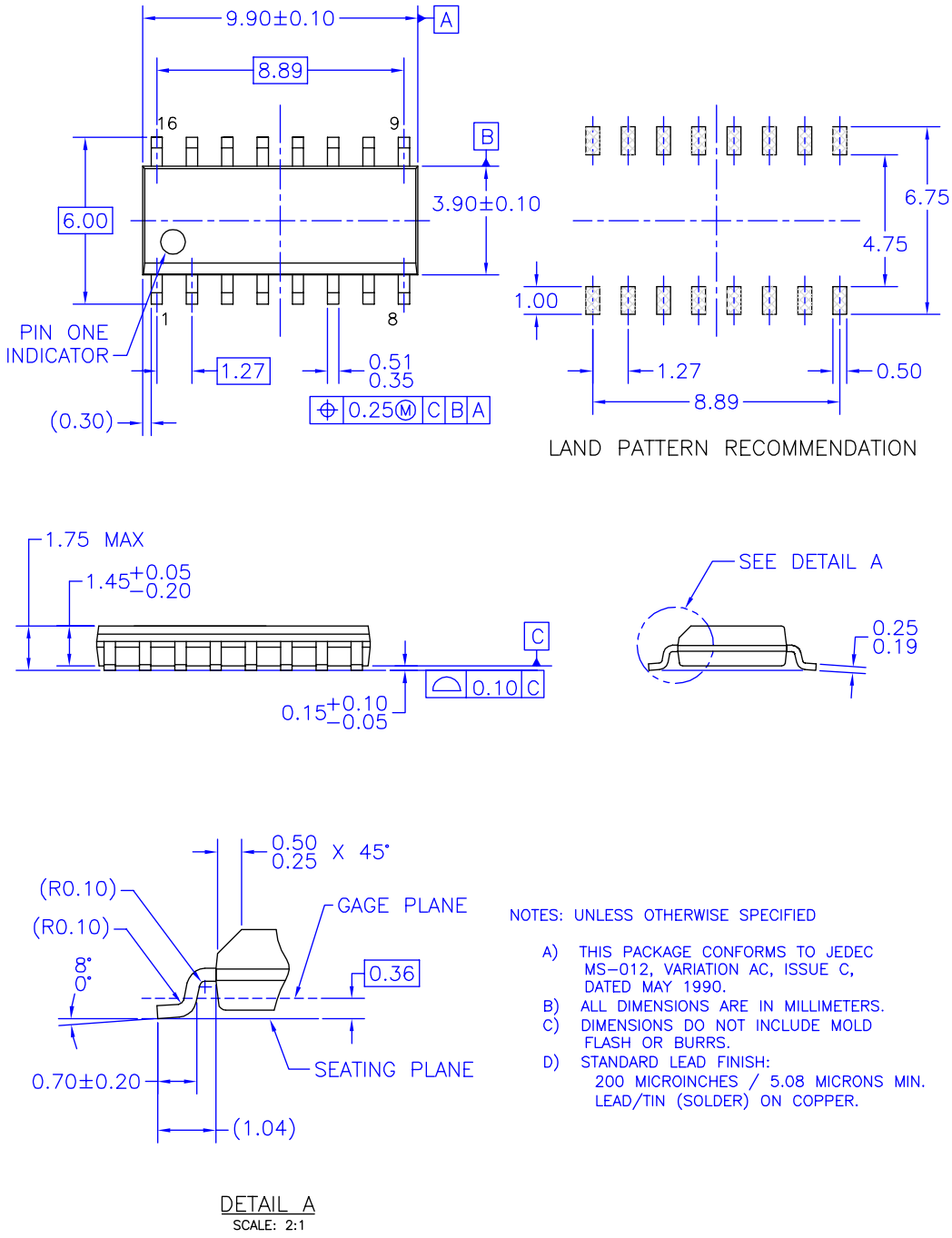


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

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