CY7C197N

256Kx1 Static RAM

Features

- **High speed**
  - **— 25 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 880 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C197N is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and three-state drivers. The CY7C197N has an automatic power-down feature, reducing the power consumption by 75% when deselected.

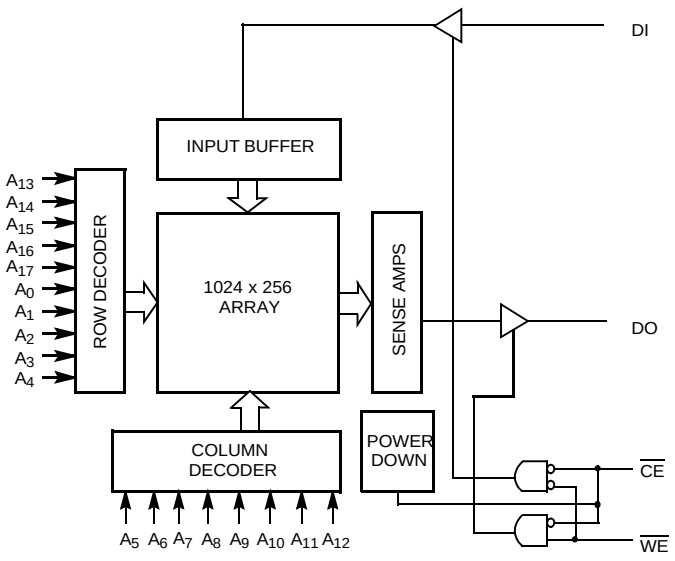
Writing to the device is accomplished when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when Chip Enable ($\overline{CE}$) is HIGH or Write Enable ($\overline{WE}$) is LOW.

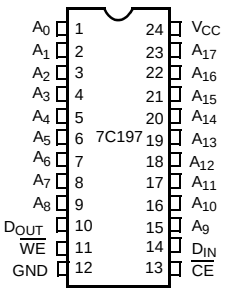
The CY7C197N utilizes a die coat to insure alpha immunity.

Logic Block Diagram



Pin Configurations

DIP
Top View



Selection Guide

	-25	-45
Maximum Access Time (ns)	25	45
Maximum Operating Current (mA)	95	
Maximum Standby Current (mA)	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

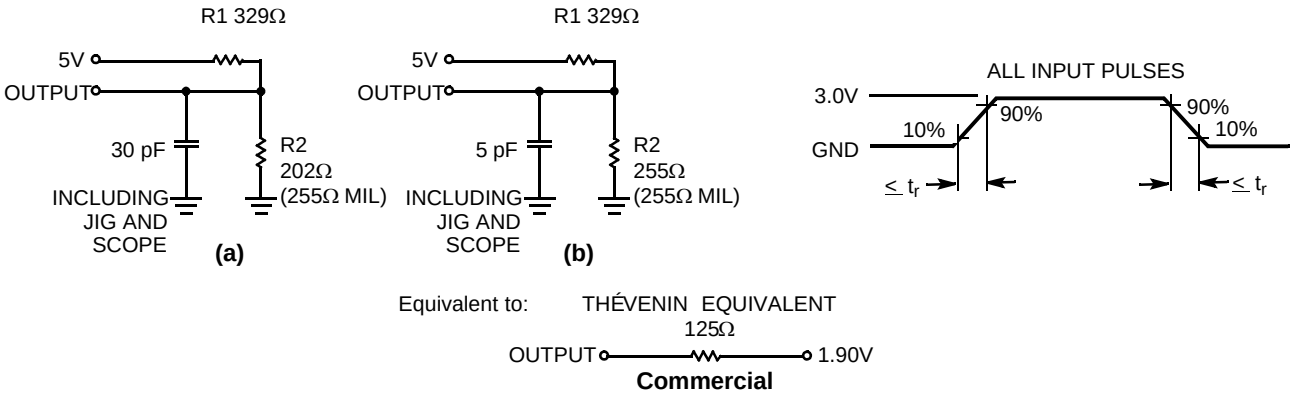
Parameter	Description	Test Conditions	-25, -45		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL}=12.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]		–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–5	+5	mA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–5	+5	mA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		95	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs[3]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[3]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} < 0.3V		15	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Note:
1. $V_{(min.)}$ = -2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested initially and after any design or process changes that may affect these parameters.
5. t_r = ≤ 5 ns for the -25 and slower speeds.

AC Test Loads and Waveforms[5]



Commercial

Switching Characteristics Over the Operating Range[8]

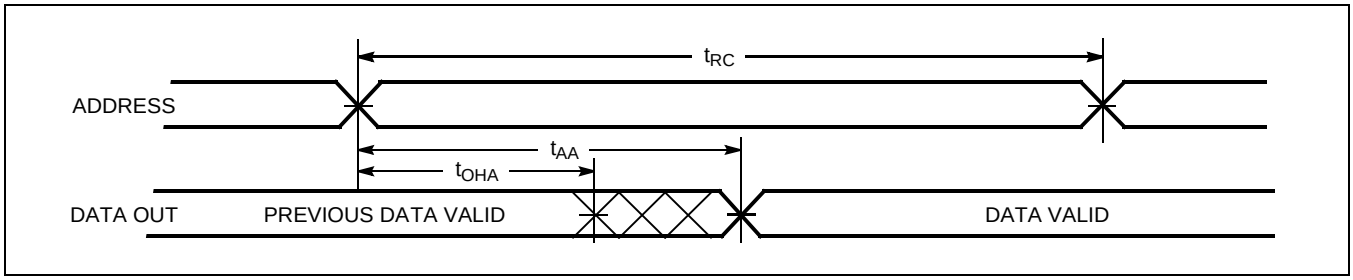
Parameter	Description	-25		-45		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		45		ns
t_{AA}	Address to Data Valid		25		45	ns
t_{OHA}	Output Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]	0	11	0	15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		30	ns
WRITE CYCLE[11]						
t_{WC}	Write Cycle Time	25		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		40		ns
t_{AW}	Address Set-Up to Write End	20		40		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		30		ns
t_{SD}	Data Set-Up to Write End	15		20		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]	0	11	0	15	ns

Note:

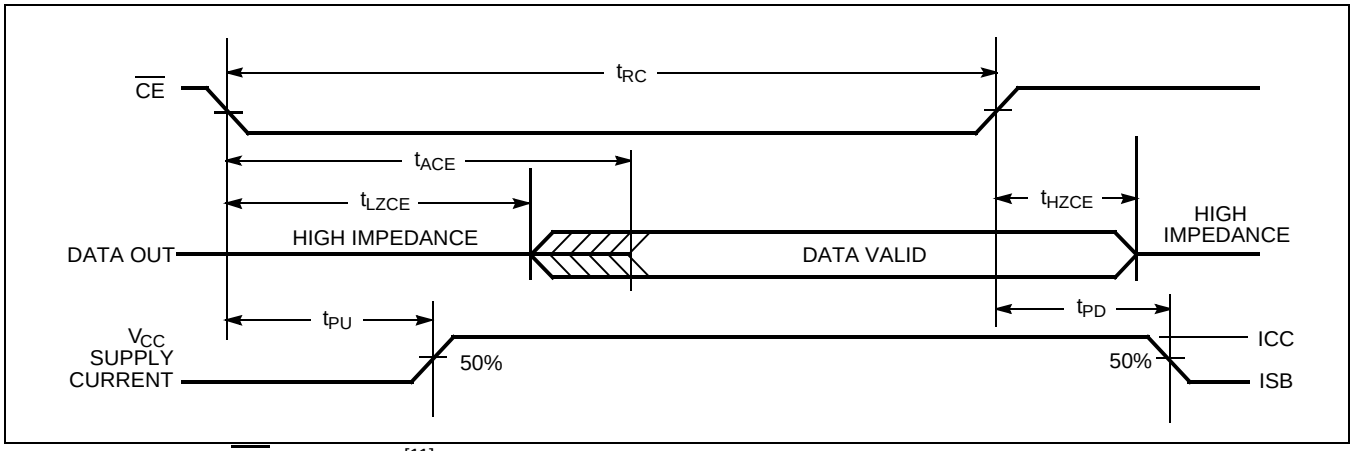
6. Tested initially and after any design or process changes that may affect these parameters.
7. $t_r = \leq 5$ ns for the -25 and slower speeds.
8. Test conditions assume signal transition time of 5 ns or less for -25 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

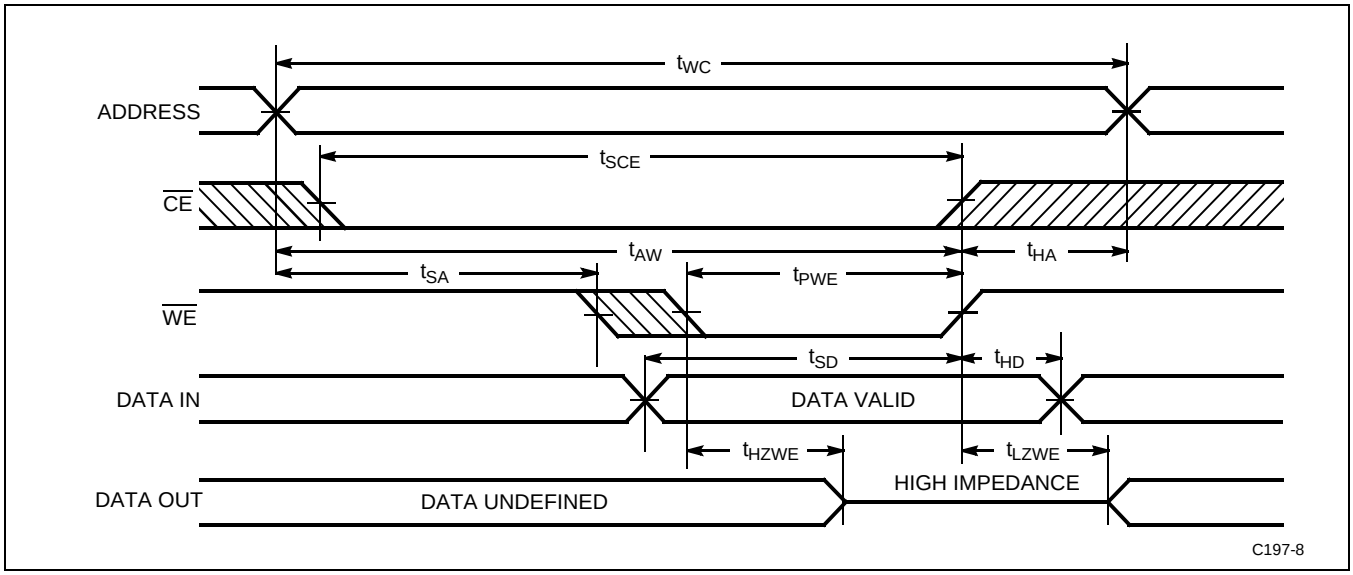
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12]



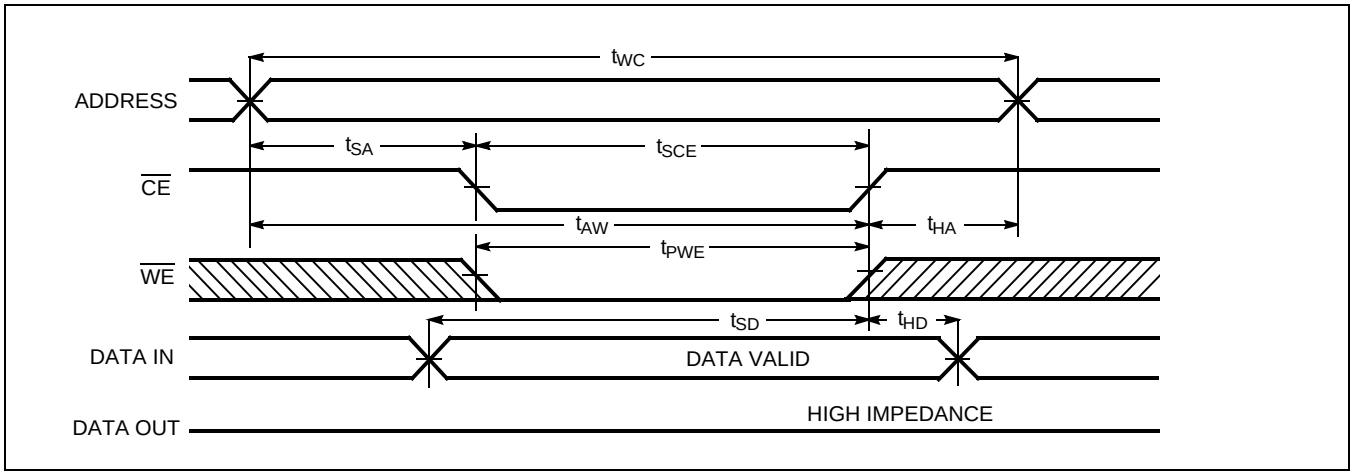
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



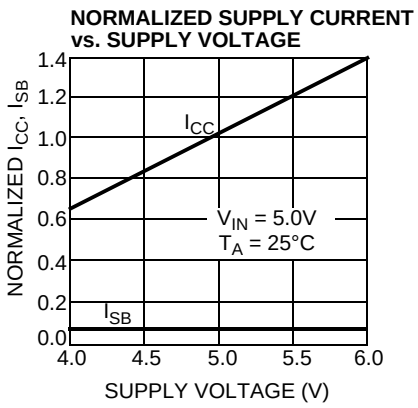
Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

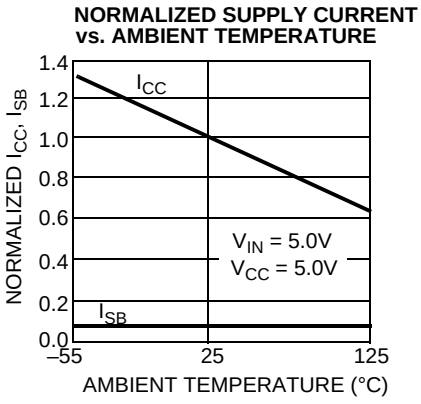
Switching Waveforms (continued)

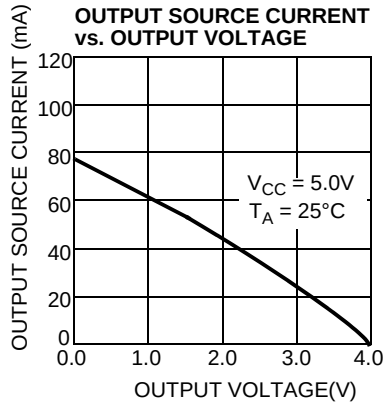
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 14]

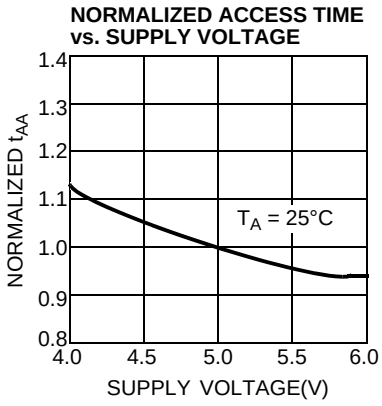


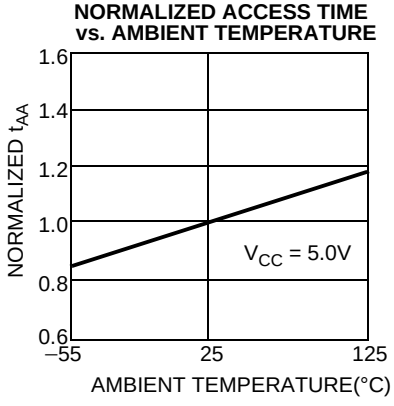
Typical DC and AC Characteristics

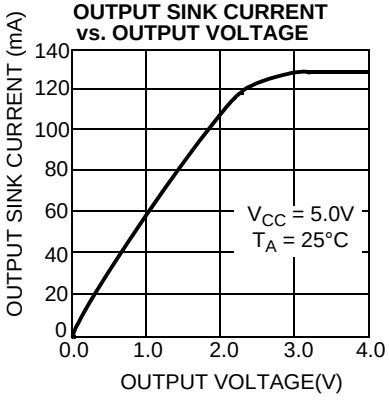




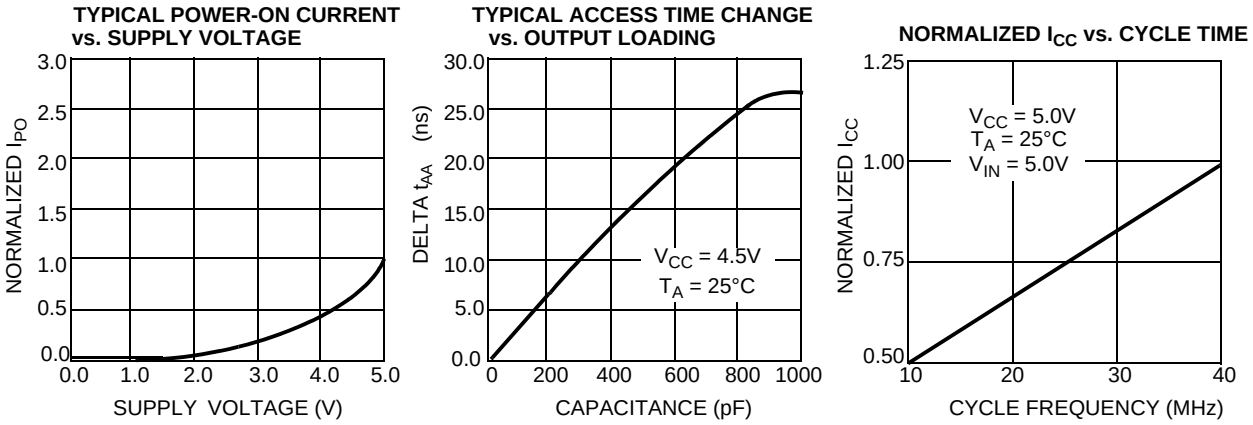








Typical DC and AC Characteristics (continued)



CY7C197N Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

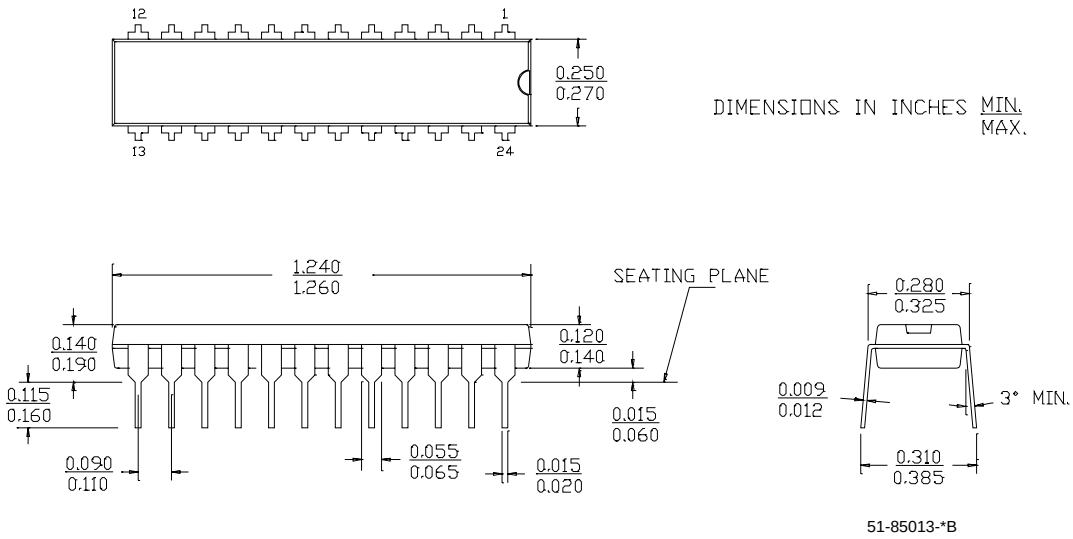
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY7C197N-25PXC	51-85013	24-Lead (300-Mil) Molded DIP (Pb-free)	Commercial
45	CY7C197N-45PXC	51-85013	24-Lead (300-Mil) Molded DIP (Pb-free)	Commercial

Please contact local sales representative regarding availability of these parts.

Package Diagram

24-Lead (300-Mil) PDIP (51-85013)



Document History Page

Document Title: CY7C197N 256Kx1 Static RAM Document Number: 001-06495				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	424111	See ECN	NXR	New Data Sheet